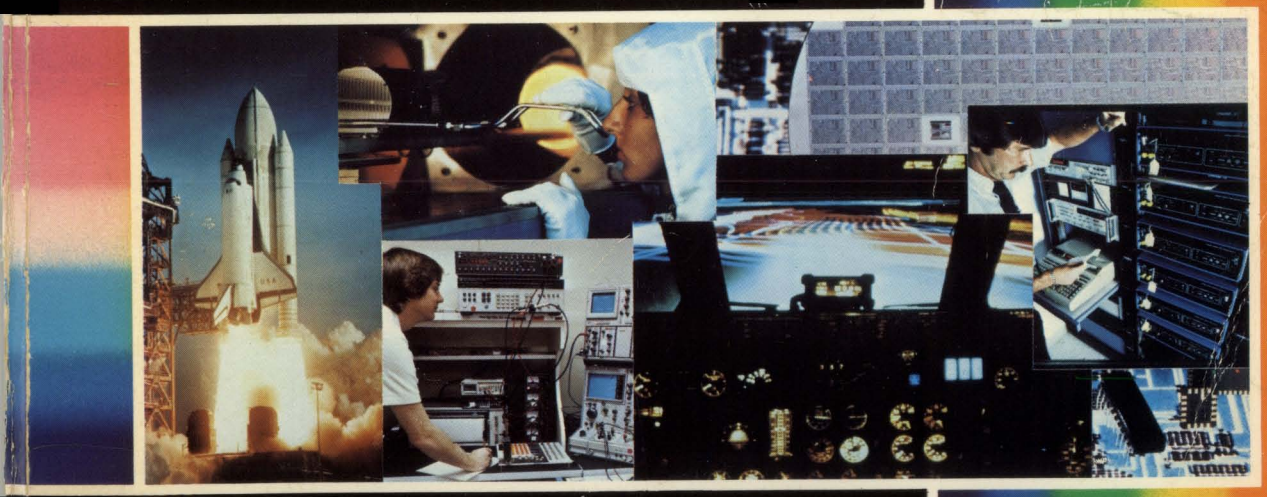
ANALOG

AND TELECOMMUNICATIONS PRODUCT DATA BOOK



Part of the Harris Spectrum of Integrated Circuits

HARRIS

Volume 4
$5.00

Harris Linear, Data Acquisition and Telecom Products

Harris Semiconductor Analog Products represent the state of the art in precision and high speed performance. Capitalizing on the advanced linear processing technologies developed over the past 17 years, Harris Semiconductor Analog Products offer high quality and unmatched performance.

This data book describes Harris Semiconductor's complete line of Linear, Data Acquisition and Telecommunication products, and includes a complete set of product specifications and data sheets, application notes and a separate section describing our quality and high reliability program.

All specifications in this data book are applicable only to packaged products. Specifications for dice are available upon request.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

Printed In USA

ANALOG

1984 Analog Data Book

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ANALOG

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Harris Semiconductor
Sector Capabilities

Harris Semiconductor is one of the five management groups of Harris Corporation, a producer of high-technology communication and information processing systems sold in over 160 countries. Five main operations of Harris Semiconductor produce standard and custom semiconductor devices. These operations are:

ANALOG PRODUCTS DIVISION

Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, sample-and-hold circuits and control functions, multiplexers, switches, voltage references, operational amplifiers, telecommunications, speech processing products, hybrid subsystem and active filters.

DIGITAL PRODUCTS DIVISION

Bipolar

Harris introduced the industry's first bipolar programmable read only memory in 1970 and has continued as a leader in the field of bipolar PROMs. Harris offers a complete spectrum of bipolar PROMs from 256 bits to 64K bits. Also, offered is a new family of programmable logic products featuring on-chip testability.

CMOS

Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products, and a full line of 80C86/88 microprocessors and peripherals. Semicustom circuit needs are met by a complete line of gate array and standard cell capabilities.

CUSTOM INTEGRATED CIRCUITS DIVISION

Harris designs, develops and manufactures custom analog, digital bipolar, radiation-hardened, and CMOS circuits for specialized military and commercial applications.

MICROWAVE SEMICONDUCTOR, INC.

Harris Microwave Semiconductor, Inc. develops and manufactures gallium arsenide transistors, integrated circuits and microwave amplifiers.

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Ordering Information

Harris proprietary Analog products are designated by "Harris Product Code". These products will always begin with the letter H and specific device numbers are isolated by hyphens. "Industry standards" are identified by their standardized part numbers and product. Examples of both product codes are shown below. When ordering, please refer to products by the full code identification.

HARRIS PRODUCT CODE EXAMPLE

H A 7 - 5135 - 5

PREFIX:
H (Harris)

FAMILY:
- A – Analog
- C – Communications
- D – Digital
- F – Filters
- I – Interface
- M – Memory
- V – Analog, High Voltage

PACKAGE:
- 1 – Dual-In-Line, Ceramic
- 2 – TO-5, Metal Can Type
- 3 – Dual In Line, Plastic
- 4 – Leadless Carriers
- 5 – LCC Hybrid
- 7 – Mini DIP, Ceramic
- 0 – Chip Form

PART NUMBER

TEMPERATURE:
- 1 – 0°C to 200°C*
- 2 – -55°C to +125°C
- 4 – -25°C to +85°C
- 5 – 0°C to +75°C
- 6 – 100% 25°C Probe (Dice Only)
- 7 – Dash-7 High Reliability Commercial Product. 0°C to +75°C
- 8 – Dash-8 Program HA2-2520-8 (Example Only)
- 9 – -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products Harris makes readily available via the high reliability DASH 8 program many products from our product lines. For details concerning this special Harris program for High Rel users, see Section 13 of this Data Book.

HARRIS DASH 7 PROGRAM

The Harris DASH 7 program extends the normal processing to include an added burn-in step for enhanced reliability. Details on DASH 7 are included in Section 13 of this Data Book.

HARRIS ANALOG JAN PROGRAM

In March 1980, Harris received JAN certification for the Analog Wafer Fabrication and Assembly facilities. All Harris Analog JAN products are produced on the certified line in strict compliance with all MIL-M-38510 program requirements.

Many Harris Analog high performance ICs are now available for immediate delivery in JAN Class B form. Consult your local Harris repesentative for an up-to-date list of all Harris JAN-qualified devices.

JAN from Harris offers the IC user high reliability, quality, and performance at a lower price and with faster delivery than similar products fabricated in accordance with non-standard source control drawings.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters, additionally desired parameters should be labeled, "Vendor will guarantee, but not necessarily test".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

IC Handling Procedures

Harris Analog I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C. internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Conductive plastic* mats on work benches and floor, connected to ground through a 1-M ohm resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground (the 1-M ohm resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient (operations should cease if R. H. falls below 25%).
- Ionized airblowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

*Supplier 3M Company
" Static Control Table Mat 8210/8210R"
"Static Control Floor Mat 8200/8200R"

Harris Analog IC Technologies

JUNCTION ISOLATION (J.I.)

This is the most common integrated circuit process. Bipolar I.C.'s generally begin with a p-type wafer into which a buried layer pattern, if used, is first diffused. Then the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area which is to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to

contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the I.C., base and emitter diffusions are performed, the wafer is coated with aluminum and the conductor pattern is etched.

Representative Harris devices using this process are HA-4741, HA-5082, and HA-5084.

DIELECTRIC ISOLATION (D.I.)

A somewhat different process has been proven particularly advantageous for fabricating high performance analog I.C.'s. This is dielectric isolation (D.I.), where each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide, and for mechanical strength imbedded in polycrystalline silicon. This process for bipolar I.C.'s begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern, then silicon dioxide and polycrystalline silicon are grown to fill the etched "moats". The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the I.C. D.I. for analog I.C.'s has a number of advantages:

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical J.I. op amps must use a lateral PNP which inherently has very low frequency response, limiting typical compensated bandwidth to 1MHz. The D.I. process makes it practical to build a vertical PNP with much higher bandwidth making possible compensated op amp bandwidths of 12MHz or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using D.I., further enhancing high frequency performance.
2. Other devices such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.
3. The isolation removes the possibility of parasitic SCR's which might create latchup under certain sequences of power and signal application.
4. Leakage currents to the substrate under high temperature conditions are greatly reduced. While the circuits in this data book were not specifically designed for operating temperatures greater than +125°C, many have shown superior performance. For I.C.'s requiring the ultimate in radiation resistance, Harris Semiconductor Programs Division should be consulted.

DIELECTRIC ISOLATED CMOS

J.I. processed CMOS Analog I.C.'s, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures and failures due to input voltage spikes. The D.I. CMOS process, which is compared in detail in Harris Application Note 521, has proved to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-506A through HI-509A and HI-506L through 509L multiplexers with built-in overvoltage protection.

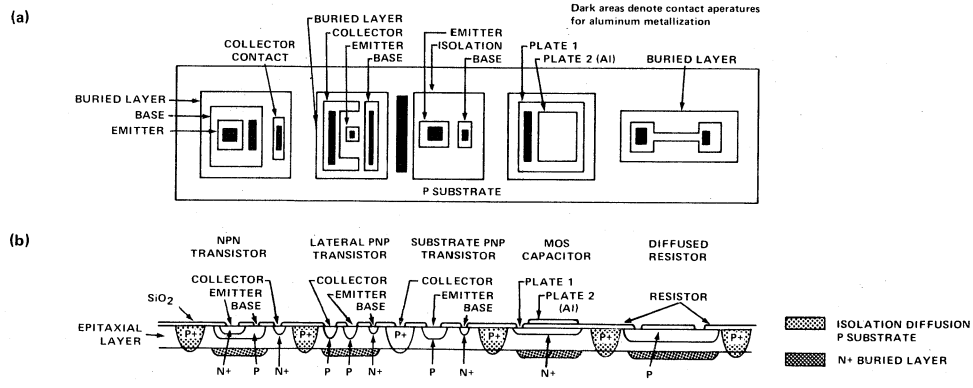


Figure 1 – Structures of various components formed in the junction-isolation process. (a) Topological view. (b) Cross-sectional view.

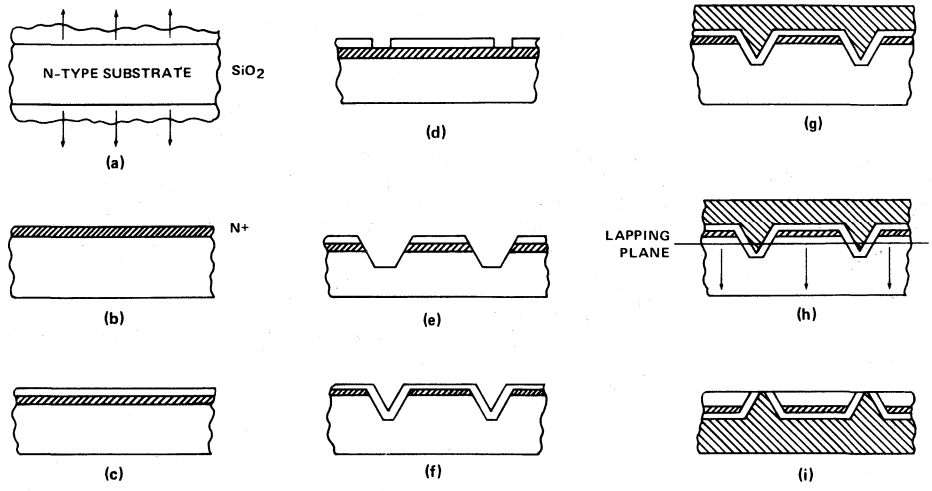


Figure 2 — Process steps for dielectric isolation. (a) Surface preparation, (b) N- buried layer diffusion, (c) masking oxide, (d) isolation pattern, (e) silicon etch, (f) dielectric oxide, (g) polycrystalline deposition, (h) backlap and polish, (i) finished slice.

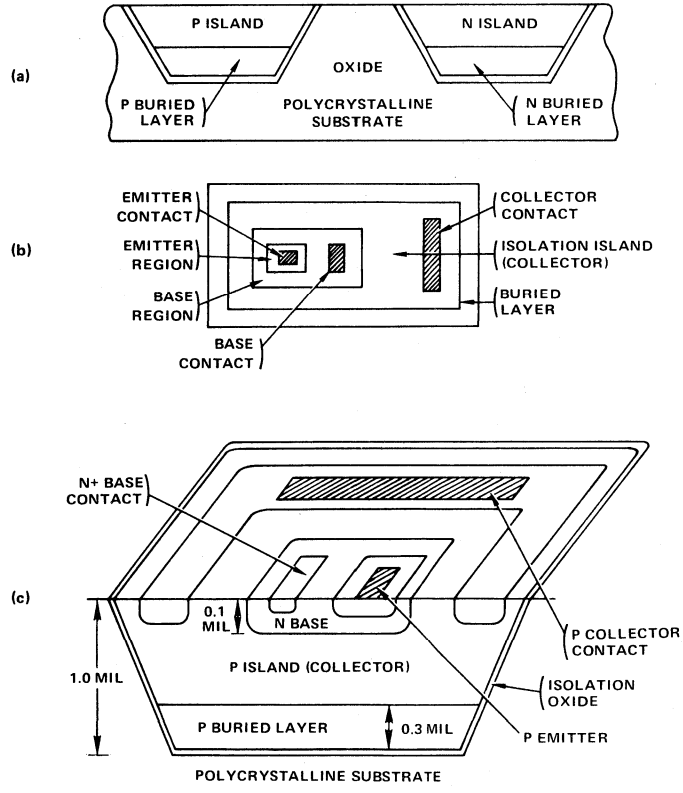


Figure 3 — The high-frequency process. (a) Cross-sectional view of P and N islands for PNP and NPN transistors. (b) Topological view showing relative placement of transistor regions. (c) Cross-sectional view of high-frequency PNP device formation in the D.I. process.

Competitive Cross Reference Chart

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
ADVANCED MICRO DEVICES (AMD)			
AM118	LM118		
AM1408		HI-5618-5	Faster, Application Resistors
AM1508		HI-5618-2	Faster, Application Resistors
AM318	LM318		
AM6012		HI-562A	Faster, Application Resistors Int. Linearity
		HI-5660	Int. Linearity, Application Resistors
AM6112		HI-774A	
AM6420		HA-5320	
		HA-5330	
LF198		HA-2420	Improved Performance
LF398		HA-2425	Improved Performance
SSS1408		HI-5618-5	Faster, Application Resistors
SSS1508		HI-5618-2	Faster, Application Resistors
ANALOG DEVICES (ADI)			
52		HA-5180	Monolithic
AD1408		HI-5618-5	Faster, Application Resistors
AD1508		HI-5618-2	Faster, Application Resistors
AD362		HI-5900/01	Faster
AD380		HA-2541	Monolithic
AD381		HA-2541	Monolithic
AD389		HA-5320	Faster, Monolithic
AD507	HA-2620		Identical
AD509	HA-2520		Identical
AD515		HA-5180	Monolithic
AD518	LM318		
AD542L		HA-5170	Better AC
AD544		HA-5100	
AD545	HA-5180		Monolithic
AD547J	HA-5170		Better AC
AD562		HI-562A	Faster
		HI-5660	Faster
AD563		HI-565A	Faster
AD565	HI-565A		Faster
AD565A	HI-565A		
AD566		HI-5660	
		HI-562	
AD566A		HI-5660	
		HI-562A	
AD574A	HI-574A		Digital timing, Faster
AD581		HI-1608	
AD582		HA-2420/25	Acquisition time
AD583K	HA-2425-5		Identical

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
ANALOG DEVICES (ADI) (continued)			
AD583K	HA-2425-5		Identical
		HA-5320	Faster, Better Accuracy
AD7501		HI-508	DI Process
AD7502		HI-509	DI Process
AD7503		HI-1818A	DI Process
AD7506	HI-506		DI Process
AD7507	HI-507		DI Process
AD7511		HI-201	
AD7512		HI-5043	
AD7521/31	HI-7541		Improved Linearity
AD7541/41A	HI-7541		Lower Output Capacitance
ADADC80		HI-574A	Power, Smaller pkg.
		HI-674A	Faster, Power, Smaller Pkg.
ADADC84/85		HI-674A	Power, Smaller Pkg.
		HI-774A	Faster, Power, Small Pkg.
ADDAC 08		HI-5618	Faster, Application Resistors
ADDAC 80		HI-5680	Faster
ADDAC 85		HI-5685	Faster
ADDAC 87		HI-5687	Faster
ADG200		HI-200	
ADLH0032		HA-5190	Monolithic
H0S050		HA-2542	Monolithic
H0S100	HA-5033		Monolithic
ANALOGIC			
MN4708		HI-508	
		HI-1818A	
MP1812A		HI-5680V	Faster, Monolithic, Power, Smaller Pkg.
MP250M		HA-2420/25	Faster, Monolithic, Smaller Pkg.
MP260		HA-2420/25	Monolithic, Smaller Pkg.
MP261		HA-2420	Monolithic, Smaller Pkg.
MP270/271		HA-5320	Monolithic, Smaller Pkg.
BECKMAN			
7541	HI-7541		Faster, Monolithic
7556		HI-574A	Faster, Smaller Pkg.
7580		HI-5680	Faster, Monolithic
BURR-BROWN			
3500		HA-2600	Better AC
3503	HA-2505		Identical
3506	HA-2605		Identical
3507	HA-2525		Identical
3508	HA-2625		Identical
3521		HA-5170	Better AC

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
BURR-BROWN (continued)			
3522	HA-5280		Better AC and DC
3523		HA-5180	Better AC
3527	HA-5180		Better AC and DC
3528		HA-5180	Better AC
3550		HA-2541	Monolithic
3553		HA-5033	Monolithic
3554		HA-2542	Monolithic
ADC80		HI-574A	Smaller Pkg.,Power
		HI-674A	Faster, Smaller Pkg.,Power
ADC84/85		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller Pkg., Power
ADC87		HI-774A	Smaller Pkg., Power
DAC70		HI-DAC16	Faster, Monolithic
DAC700/701		HI-DAC16	
DAC702/703		HI-DAC16	
DAC71/72		HI-DAC16	Monolithic, "I" Output
DAC80	HI-5680		Faster, Monolithic, Power
DAC800	HI-5680		Faster, Lower Power
DAC85	HI-5685		Faster, Monolithic, Power
DAC850	HI-5685		Faster, Lower Power
DAC851	HI-5687		Faster, Lower Power
DAC87	HI-5687		Faster, Monolithic,Power
DAC870	HI-5687		Faster, Monolithic
MPC16S	HI-506A-5		Identical
MPC4D	HI-509A-5		Identical
MPC800KG	HI-516-5		Identical
MPC801KG	HI-518-5		Identical
MPC801SG	HI-518-2		Identical
MPC8D	HI-507A-5		Identical
MPC8S	HI-508A-5		Identical
OPA11	HA-2600		
OPA101		HA-5110	Better AC
OPA102		HA-5110	
OPA103		HA-5180	Better AC
OPA104		HA-5180	
SHC298AM		HA-2425	Improved Performance
SHC80/85		HA-2425	Faster, Monolithic, Power
SHC85ET		HA-2420	Faster, Monolithic, Power
SHM60		HA-5320	Monolithic, Smaller Pkg.
DATA DEVICE CORP. (DDC)			
ADH051		HA-5330	Monolithic, Smaller Pkg., Power
ADH8585		HI-674A	Smaller pkg., Power
		HI-774A	Faster, Smaller Pkg.

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
DATA DEVICE CORP. (DDC) (continued)			
ADH8586		HI-774A	Smaller Pkg., Power
DDC5200		HI-574A	Faster
DDC5210/11		HI-674A	
DDC5212/16		HI-674A	
DDC5240		HI-774A	Smaller Pkg., Power
DDCADC85		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller Pkg., Power
DDCADC87		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller Pkg., Power
DDCDAC85LD	HI-5685		Monolithic, Power
DDCDAC87	HI-5687		Monolithic, Power
DGL13		HA-5320	Monolithic, Smaller Pkg. Power
THC4460		HA-5320	Monolithic, Smaller Pkg.
DATEL			
ADC52XX		HI-674A	Lower Power
		HI-774A	Faster, Lower Power
ADC574A	HI-574A		Identical
ADC8412		HI-674A	Smaller Pkg. Power
		HI-774A	Faster, Smaller Pkg., Power
ADC85C12		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller pkg., Power
ADC8712		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller Pkg., Power
ADCEH12B1		HI-774A	Faster, Smaller Pkg., Power
ADCHX12B		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
ADCL12B2		HI-574A	Smaller Pkg.
		HI-674A	Faster, Smaller Pkg.
ADCM12B2		HI-674A	Smaller Pkg.
		HI-774A	Faster, Smaller Pkg.
ADCMA12B2A		HI-574A	Faster, Smaller Pkg.
ADCMA12B2B		HI-574A	Smaller Pkg.
		HI-674A	Faster, Smaller Pkg.
AM450	HA-2505		
AM452	HA-2525		
AM460	HA-2605		
AM462	HA-2625		
AM464	HA-2645		
DAC08B		HI-5618	Faster, Application Resistors

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
DATEL (continued)			
DAC562	HI-562A		Identical
DAC71/72		HI-DAC16	Monolithic
DAC7541	HI-7541		Equivalent
DAC85	HI-5685		Faster, Monolithic, Power
DAC85C	HI-5680		Faster, Monolithic, Power
DAC87	HI-5687		Faster, Monolithic, Power
DACHA12B	HI-7541		Faster, Monolithic
DACHP16B		HI-DAC16	Monolithic
DACHR16B		HI-DAC16	Monolithic, Smaller Pkg.
DACHZ12B		HI-5680/85/87	Faster, Monolithic
DACIC10B		HI-5610	Faster, Application Resistors
DACIC8B		HI-5618	Faster, Application Resistors
MV1606	HI-506		Identical
MV808	HI-1818A		Identical
MVD409	HI-1828A		Identical
MVD807	HI-507		Identical
MX1606	HI-506A		Identical
MX1616	HI-516		Identical
MX808	HI-508A		Identical
MX818	HI-518		Identical
MXD409	HI-509A		Identical
MXD807	HI-507A		Identical
SHM1C-1	HA-2425		Identical
SHM1C-1M	HA-2420		Identical
SHM20	HA-5320		Identical
SHM6M		HA-5320	Monolithic, Smaller Pkg.
		HA-5330	Faster, Monolithic, Smaller Pkg.
SHM9M		HA-2420	Faster, Monolithic, Smaller Pkg.
SHMLM-2		HA-2420	Faster
EXAR			
XR4212		HA-4741	
FAIRCHILD			
μA0801/02		HI-5618	Faster, Application Resistors
μA198		HA-2420	Improved Performance
μA398		HA-2425	Improved Performance
μA565	HI-565A		
μA702		HA-2620	Improved Performance
μA709		HA-2620	
μA714		HA-5130	Better DC
μA715		HA-2520	Better AC
μA727		HA-5130	Better DC
μA740		HA-5170	Better AC

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
FAIRCHILD (continued)			
μA741	HA-2600		Better AC
μA747	HA-5102		Better noise
μA748		HA-2600	Better AC
μA776	HA-2720		Better AC and noise
μA1458	HA-5102		Better AC and noise
μA1558	HA-5102		Better AC and noise
HITACHI			
HA-17408		HI-5618	Faster, Application Resistors
HYBRID SYSTEMS			
ADC550		HI-574A	Faster, Smaller Pkg., Power
ADC581		HI-574A	
		HI-674A	Faster
DAC328I-16		HI-DAC16	Monolithic, Smaller Pkg.
DAC331-12	HI-7541		Faster
DAC335-12		HI-5687V	Faster, Monolithic
DAC346C-12		HI-5680V	Faster, Monolithic
DAC347LP-12		HI-5687V	Faster, Monolithic
DAC372		HI-5680	Monolithic
DAC3721-10		HI-5610	Faster, Monolithic, Smaller Pkg.
DAC3721-8		HI-5618	Faster, Monolithic
DAC395-8		HI-5618	Monolithic, Smaller Pkg.
HS346		HA-5320	Faster, Monolithic
HS5200		HI-674A	
		HI-774A	Faster
HS574	HI-574A		Digital timing, Faster
HS730		HA-5320	Monolithic, Smaller Pkg.
		HA-5330	Faster, Monolithic, Smaller Pkg.
HS7541	HI-7541		Lower Output Capacitance
HSDAC80		HI-5680	Faster, Monolithic, Power
HSDAC87	HI-5687		Faster, Monolithic, Power
MUX201	HI-1818A		Lower Power, Smaller Pkg.
SH725		HA-2420	Faster, Monolithic, Smaller Pkg.
INTECH			
104BIN-P		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
411-10BIN		HI-5610	Faster, Smaller Pkg.
416 BIN		HI-DAC16	Smaller Pkg.
A3103		HI-674A	Smaller Pkg., Power
		HI-774A	Faster, Smaller Pkg., Power

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
INTECH (continued)			
A3155		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
A880/880-2		HA-5320	Faster, Monolithic, Power
A881		HA-5320	Monolithic, Smaller Pkg., Power
A882/884		HA-2420/25	Faster, Monolithic, Power
ADC111		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
ADC2812		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
ASH240/250		HA-2420/25	Monolithic, Smaller Pkg., Power
ASH271		HA-5320	Monolithic, Smaller Pkg., Power
CY2219		HI-7541	Faster, Smaller Pkg., Power
CYAAD12QM		HI-574A	Smaller Pkg., Power
		HI-674A	Faster, Smaller Pkg., Power
INTEL			
D2912	HC-5512		Lower Power, Lower Noise
D2912A	HC-5512		Lower Power, Lower Noise
	HC-5512A		Lower Power,Lower Noise
D2910	HC-5510		Lower Power, Two Supplies
D2910A	HC-5510		Lower Power, Two Supplies
D2911	HC-5511		Lower Power, Two Supplies
D2911A	HC-5511		Lower Power, Two Supplies
INTERSIL			
AD7521/31	HI-7541		Improved Linearity
AD7541	HI-7541		Lower output capacitance
DG200	HI-200		Dielectric Isolation
DG201	HI-201		Dielectric Isolation
HA-2500	HA-2500		Identical
HA-2510	HA-2510		Identical
HA-2520	HA-2520		Identical
HA-2600	HA-2600		Identical
HA-2620	HA-2620		Identical
ICL7611	HA-2720		Better noise
ICL7615	HA-5141		Better AC and noise
ICL7621	HA-5142		Better AC and noise
ICL7642	HA-5144		Better AC and noise
ICL8017		HA-2520	
ICL8021	HA-2720		Better AC
ICL8075		HA-1608	
ICL8211		HA-1608	
IH201	HI-201		Dielectric Isolation
IH5040	HI-5040		Dielectric Isolation
IH5041	HI-5041		Dielectric Isolation

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
INTERSIL (continued)			
IH5042	HI-5042		Dielectric Isolation
IH5043	HI-5043		Dielectric Isolation
IH5044	HI-5044		Dielectric Isolation
IH5045	HI-5045		Dielectric Isolation
IH5046	HI-5046		Dielectric Isolation
IH5047	HI-5047		Dielectric Isolation
IH5048	HI-5048		Dielectric Isolation
IH5049	HI-5049		Dielectric Isolation
IH5050	HI-5050		Dielectric Isolation
IH5051	HI-5051		Dielectric Isolation
IH5108		HI-508A	Signal Range, Same Pin-out
IH5110/11		HA-2420/25	Monolithic
IH5112/13		HA-2420/25	Monolithic
IH5114/15		HA-2420/25	Monolithic
IH5200	HI-200		Dielectric Isolation
IH5201	HI-201		Dielectric Isolation
IH5208		HI-509A	Vin Range, Same pin-out
IH6108		HI-508	Ron, DI, Same pin-out
IH6116		HI-506	Ron, DI, Same pin-out
IH6208		HI-509	Ron, DI, Same pin-out
IH6216		HI-507	Ron, DI, Same pin-out
LM4250	HA-2720		Better AC and noise
INTRONICS			
A-560	HA-2525		
A-561	HA-2625		
MICRO NETWORKS (MNI)			
ADC80		HI-574A	Smaller pkg., Power
		HI-674A	Faster, Smaller pkg., Power
DAC80	HI-5680		Faster, Monolithic, Power
DAC85	HI-5685		Faster, Monolithic, Power
DAC87	HI-5687		Faster, Monolithic, Power
MN-ADC84/85/87		HI-674A	Smaller pkg., Power
		HI-774A	Faster, Smaller pkg., Power
MN3009		HI-5618	Monolithic
MN3014		HI-5618	Monolithic
MN3348		HI-5680V/87V	Faster, Monolithic, Power
MN3349		HI-5685V/87V	Faster, Monolithic
MN3412		HI-7541	Monolithic
MN343/344		HA-2420	Faster, Monolithic
MN346/347		HA-5320	Faster, Monolithic
MN370/371		HI-5687V	Monolithic
MN373		HA-5320	Faster, Monolithic
MN375		HA-5330	Monolithic, Lower Power
MN5200		HI-574A	Faster
MN5210		HI-674A	Two Chip Design
		HI-774A	Faster, Two Chip Design

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
MICRO NETWORKS (MNI) (continued)			
MN5240		HI-774A	Smaller Pkg., Power
MN565A	HI-565A		
MN574A	HI-574A		Faster
MICRO POWER SYSTEMS (MPS)			
MP200DI	HI-200		
MP201DI	HI-201		
MP5507	HA-OP07		Better AC
MP5527	HA-OP27		
MP5532		HA-1608	
MP5537	HA-OP27		
MP562	HI-562A		Faster
MP574	HI-574A		Digital timing, Faster
MP7501/03		HI-1818A	
MP7502		HI-1828A	
MP7506	HI-506		DI Processing
MP7507	HI-507		DI Processing
MP7508DI	HI-508A		Input Overvoltage Isolation
MP7509DI	HI-509A		Input Overvoltage Isolation
MP7521/31	HI-7541		Improved Performance
MP7541	HI-7541		
MP7621/23	HI-7541		
MITEL			
MT8912	HC-5512		Better noise, better cross talk
MOSTEK			
MK5912	HC-5512		Better noise
MOTOROLA			
LF155		HA-5100	Better DC
LF155A		HA-5100	Better DC
LF156		HA-5100	Better DC
LF156A		HA-5100	Better DC
LF157		HA-5110	Better DC
LF157A		HA-5110	Better DC
LF355		HA-5105	Better DC
LF355A		HA-5105	Better DC
LF356		HA-5105	Better DC
LF356A		HA-5105	Better DC
LF357		HA-5115	Better DC
LF357A		HA-5115	Better DC
MC1408		HI-5618-5	Faster, Application Resistors
MC1430		HA-2600	Better AC
MC1431		HA-2600	Better AC
MC1436		HA-2640	Better AC and DC

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
MOTOROLA (continued)			
MC1458	HA-5102		Better AC and noise
MC1508		HI-5618-2	Faster, Application Resistors
MC1558	HA-5102		Better AC and noise
MC1748		HA-2600	Better AC and DC
MC1776	HA-2720		Better AC and noise
MC3403		HA-4741	Better AC
MC3410		HI-5610-5	Faster, Application Resistors
MC3412	HI-565A		
MC3417		HC-55564	Lower power, few external components
MC3419		HC5502	Better longitudinal balance
		HC5504	Better Transhybrid loss Fewer external components
MC3510		HI-5610-2	Faster Application Resistors
MC4741	HA-4741		Better AC Fewer external components
MC34002	HA-5082		Better AC
MC34004	HA-5084		Better AC
MC35002	HA-5082		Better AC
MC35004	HA-5084		Better AC
NATIONAL SEMICONDUCTOR (NSC)			
AD7521/31	HI-7541		Improved Linearity
ADC1080/1280		HI-574A	Smaller Pkg., Lower Power
		HI-674A	Faster, Smaller pkg. Power
ADC1210/11		HI-574A	Faster, Complete A/D
DAC0800/01/02		HI-5618	Faster, Application Resistors
DAC0806/06/08		HI-5618	Faster, Application Resistors
DAC1200/01		HI-5685V/87V	Faster, Lower Power
DAC1218/19	HI-7541		
DAC1220/21/22	HI-7541		Improved Linearity
DAC1265	HI-565A		
DAC1266		HI-5660	
DAC1280		HI-5680	Monolithic, Performance
DAC1285		HI-5685/87	Monolithic, Performance
LF0023/43		HA-2420	Monolithic, Performance
LF0053		HA-2420/25	Monolithic
		HA-5320	Faster, Monolithic
LF147	HI-5084		
LF151		HA-5100	

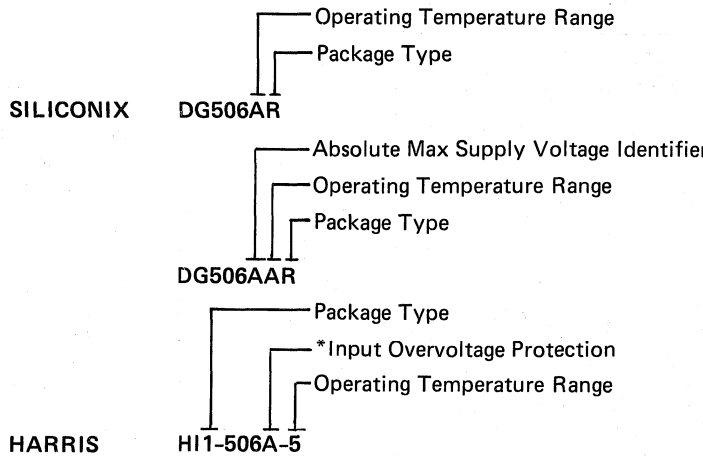
MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
NATIONAL SEMICONDUCTOR (NSC) (continued)			
LF153	HA-5082		
LF155		HA-5100	Better DC
LF155A		HA-5100	Better DC
LF156		HA-5100	Better DC
LF156A		HA-5100	Better DC
LF157		HA-5110	Better DC
LF157A		HA-5110	Better DC
LF198		HA-2420	Improved Performance
LF247	HA-5084		
LF253	HA-5082		
LF347	HA-5084		
LF351		HA-5105	Better DC
LF353	HA-5082		
LF355		HA-5105	Better DC
LF355A		HA-5105	Better DC
LF356		HA-5105	Better DC
LF356A		HA-5105	Better DC
LF357		HA-5115	Better DC
LF357A		HA-5115	Better DC
LF398		HA-2425	Improved Performance
LF412	HA-5082		
LF412A	HA-5082		
LF441		HA-5141	Better noise
LF442	HA-5062		
LF444	HA-5064		
LF11201	HI-201		C-MOS Dielectric Isolation
LF11508	HI-508-2		Faster, Ron, Power
LF11509	HI-509-2		Faster, Ron, Power
LF13201	HI-201		C-MOS Dielectric Isolation
LF13508	HI-508-5		Faster, Ron, Power
LF13509	HI-509-5		Faster, Ron, Power
LH0002		HA-5033	Monolithic, Better AC and DC
LH0003		HA-2520	Monolithic
LH0004		HA-2640	Monolithic
LH0005		HA-2620	Monolithic
LH0022		HA-5180	Monolithic, better AC and DC
LH0032	HA-2541		Monolithic
LH0033		HA-5033	Monolithic, better DC
LH0042		HA-5180	Monolithic, better AC and DC
LH0052		HA-5180	Monolithic, better AC
LH0062		HA-5160	Monolithic, better AC
LH0072		HA-1608	Monolithic, better DC
LM108	HA-5135		Better DC and AC
LM108A	HA-5135		Better DC and AC
LM118	LM118		
LM124		HA-4741	Better AC
LM143	LM143		
LM144		HA-2640	
LM146	HA-2740		
LM148		HA-4741	Better AC
LM208	HA-5135		Better DC and AC
LM208A	HA-5135		Better DC and AC
LM308	HA-5135		Better DC and AC

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
NATIONAL SEMICONDUCTOR (NSC) (continued)			
LM308A	HA-5135		Better DC and AC
LM318	LM318		
LM324		HA-4741	Better AC
LM343	LM343		
LM344		HA-2640	
LM346	HA-2740		
LM348		HA-4741	Better AC
LM3080	HA-23080		
LM4250	HA-2720		Better noise
TP3040	HC-5512		Identical
TP3040A	HC-5512A		Identical
TP3020	HC-5510		Identical
TP3021	HC-5511		Identical
TP3054	HC-5554		Better Asychronous Performance
TP3057	HC-5557		Better Asychronous Performance
PRECISION MONOLITHICS INC. (PMI)			
DAC-08		HI-5618	Faster, Application Resistors
DAC-10		HI-5610	Application Resistors
DAC-100		HI-5610	Faster, Monolithic
DAC-1408		HI-5618-5	Faster, Application Resistors
DAC-1508		HI-5618-2	Faster, Application Resistors
DAC-312		HI-562A	Int. Linearity, Application Resistors
DMX-88	HI-508		V_{IN} Range, Lower Power
GAP01		HA-2400	4 channels
MUX-08	HI-508A		V_{IN} Range, Lower Power
MUX-16	HI-506A		V_{IN} Range, Lower Power
MUX-24	HI-509A		V_{IN} Range, Lower Power
MUX-28	HI-507A		V_{IN} Range, Lower Power
MUX-88	HI-508A		V_{IN} Range, Lower Power
OP01		HA-2500	Better AC
OP05	HA-5135		Better AC and DC
OP07	HA-OP07		Better AC and DC
OP11		HA-4741	
OP15		HA-5100	Better AC
OP16		HA-5100	
OP17		HA-5110	Better AC
OP20	HA-5141		Better AC
OP27	HA-OP27		
OP37	HA-OP37		
OP220	HA-5142		Better AC
OP420	HA-5144		Better AC
PM-562		HI-562A	Faster
REF01		HA-1608	
SMP-10/11		HA-2420/25	Lower Power
		HA-5320	Faster, Improved Accuracy
SMP-81		HA-2420/25	Lower Power
		HA-5320	Faster, Improved Accuracy
SSS1458	HA-5102		Better AC and noise
SSS1558	HA-5102		Better AC and noise

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
RAYTHEON (RAY)			
LF155		HA-5100	Better DC
LF155A		HA-5100	Better DC
LF156		HA-5100	Better DC
LF156A		HA-5100	Better DC
LF157		HA-5110	Better DC
LF157A		HA-5110	Better DC
LF355		HA-5105	Better DC
LF355A		HA-5105	Better DC
LF356		HA-5105	Better DC
LF356A		HA-5105	Better DC
LF357		HA-5115	Better DC
LF357A		HA-5115	Better DC
LM108	HA-5135		Better AC and DC
LM108A	HA-5135		Better AC and DC
LM118	LM118		
LM124		HA-4741	Better AC
LM148		HA-4741	Better AC
LM208	HA-5135		Better AC and DC
LM208A	HA-5135		Better AC and DC
LM308	HA-5135		Better AC and DC
LM308A	HA-5135		Better AC and DC
LM318	LM318		
LM324		HA-4741	Better AC
LM348		HA-4741	Better AC
RC1556	HA-2605		Better AC and DC
RC4131	HA-2605		Better AC
RC4136		HA-4741	
RC4156	HA-4156		
RC4531	HA-2505		Dielectric Isolation
RC4741	HA-4741		Better AC
RM1556	HA-2600		Better AC and DC
RM4131	HA-2600		Better AC
RM4136		HA-4741	
RM4156	HA-4741		
RM4531	HA-2500		Dielectric Isolation
RM4741	HA-4741		Better AC
RCA			
CA3020		HA-2630	
CA3078		HA-5144	
CA3080	HA-23080		Better AC and DC
CA3100	HA-2620		
CA6078		HA-2720	
CD4016		HI-201	Better AC and DC

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
SIGNETICS (SIG)			
AM6012		HI-562A	Int. Linearity, Application Resistors
		HI-5660	Int. Linearity, Application Resistors
DAC08		HI-5618	Faster, Application Resistors
LF198		HA-2420	Improved Performance
LF398		HA-2425	Improved Performance
MC1408		HI-5618-5	Faster, Application Resistors
MC1508		HI-5618-2	Faster, Application Resistors
MC3410/10C		HI-5610-5	Faster, Application Resistors
MC3510		HI-5610-2	Faster, Application Resistors
NE531		HA-2515	
NE5410		HI-5610-5	Faster, Application Resistors
NE5532		HA-5102	Better noise
NE5533		HA-5112	Better noise
NE5534		HA-5135	
NE5537		HA-2425-5	Lower Power
		HA-5320-5	Faster
NE5539		HA-2539	Better AC
SE531		HA-2510	
SE5410		HI-5610-2	Faster, Application Resistors
SE5532		HA-5102	Better noise
SE5533		HA-5112	Better noise
SE5534		HA-5135	
SE5539		HA-2539	Better AC
SILICON-GENERAL			
SG741		HA-2500	
SG3551	HA-23551		
SILICONIX			
DG181		HI-381	Dielectric Isolation
DG182		HI-381	Dielectric Isolation
DG184		HI-384	Dielectric Isolation
DG185		HI-384	Dielectric Isolation
DG187		HI-387	Dielectric Isolation
DG188		HI-387	Dielectric Isolation
DG190		HI-390	Dielectric Isolation
DG191		HI-390	Dielectric Isolation
DG200A	HI-200		Dielectric Isolation
DG201A	HI-201		Dielectric Isolation
DG211		HI-201	Full temp range specified
DG300A	HI-300		Dielectric Isolation
DG301A	HI-301		Dielectric Isolation
DG302A	HI-302		Dielectric Isolation
DG303A	HI-303		Dielectric Isolation

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
SILICONIX (continued)			
DG304A	HI-304		Dielectric Isolation
DG305A	HI-305		Dielectric Isolation
DG306A	HI-306		Dielectric Isolation
DG307A	HI-307		Dielectric Isolation
DG381A	HI-381		Dielectric Isolation
DG384A	HI-384		Dielectric Isolation
DG387A	HI-387		Dielectric Isolation
DG390A	HI-390		Dielectric Isolation
DG5040	HI-5040		Dielectric Isolation
DG5041	HI-5041		Dielectric Isolation
DG5042	HI-5042		Dielectric Isolation
DG5043	HI-5043		Dielectric Isolation
DG5044	HI-5044		Dielectric Isolation
DG5045	HI-5045		Dielectric Isolation
DG506	HI-506		Lower Power, DI processing
DG506A	HI-506		Lower Power, DI processing
DG507	HI-507		Lower Power, DI processing
DG507A	HI-507		Lower Power, DI processing
DG508	HI-508		Lower Power, DI processing
DG508A	HI-508		Lower Power, DI processing
DG509	HI-509		Lower Power, DI processing
DG509A	HI-509		Lower Power, DI processing
DG528		HI-508L	Overvoltage prot., DI processing
DG529		HI-509L	Overvoltage prot., DI processing
SD5200		HI-201HS	Dielectric Isolation



*Note: The Harris HI-50XA family features input overvoltage protection for which there are no Siliconix equivalents.

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
SOLITRON			
CM4016A		HI-201	Better AC and DC
UC4000		HA-2600	
UC4002		HA-2605	
UC4250	HA-2720		Better AC and noise
SPRAGUE			
ULN2139		HA-2600	
ULN2151		HA-2600	
ULN2156		HA-2600	
ULN2157		HA-2650	
ULN2158		HA-2650	
ULN2171		HA-2600	
ULN2172		HA-2620	
ULN2173		HA-2600	
ULN2174		HA-2620	
ULN2175		HA-2600	
ULN2176		HA-2600	
TELEDYNE PHILBRICK			
1321	HA-2620		Identical
1322	HA-2520		Identical
1332	HA-2645		Identical
1339		HA-2625	
1341	HA-2540		Identical
1342	HA-2539		Identical
1343	HA-5190		Identical
1344	HA-5160		Identical
1345	HA-5162		Identical
1346	HA-5180		Identical
1347	HA-5180A		Identical
1437		HA-2541	Monolithic
1438		HA-2541	Monolithic
1460		HA-2542	Monolithic
1466		HA-2542	Monolithic
4058		HI-5680	Monolithic
4058-83		HI-5687	Monolithic
4068A	HI-562A		Identical
4084	HI-5618		Identical
4088	HI-DAC16		Identical
4189		HI-774A	
4551	HI-507A		Identical
4552	HI-506A		Identical
4553	HI-509A		Identical
4554	HI-508A		Identical
4853		HA-5320	Monolithic, Smaller Pkg.
4854		HA-2420	Faster, Monolithic, Smaller pkg.

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
TELEDYNE PHILBRICK (continued)			
4856	HA-2420/25		Identical
4857		HA-5320	Monolithic, Smaller pkg., Power
4866	HA-5320		Identical
7541	HI-7541		Identical
DAC80I/V	HI-5680I/V		Identical
TP5210		HI-674A	
		HI-774A	Faster
TP565A	HI-565A		Identical
TP574A	HI-574A		Identical
TPADC85/87		HI-774A	
TEXAS INSTRUMENTS (TI)			
MC1458	HA-5102		Better noise
MC1558	HA-5102		Better noise
TCM2910A	HC-5510		Lower power, two supplies
TCM2911A	HC-5511		Lower power, two supplies
TCM2912C	HC-5512		Better noise, better cross talk lower power
TCM4110	HC-5510		Lower power, two supplies
TCM4910	HC-5510		Lower power, two supplies
TL022	HA-5142		Better DC
TL044		HA-5144	Better DC
TL061		HA-5141	Better DC and noise
TL062	HA-5062		MIL range available
TL064	HA-5064		MIL range available
TL072	HA-5082		MIL range available
TL074	HA-5084		MIL range available
TL081		HA-5100	Better DC
TL082	HA-5082		MIL range available
TL084	HA-5084		MIL range available
TRANSITRON			
TOA7709	HA-2600		
TOA8709	HA-2605		

High Temperature Electronics

To serve the growing need for electronics that will operate in severe high temperature environments, Harris will offer integrated circuits that have been characterized over elevated temperatures and that have electrical characteristics guaranteed at 200°C.

Typical applications include:

- Well Logging
- Industrial Process Control
- Engine Control and Testing
- High Temperature Data Acquisition Systems

It is the intention of Harris Semiconductor to make available in the high temperature series (identified by the -1 suffix following the device part number) all the basic elements required for the designer to build a data acquisition system that will function to specified limits at 200°C.

The devices to be offered:

- Operational Amplifiers
- Analog Switches
- Analog Multiplexers
- 12 Bit Digital to Analog Converter
- Sample & Hold Amplifiers
  A/D Converters

All parts offered in the -1 series have had their electrical performance parameters characterized up to 250°C.

Production flow of -1 parts includes 160 hours burn-in and final electrical test at 200°C.

Devices available Now:

• HA-2420-1	Sample & Hold Amplifier
• HA-2600-1	Operational Amplifier
• HA-2620-1	Operational Amplifier
• HA-4640-1	Quad Operational Amplifier
• HI-200-1	Analog Switch
• HI-201-1	Analog Switch

Consult factory for price and availability information.

Advanced Packaging Techniques

Harris Semiconductor is now offering Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is essentially comprised of the cavity and seal ring section of a standard DIP. It offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

The LCC's two principle advantages over conventional side braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependant on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28, and 48 lead LCCs to 18, 28, and 48 lead side braze DIPs. The chart indicates a 270% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously,sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side braze DIPs. As pin

count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex, these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is significantly smaller determinant of system performance.

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by small hermetic package in which internal water vapor content can be carefully controlled during production.

In summary, Harris Semiconductor Leadless Chip Carriers use a proven technology to provide a reliable high density, high performance packaging option for today's systems.

A list of products available in LCC form is provided in the Packaging Section on page 11-6. Consult the factory or your Harris sales representative for pricing and availability.

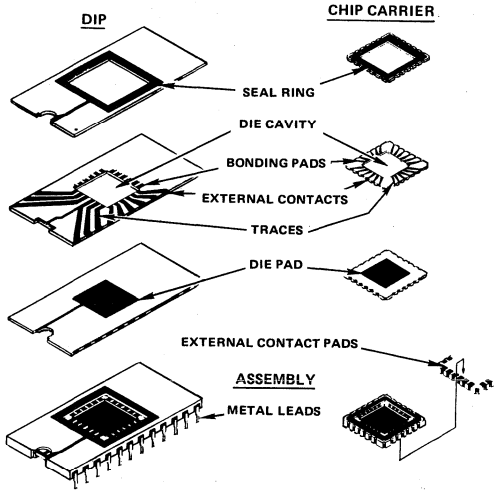
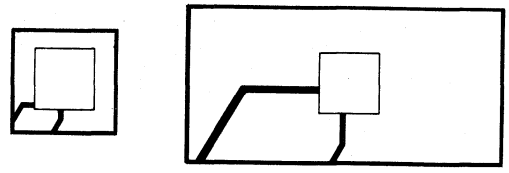


FIGURE 1. Exploded view of Chip Carrier and DIP.



LEAD COUNT	LONGEST TRACE DIP / LONGEST TRACE CC	LONGEST TRACE / SHORTEST TRACE	
		CC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. Electrical Performance (Resistance and Speed)

TABLE I

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA VS. LCC AREA
18	0.10	0.22	270%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All units in square inches)

ANALOG

Operational Amplifiers, Comparators & Control Functions

2

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Operational Amplifiers, Comparators and Control Functions

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HA-OP07	Precision Operational Amplifier	2-10
Advance HA-OP27	Precision, Low Noise Operational Amplifier	2-18
Advance HA-OP37	High Slew Rate, Precision, Low Noise Operational Amplifier	2-19
HA-1608	+10V Adjustable Voltage Reference	2-20
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HA-2500/02/05	High Slew Rate Operational Amplifiers	2-27
HA-2510/12/15	High Slew Rate Operational Amplifiers	2-31
HA-2520/22/25	High Slew Rate Operational Amplifiers	2-35
HA-2539	High Slew Rate, Wide Bandwidth Operational Amplifier	2-39
HA-2540	High Slew Rate, Wide Bandwidth Operational Amplifier	2-45
Advance HA-2541	High Slew Rate, Unity Gain Stable Op Amp	2-51
Advance HA-2542	High Slew Rate, Power Op Amp	2-52
HA-2600/02/05	General Purpose High Performance Operational Amplifiers	2-53
HA-2620/22/25	Wide Bandwidth Operational Amplifiers	2-57
HA-2630/35	High Performance Current Boosters	2-61
HA-2640/45	High Voltage Operational Amplifiers	2-65
HA-2650/55	Dual General Purpose High Performance Op Amp	2-69
HA-2720/25	Programmable Low Power Operational Amplifiers	2-73
HA-2730/35	Dual Programmable Low Power Op Amps	2-79
HA-2740	Quad Programmable Low Power Op Amp	2-85
HA-4156	Quad General Purpose High Performance Op Amp	2-92
HA-4600/02/05	Quad General Purpose High Performance Op Amps	2-96
HA-4620/22/25	Quad High Slew Rate, Wide Bandwidth Op Amps	2-103
HA-4640-1	Quad High Temperature Operational Amplifier	2-109
HA-4741	Quad General Purpose High Performance Op Amp	2-112
HA-4900/02/05	Quad High Speed Comparators	2-116
HA-5033	High Slew Rate Current Buffer	2-123
HA-5062	Dual Low Power J-FET Op Amp	2-131
HA-5064	Quad Low Power J-FET Op Amp	2-134
HA-5082	Dual General Purpose J-FET Op Amp	2-137
HA-5084	Quad General Purpose J-FET Op Amp	2-140
HA-5100/05	General Purpose High Performance J-FET Op Amps	2-143
HA-5102	Dual General Purpose Low Noise Op Amp	2-149
HA-5104	Quad General Purpose Low Noise Op Amp	2-149
HA-5110/15	High Slew Rate, Wide Bandwidth J-FET Op Amps	2-154
HA-5112	Dual High Slew Rate, Low Noise Op Amp	2-149
HA-5114	Quad High Slew Rate, Low Noise Op Amp	2-149
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HA-5141	Ultra-Low Power Operational Amplifier	2-167
HA-5142	Dual Ultra-Low Power Operational Amplifier	2-167
HA-5144	Quad Ultra-Low Power Operational Amplifier	2-167
Advance HA-5147	High Slew Rate, Precision, Low Noise Op Amp	2-173
HA-5160/62	High Slew Rate, Wide Bandwidth J-FET Op Amps	2-174
HA-5170	J-FET Precision Operational Amplifier	2-181
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HA-5190/95	High Slew Rate, Fast Settling Operational Amplifiers	2-193
HA-23080	Transconductance Amplifier	2-200
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LF147/347	Quad General Purpose J-FET Operational Amplifiers	2-212
LF- 353	Dual General Purpose J-FET Operational Amplifier	2-220
LM118/318	High Slew Rate Operational Amplifiers	2-229
LM143/343	High Voltage Operational Amplifiers	2-236

OPERATIONAL AMPLIFIERS: HIGH SLEW-RATE

	Part Number	Temperature Range	Slew Rate (V/μs)	Band-width Product (MHz)	Full Power Bandwidth (MHz)	Bias Current (nA)	Open Loop Gain (V/mV)	Minimum Gain Stable	Comments	Page
SINGLES	HA-OP37	Mil/Com	17	63	0.3	8	1500	5	Low Noise	2-19
	HA-5147	Mil/Com	35	100	0.5	8	1800	10	Low Noise	2-173
	HA-2620	Mil	35	100	0.6	1	150	5		2-57
	HA-2622	Mil	35	100	0.6	5	150	5		2-57
	HA-2625	Com	35	100	0.6	5	150	5		2-57
	HA-5115	Com	40	50	0.625	0.05	100	10	JFET	2-154
	HA-5110	Mil/Com	50	60	0.625	0.02	150	10	JFET	2-154
	HA-2512	Mil	60	12	1.0	125	15	Unity		2-31
	HA-2515	Com	60	12	1.0	125	15	Unity		2-31
	HA-2510	Mil	65	12	1.0	100	15	Unity		2-31
	LM118	Mil	70	15	1.0	120	15	Unity		2-229
	LM318	Com	70	15	1.0	150	15	Unity		2-229
	HA-5162	Mil/Com	70	100	1.0	0.02	100	10	JFET	2-174
	HA-5160	Mil/Com	120	100	1.0	0.02	150	10	JFET	2-174
	HA-2520	Mil	120	20	2.0	100	15	3		2-35
	HA-2522	Mil	120	20	1.6	125	15	3		2-35
	HA-2525	Com	120	20	1.6	125	15	3		2-35
	HA-5190	Mil	200	150	6.5	5000	30	5		2-193
	HA-5195	Com	200	150	6.5	5000	30	5		2-193
	HA-2541	Mil/Com	300	40	5	15000	15	Unity		2-51
	HA-2542	Mil/Com	350	60	5.5	25000	10	2	Power Output	2-52
	HA-2540	Mil/Ind/Com	400	400	6.0	5000	30	10		2-45
	HA-2539	Mil/Ind/Com	600	600	9.5	5000	30	10		2-39
DUAL	HA-5112	Mil/Com	20	60	0.25	130	250	10	Low Noise	2-149
QUADS	HA-5114	Mil/Com	20	60	0.25	130	250	10	Low Noise	2-149
	HA-2400	Mil	30	40	0.5	50	150	10	Addressable	2-23
	HA-2404	Ind	30	40	0.5	50	150	10	Addressable	2-23
	HA-2405	Com	30	40	0.5	50	150	10	Addressable	2-23

Selection Guide (continued)

OPERATIONAL AMPLIFIERS: WIDE BANDWIDTH

	Part Number	Temperature Range	Gain Band-Width Product (MHz)	Full Power Bandwidth (MHz)	Slew Rate (V/μs)	Bias Current (nA)	Open Loop Gain (V/mV)	Minimum Gain Stable	Comments	Page
SINGLES	HA-2510	Mil	12	1.0	65	100	15	Unity		2-31
	HA-2512	Mil	12	1.0	60	125	15	Unity		2-31
	HA-2515	Com	12	1.0	60	125	15	Unity		2-31
	HA-2600	Mil	12	0.075	7	1	150	Unity		2-53
	HA-2602	Mil	12	0.075	7	15	150	Unity		2-53
	HA-2605	Com	12	0.075	7	5	150	Unity		2-53
	LM118	Mil	15	1.0	70	120	15	Unity		2-229
	LM318	Com	15	1.0	70	150	15	Unity		2-229
	HA-2520	Mil	20	2.0	120	100	15	3		2-35
	HA-2522	Mil	20	1.6	120	125	15	3		2-35
	HA-2525	Com	20	1.6	120	125	15	3		2-35
	HA-2541	Mil/Com	40	5	300	15000	15	Unity		2-51
	HA-2542	Mil/Com	60	5.5	350	25000	10	2	Power Output	2-52
	HA-OP37	Mil/Com	63	0.3	17	8	1500	5	Low Noise	2-19
	HA-5147	Mil/Com	100	0.5	35	8	1800	10	Low Noise	2-173
	HA-2620	Mil	100	0.6	35	1	150	5		2-57
	HA-2622	Mil	100	0.6	35	5	150	5		2-57
	HA-2625	Com	100	0.6	35	5	150	5		2-57
	HA-5160	Mil/Com	100	1.0	120	0.02	150	10	JFET	2-174
	HA-5162	Mil/Com	100	1.0	70	0.02	100	10	JFET	2-174
	HA-5190	Mil	150	6.5	200	5000	30	5		2-193
	HA-5195	Com	150	6.5	200	5000	30	5		2-193
	HA-2540	Mil/Ind/Com	400	6.0	400	5000	30	10		2-45
	HA-2539	Min/Ind/Com	600	9.5	600	5000	30	10		2-39
DUAL	HA-5112	Mil/Com	60	0.25	20	130	250	10	Low Noise	2-149
QUADS	HA-2400	Mil	40	0.5	30	50	150	10	Addressable	2-23
	HA-2404	Ind	40	0.5	30	50	150	10	Addressable	2-23
	HA-2405	Com	40	0.5	30	50	150	10	Addressable	2-23
	HA-5114	Mil/Com	60	0.25	20	130	250	10	Low Noise	2-149

Selection Guide (continued)

OPERATIONAL AMPLIFIERS: PRECISION

Part Number	Temperature Range	Offset Voltage (μV)	Offset Voltage Drift (μV/°C)	Bias Current (nA)	Open Loop Gain (V/mV)	Noise Current (pA/$\sqrt{Hz}$)	Noise Voltage (nV/$\sqrt{Hz}$)	CMRR (dB)	PSRR (dB)	Supply Current (mA)	Comments	Page
HA-5180	Mil/Ind/Com	1000	5	0.0003	1000	0.01	70	110	105	0.8	JFET	2-186
HA-5170	Mil/Ind/Com	100	2	0.02	600	0.01	10	100	105	1.9	JFET	2-181
HA-5180A	Mil/Ind/Com	100	5	0.0003	1000	0.01	70	110	105	0.8	JFET	2-186
HA-OP07C	Com	60	0.4	1	10000	0.14	9.8	120	130	1		2-10
HA-OP07E	Com	10	0.4	1	10000	0.14	9.6	120	130	1		2-10
HA-OP07	Mil	10	0.4	1	10000	0.14	9.6	120	130	1		2-10
HA-OP07A	Mil	10	0.4	1	10000	0.14	9.6	120	130	1		2-10
HA-OP27	Mil/Com	10	0.2	8	1500	0.60	3	120	120	3		2-18
HA-OP37	Mil/Com	10	0.2	8	1500	0.60	3	120	120	3	High Speed	2-18
HA-5147	Mil/Com	10	0.2	8	1800	0.60	3	120	120	3	High Speed	2-173

OPERATIONAL AMPLIFIERS: LOW POWER

	Part Number	Temperature Range	Supply Current* (μA)	Supply Range (V)	Slew Slew Rate (V/μs) At Indicated Supply Current	Gain Band-width Product (kHz) At Indicated Supply Current	Output Swing (V) ± 15V Power Supplies	Offset Voltage (mV)	Comments	Page
SINGLES	HA-5141	Mil/Com	50	+2/+40	1.0	400	0/ +3 (+5V)	0.7		2-167
	HA-5141A	Mil/Com	45	+2/+40	1.5	400	0/ +4 (+5V)	0.5		2-167
DUALS	HA-5062	Mil/Ind/Com	200	± 5/ ± 15	4	1000	± 12	4	JFET	2-131
	HA-5062A	Com	200	± 5/ ± 15	4	1000	± 12	3	JFET	2-131
	HA-5062B	Com	200	± 5/ ± 15	4	1000	± 12	2	JFET	2-131
	HA-5142	MIL/Com	50	+2/ +40	1.0	400	0/ +3 (+5V)	0.7		2-167
	HA-5142A	Mil/Com	45	+2/ +40	1.5	400	0/ +4 (+5V)	0.5		2-167
QUADS	HA-5064	Mil/Ind/Com	200	± 5/ ± 15	4	1000	± 12	4	JFET	2-134
	HA-5064A	Com	200	± 5/ ± 15	4	1000	± 12	3	JFET	2-134
	HA-5064B	Com	200	± 5/ ± 15	4	1000	± 12	2	JFET	2-134
	HA-5144	Mil/Com	50	+2/ +40	1.0	400	0/ +3 (+5V)	0.7		2-167
	HA-5144A	Mil/Com	45	+2/ +40	1.0	400	0/ +3 (+5V)	0.7		2-167

*Per Op Amp

Selection Guide (continued)

OPERATIONAL AMPLIFIERS: GENERAL PURPOSE

	Part Number	Temperature Range	Gain Bandwidth Product (MHz)	Slew Rate (V/μs)	Offset Voltage (mV)	Bias Current (nA)	Noise Voltage (nV/√Hz)	Open Loop Gain (V/mV)	Common Mode Range (V) ±15V Power Supplies	Supply Current (mA)	Comments	Page
SINGLES	HA-2600	Mil	12	7	0.5	1	16	150	±11	3		2-53
	HA-2602	Mil	12	7	3	15	16	150	±11	3		2-53
	HA-2605	Com	12	7	3	5	16	150	±11	3		2-53
DUALS	HA-5082	Mil/Com	4	15	4	0.03	20	200	±12	3.5	JFET	2-137
	HA-5082A	Com	4	15	3	0.03	20	200	±12	3.5	JFET	2-137
	HA-5082B	Com	4	15	2	0.03	20	200	±12	3.5	JFET	2-137
	HA-5102	Mil/Com	8	3	0.5	130	4.3	250	±12	3	Low Noise	2-149
QUADS	HA-4741	Mil/Com	3.5	1.6	1	60	9	50	±12	7		2-112
	HA-5084	Mil/Com	4	15	5	0.03	20	25	±10	7.2	JFET	2-140
	HA-5084A	Com	4	15	4	0.03	20	50	±10	7.2	JFET	2-140
	HA-5084B	Com	4	15	2	0.03	20	50	±10	7.2	JFET	2-140
	HA-5104	Mil/Com	8	3	0.5	130	4.3	250	±12	3	Low Noise	2-149
	HA-2400	Mil	40	30	4	50	20	150	±9	4.8	Addressable	2-23
	HA-2404	Ind	40	30	4	50	20	150	±9	4.8	Addressable	2-23
	HA-2405	Com	40	30	4	50	20	150	±9	4.8	Addressable	2-23

OPERATIONAL AMPLIFIERS: HIGH VOLTAGE

Part Number	Features	Applications	Page
HA-2640 HA-2645	• Slew Rate 1V/μs • Bandwidth: 4MHz • Input Offset Voltage: 4mV • Offset Current: 5nA • Output Voltage Swing: ±35V • Input Voltage Swing ±35V • Supply Range: ±10V to ±40V • Output overload protection	• Industrial control systems • Power supplies • High voltage regulators • Resolver excitation • Signal conditioning	2-65

Selection Guide (continued)

OPERATIONAL AMPLIFIERS: ADDRESSABLE

Part Number	Features	Applications	Page
HA-2400 HA-2404 HA-2405	• Four Channels Addressable • High Slew Rate 30V/μs • Wide Gain Bandwidth • Products: 40MHz • High Gain: 150K • TTL Compatible	• Signal selection/multiplexing • Variable gain stages • Oscillators • Filters • Comparators • Integrators	2-23

OPERATIONAL AMPLIFIERS: CURRENT BUFFERS

Part Number	Features	Applications	Page
HA-5033	• Differential Phase Error: 0.1° • Differential Gain Error: 0.1% • High Slew Rate: 1300V/μs • Wide Power Bandwidth: 80MHz • Fast Rise Time: 3ns • Wide Power Supply Range: ±5/±16V	• Video Buffers • HF Buffers • Op Amp Isolation Buffers • High Speed Line Drivers • Impedance matching	2-123
HA-2542	Also see HA-2542.		

COMPARATORS

Part Number	Features	Applications	Page
HA-4900 HA-4902 HA-4905	• Fast Response Time: 130ns • Low Offset Voltage: 2mV • Low Offset Current: 10nA • Single or Dual Supply • Analog and logic supplies separated for easier interface and noise immunity	• Threshold Detectors • Zero Crossing Detectors • Window Detectors • Interface • Oscillators	2-116

CONTROL FUNCTIONS

INDUCTION MOTOR ENERGY SAVER

Part Number	Features	Applications	Page
HV-1000 HV-1000A NEW	• HV-1000: Operates directly off 110 VAC line • HV-1000A: Operates directly off 220 VAC line • No Power Supply Required • Provides Power Savings from 10% to 50% for motors with light or variable loads. • SCR output triggers Triac directly • Load Anticipator senses shock loads and responds instantly with full power. • Withstands line surges up to 3500V. • Allows motor to run cooler and quieter. • Can be mounted inside motor. • Requires only 3 resistors, 3 capacitors and one Triac to assemble complete controller.	• Power Tools • Disk Drives • Heat Pumps • Presses • Conveyors • Any application where a single phase motor will occasionally drive at less than its rated load.	2-207

TRIPLE CURRENT SENSE WITH LATCH

Part Number	Features	Applications	Page
HA-23551	• Current sensing with precision threshold voltage • Large Common Mode Voltage Range: 3.5V to 40V. • Switching Delay: 190ns. • Open Collector Output • TTL Compatible Reset	• Solenoid Drivers • Switching Power Supplies • Stepper Motor Drivers • Temperature Control	2-203

VOLTAGE REFERENCES

Part Number	Features	Applications	Page
HA-1608	• Monolithic • Accuracy: 10V ± 0.01V • Total Output Error: ± 1/4 LSB (8 Bits) • Low Noise: 20 μV_{pp} • Wide Input Range: 12V to 30V • Short-circuit Protected • Adjustable Output	• Digital to Analog Converters, External Reference • Analog to Digital Converters, External Reference • Data Acquisition Systems • Instrumentation	2-20

Operational Amplifiers Glossary

AVERAGE INPUT OFFSET CURRENT DRIFT ($\Delta IOS/\Delta T$) - The ratio of the change in the offset current to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT ($\Delta V_{OS}/\Delta T$) - The ratio of the change in the offset voltage to the change in temperature producing it.

BANDWIDTH (BW) - That frequency at which the gain of the amplifier is 3dB below its low frequency value.

CHANNEL SEPARATION - The ratio of the input of a driven amplifier to the output of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the two input voltages.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifer to cease operating properly.

COMMON MODE REJECTION RATIO (C_{MRR}) - The ratio of the differential voltage gain to the common mode voltage gain.

Note: This is measured by determining the ratio of the change in input common-mode voltage to the resulting change in offset voltage.

COMMON MODE RESISTANCE (r_{ic}) - The value of resistance looking into both inputs tied together.

DIFFERENTIAL INPUT RESISTANCE (r_{id}) - The value of resistance between two ungrounded inputs.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full size undistorted sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH PRODUCT - The product of the gain and bandwidth at some specified frequency.

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT CAPACITANCE (C_{IN}) - The capacitance of either input with the other grounded.

INPUT NOISE CURRENT (i_n) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero voltage.

INPUT OFFSET VOLTAGE (V_{OS}) - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_n) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

INPUT RESISTANCE (R_{IN}) - The ratio of the change in input voltage to the change in input current at either terminal with the other grounded.

LARGE SIGNAL VOLTAGE GAIN (A_v) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The maximum output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (VOUT) - The peak to peak output voltage swing, referred to ground, that can be obtained without clipping under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_r) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small voltage pulse.

SETTLING TIME - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

HARRIS

HA-OP07

Precision Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE — 25 μV
- LOW OFFSET VOLTAGE DRIFT — 0.4 μV/^{o}C
- LOW NOISE — 9nV/$\sqrt{Hz}$
- OPEN LOOP GAIN — 10^7
- BANDWIDTH (UNITY GAIN) — 2.5MHz
- ALL BIPOLAR CONSTRUCTION
- PIN CONFIGURATION SAME AS OP-07

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The HA-OP07 is a precision operational amplifier manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25 μV (Max.) input offset voltage and 0.4 μV/^{o}C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

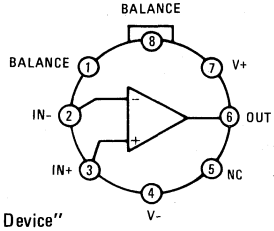
These features coupled with 120dB CMRR and PSRR make the HA-OP07 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjuction with 2.5MHz bandwidth and 0.8V/ μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

The HA-OP07 is packaged in an 8 pin (TO-99) can, an 8 lead Cerdip, an 8 pin epoxy DIP and is compatible with OP-07 configuration.

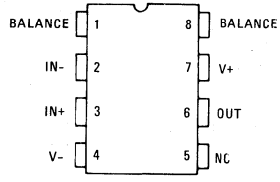
HA-OP07/HA-OP07A are specified for -55^{o}C to +125^{o}C operation while the HA-OP07C/HA-OP07E operate from 0^{o}C to +75^{o}C.

PINOUTS

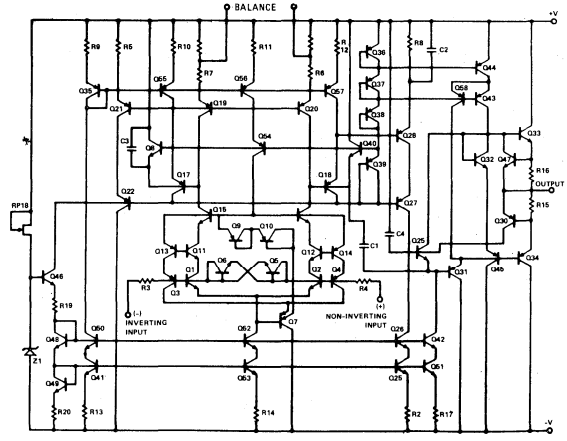
TOP VIEWS



"Caution:
ESD Sensitive Device"



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±22V	Storage Temperature Range	
Internal Power Dissipation (Note 2)	500mW	J and Z Packages	-65°C to +150°C
Differential Input Voltage	±15V		
Input Voltage	±V Supplies	Operating Temperature Range	
Output Short Circuit Duration	Indefinite	OP-07A, OP-07	-55°C to +125°C
		OP-07E, OP-07C	0°C to +75°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07A			HA-OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	10	25	–	10	75	μV
I_{OS}	Input Offset Current				2.0			2.8	nA
I_B	Input Bias Current		–	±1.0	±2.0	–	±1.0	±3.0	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz	–	–	0.6	–	–	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	13.0 10.0 9.6	18.0 13.0 11.0	– – –	13.0 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
I_{np-p}	Input Noise Current	0.1Hz to 10Hz	–	15.0	30	–	15.0	30	pA_{p-p}
I_n	Input Noise Current Density	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.4 0.17 0.14	0.80 0.23 0.17	– – –	0.4 0.17 0.14	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance - Differential Mode		20	30	–	20	30	–	MΩ
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	120	–	110	120	–	dB
PSRR	Power Supply Rejection Ratio	V_S ±3V to ±18V	100	130	–	100	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	140	–	120	140	–	dB
V_O	Output Voltage Swing	R_L = 2kΩ R_L = 600Ω	±12 ±10	±12	–	±12 ±10	±12	–	V
SR	Slewing Rate	$R_L \geq 2k\Omega$	0.5	0.8	–	0.5	0.8	–	V/μs
BW	Closed Loop Bandwidth	A_{VCL} = +1.0	0.6	2.5	–	0.6	2.5	–	MHz
R_O	Open Loop Output Resistance	f = 100Hz	–	45	–	–	45	–	Ω
I_{CC}	Supply Current	No Load	–	1.0	1.3	–	1.0	1.7	mA
P_D	Power Consumption	V_{CC} = ±15V V_{CC} = ±3V		27 5.4	35 6.0		27 5.4	35 6.0	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07A			HA-OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	50	60	–	60	130	μV
TCV_{OS}	Avg. Input Offset Voltage Drift Without External Trim		–	0.4	0.6	–	0.4	1.3	μV/°C
I_{OS}	Input Offset Current		–	–	4.0	–	–	5.6	nA
TCI_{OS}	Avg. Input Offset Current Drift		–	20	40	–	20	40	pA/°C
I_B	Input Bias Current		–	–	±4.0	–	–	±6.0	nA
TCI_B	Avg. Input Bias Current Drift		–	20	40	–	20	40	pA/°C
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	–	–	120	–	–	dB
V_O	Output Voltage Swing	R_L = 600Ω R_L = 2kΩ	±10 ±12	–	–	±10 ±12	–	–	V

NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2k\Omega$. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^oC$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07E			HA-OP07C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	10	75	–	60	150	μV
I_{OS}	Input Offset Current		–	–	3.8	–	–	6.0	nA
I_B	Input Bias Current		–	±1.0	±4.0	–	±1.0	±7.0	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz	–	–	0.6	–	–	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz	– – –	13.0 10.0 9.6	18.0 13.0 11.0	– – –	13.0 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
I_{np-p}	Input Noise Current	0.1Hz to 10Hz	–	15.0	30	–	15.0	35	pA_{p-p}
I_n	Input Noise Current Density	f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz	– – –	0.4 0.17 0.14	0.80 0.23 0.17	– – –	0.4 0.17 0.14	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance - Differential Mode		20	30	–	20	30	–	MΩ
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	V_S ±3V to ±18V	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	140	–	100	140	–	dB
V_O	Output Voltage Swing	R_L = 2KΩ R_L = 600Ω	±12 ±10	±12	–	±11.5 ±10	±12	–	V
SR	Slewing Rate	$R_L \geq 2k\Omega$	0.5	0.8	–	0.5	0.8	–	$V/\mu s$
BW	Closed Loop Bandwidth	A_{VCL} = +1.0	0.6	2.5	–	0.6	2.5	–	MHz
R_O	Open Loop Output Resistance	f = 100Hz	–	45	–	–	45	–	Ω
I_{CC}	Supply Current	No Load	–	1.0	1.3	–	1.0	1.7	mA
P_D	Power Consumption	V_{CC} = ±15V V_{CC} = ±3V			35 6.0			50 8	mW

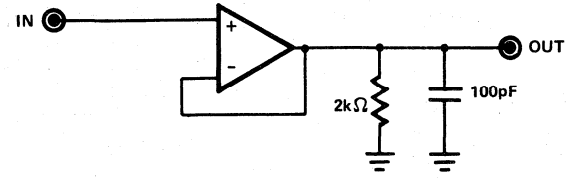
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^oC \leq T_A \leq +70^oC$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07E			HA-OP07C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	50	130	–	50	250	μV
TCV_{OS}	Avg. Input Offset Voltage Drift Without External Trim		–	0.4	0.6	–	0.4	1.3	$\mu V/^oC$
I_{OS}	Input Offset Current		–	–	5.3	–	–	8.0	nA
TCI_{OS}	Avg. Input Offset Current Drift		–	20	40	–	20	50	$pA/^oC$
I_B	Input Bias Current		–	–	5.5	–	–	9.0	nA
TCI_B	Avg. Input Bias Current Drift		–	20	40	–	20	50	$pA/^oC$
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	–	–	100	–	–	dB
V_O	Output Voltage Swing	R_L = 600Ω R_L = 2kΩ	±10 ±12	–	–	±10 ±12	–	–	V

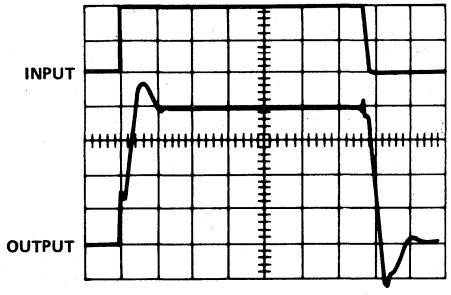
NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2k\Omega$. Gain dB = $20 \log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV

TEST CIRCUITS

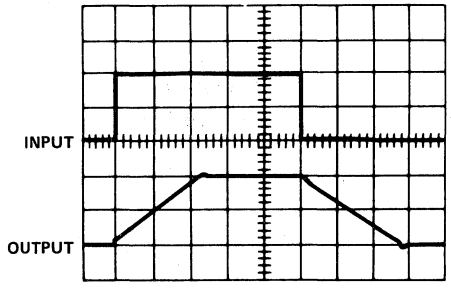
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



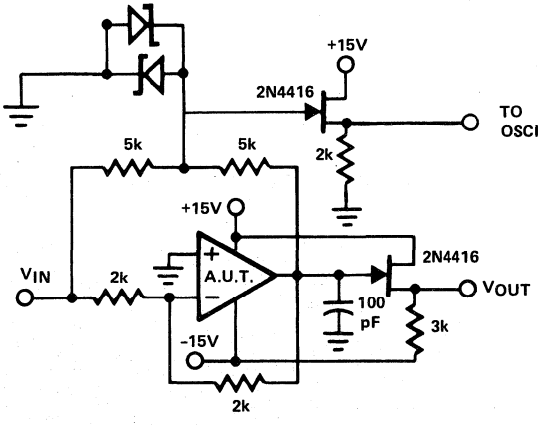
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)

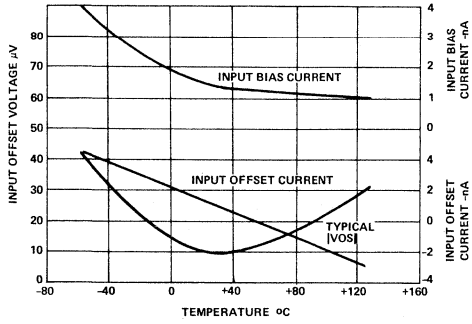


SETTLING TIME CIRCUIT

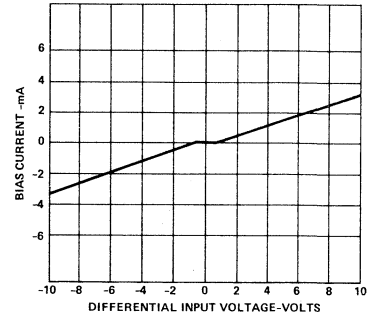


- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

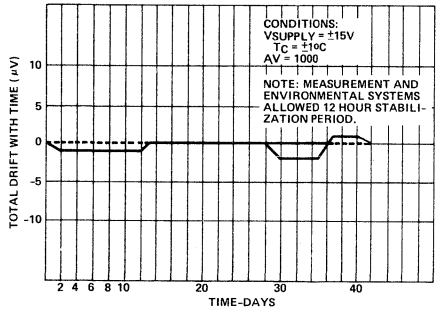
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



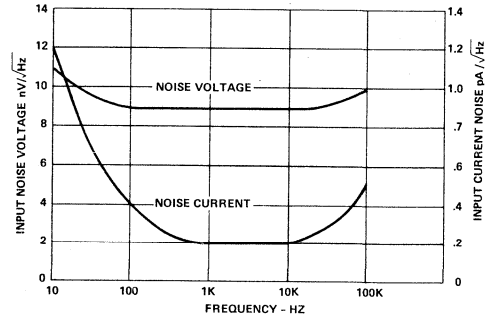
INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE



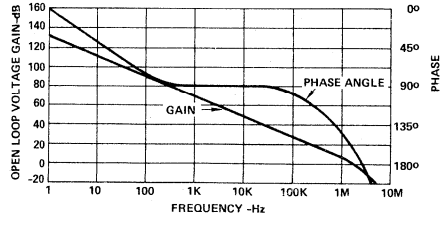
OFFSET VOLTAGE STABILITY VS. TIME



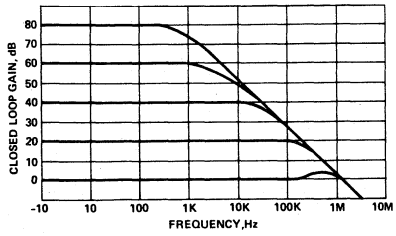
INPUT - NOISE VS. FREQUENCY



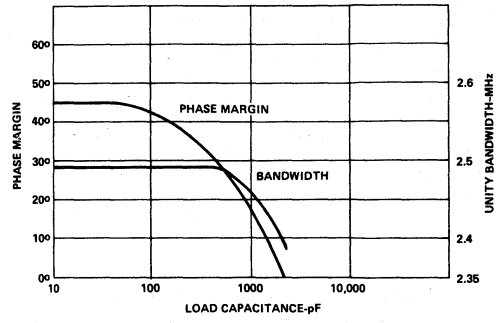
OPEN LOOP FREQUENCY RESPONSE



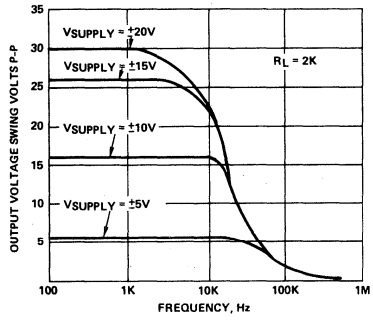
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



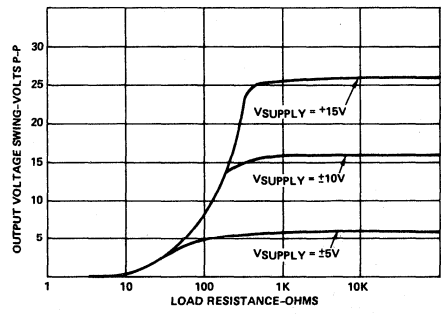
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



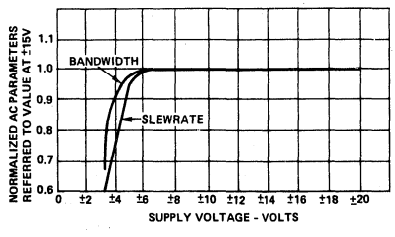
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE

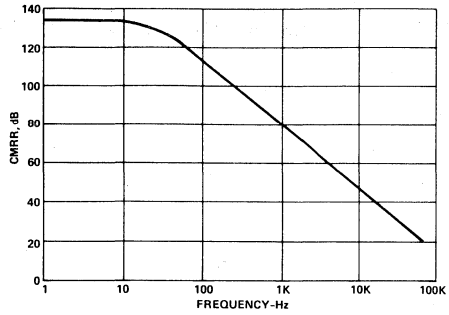


NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE

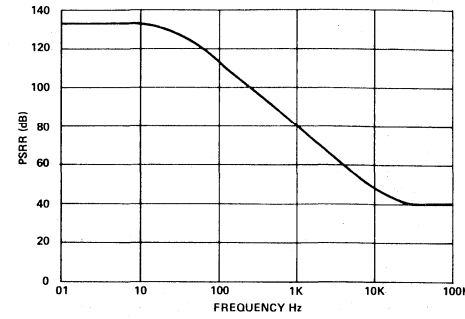


PERFORMANCE CURVES (Continued)

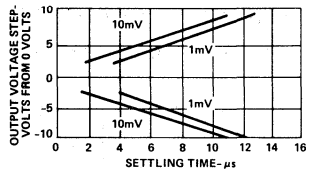
CMRR VS. FREQUENCY



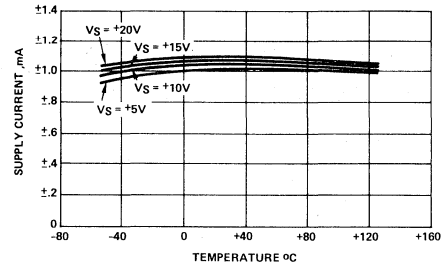
PSRR VS. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



APPLYING THE HA-OP07 OPERATIONAL AMPLIFIERS

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces, and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings, and shield drivers are recommended for the most critical applications.

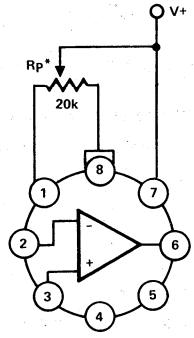
3. When driving large capacitive loads (> 500pF), as small value resistor (≈50Ω) should be connected in series with the output and inside the feedback loop.

4. OFFSET VOLTAGE ADJUSTMENT: A 20 KΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10KΩ, 50KΩ, and 100KΩ may be used. The minimum adjustment range for given values is ±2mV.

5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

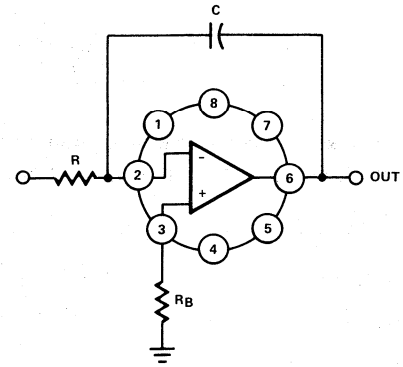
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.

OFFSET NULLING CONNECTIONS



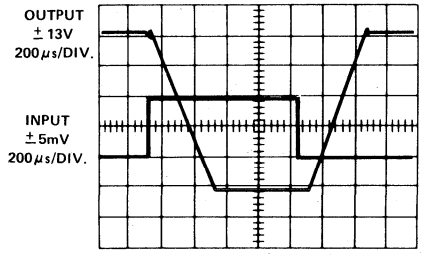
*Although Rp is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

PRECISION INTEGRATOR

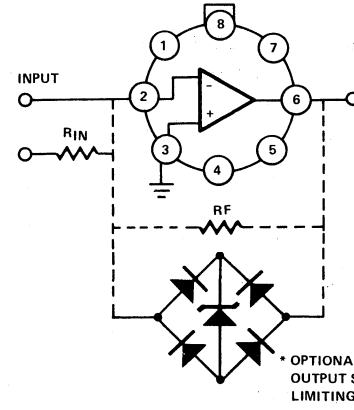


The excellent input and gain characteristics of HA-OP07 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-OP07, virtually nullifies the need for more expensive chopper-type amplifiers.

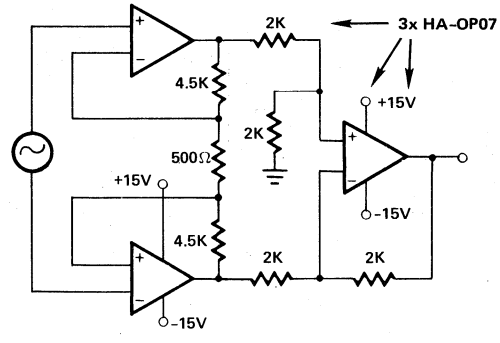
ZERO CROSSING DETECTOR



Low V_{OS} coupled with high open loop Gain, high CMRR, and high PSRR make HA-OP07 ideally suited for precision detector applications.



PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



HARRIS

ADVANCE

HA-OP27

Ultra-Low Noise, Precision Operational Amplifiers

FEATURES

- LOW NOISE — 3nV/$\sqrt{Hz}$
- LOW DRIFT — 0.2 μV/^{o}C
- LOW V_{OS} — 10 μV
- HIGH GAIN — 1.5 x 10^{6}
- HIGH CMRR/PSRR — 120dB
- WIDEBAND — 8MHz

APPLICATIONS

- LOW LEVEL TRANSDUCER AMPLIFIERS
- PRECISION SUMMING AMPLIFIERS
- AUDIO PREAMPLIFIERS
- INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The HA-OP27 is a "State-of-the-Art" low noise operational amplifier offering an exceptional blend of DC and dynamic specifications. Through advanced processing techniques, this design offers a 3.8nV/$\sqrt{Hz}$ maximum noise value at 1kHz while combining the outstanding qualities of precision and wideband amplifiers.

Laser trimming is employed to precisely adjust the input stage for 10 μV offset voltage while stabilizing TC V_{OS} to 0.2 μV/^{o}C without affecting the 8MHz bandwidth or the 2.8V/μs slew rate. True precision is further enhanced with features such as Avol above 1.5m, CMR or $\pm$ 11V, and CMRR/PSRR exceeding 120dB.

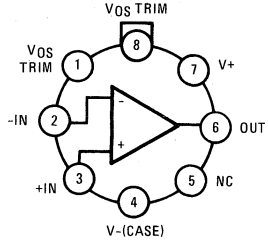
Additional qualities include a modest supply current requirement of 3mA and ease of use through on chip compensation for unity gain stability.

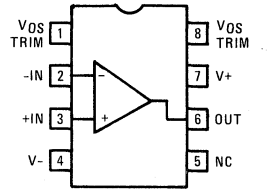
This ideal merging of features makes the HA-OP27 an unparalleled selection for low level signal transducer applications. Additionally, the HA-OP27 is ideally suited for precision summers, audio preamplifiers, stable integrators, and precision threshold detectors.

The HA-OP27 can also be used as a design enhancement by directly replacing the 725, OP06, OP07 and OP05.

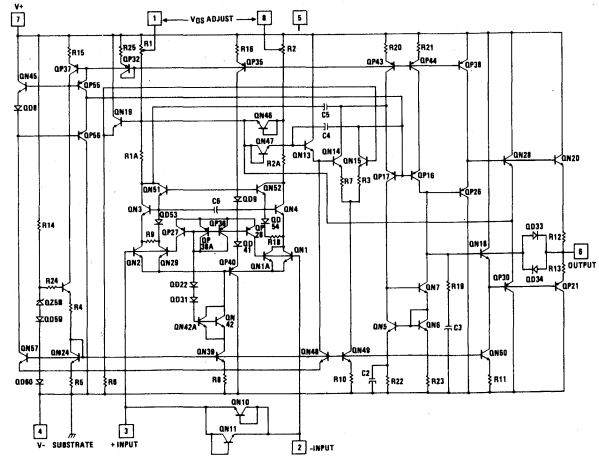
PINOUTS

TOP VIEWS





SCHEMATIC



HARRIS

ADVANCE

HA-OP37

Ultra-Low Noise, Precision, High-Speed Operational Amplifier

FEATURES

- LOW NOISE — 3nV/$\sqrt{Hz}$ at 1kHz
- LOW DRIFT — 0.2 μV/°C
- LOW V_{OS} — 10 μV
- HIGH GAIN — 1.5 x 10^6
- HIGH CMRR/PSRR — 120dB
- FAST — 17V/μs

APPLICATIONS

- LOW LEVEL TRANSDUCER AMPLIFIERS
- RIAA PHONO PREAMPLIFIERS
- AUDIO PREAMPLIFIERS
- PRECISION THRESHOLD DETECTORS
- SIGNAL CONDITIONERS

DESCRIPTION

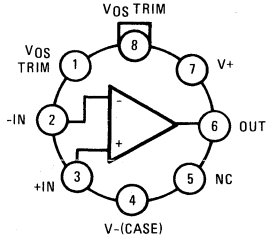
The HA-OP37 operational amplifier truly represents a missing link between precision instrumentation and high speed performances. This device utilizes an innovative design complimented by advanced processing techniques to offer an array of exceptional AC and DC characteristics. The HA-OP37 features include low noise (3nV/$\sqrt{Hz}$), low V_{OS} (10 μV typical), high gain (1.8V/μV), and a fast 17V/μs slew rate.

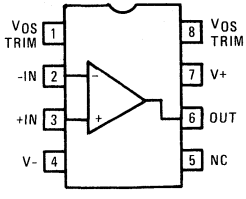
In addition, this amplifier offers exceptional gain bandwidth (63MHz) and very high CMRR/PSRR (120dB). This combination of features makes the HA-OP37 an excellent choice for all low noise, precision amplifier applications requiring gains greater than 5. Applications such as RIAA phono preamplifiers, NAB Equalization circuits, and high speed or wideband signal conditions represent just a few of the many applications which can utilize the outstanding features of the HA-OP37.

The HA-OP37 can also be used as an enhancement for existing designs by directly replacing 725, OP05, OP06 and OP07 in gains greater than 5.

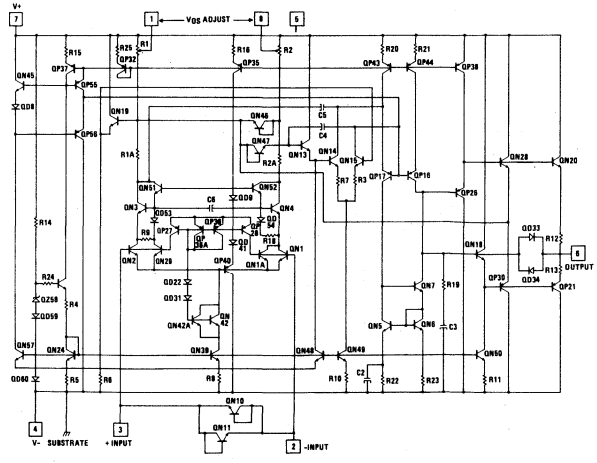
PINOUTS

TOP VIEWS





SCHEMATIC



HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ±1/4 LSB
- LOW NOISE $20\mu V_{p-p}$
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408; AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

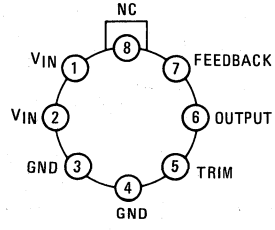
HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

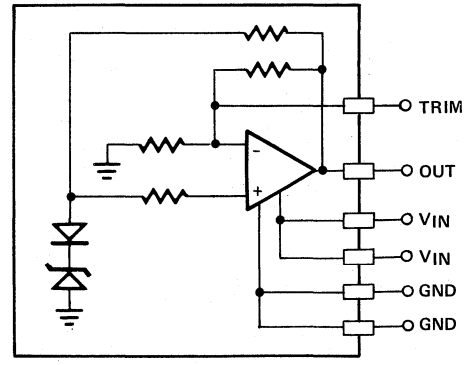
HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

PINOUT

TOP VIEW



FUNCTIONAL SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	TYP	MAX	HA-1608-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, EN 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ±0.1%	25°C		2.5			2.5		μs
to ±0.01%	25°C		5			5		
Warm-up Time (to ±0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

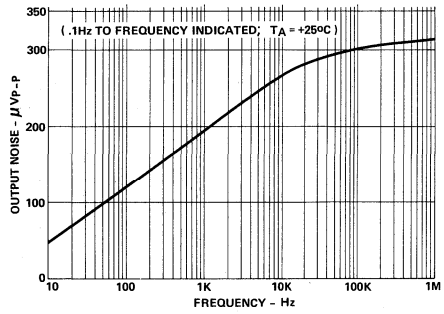
2. The specified electrical characteristics apply to suggested hook-up only.

DEFINITIONS

1. Output Noise Voltage - the output noise voltage in a specified frequency band.
2. Quiescent Current, I_Q - the current required from the supply to operate the device at no load condition after the device is warmed-up.
3. Output Voltage Error Total - Includes effects of Noise Voltage, Line Regulation, and ΔV_0TC relative to 8-bit (10V output) resolution where: 1 LSB = one part in 256 or 39mV for a +10V output.
4. Line Regulation (%/V) - the ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_0/10V) \times 100]/\Delta V_{IN}$.
5. Load Regulation (%/mA) - the ratio of the change in output voltage to the change in load current producing it; load regulation (%/mA) = $[(\Delta V_0/10V) \times 100]/\Delta mA$.
6. Dynamic Load Settling Time - the time required for the output to settle to within the specified error band for a change in the load current of 1mA.

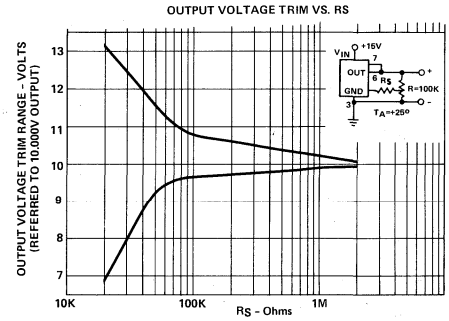
PERFORMANCE CURVES

OUTPUT WIDEBAND NOISE VS. BANDWIDTH

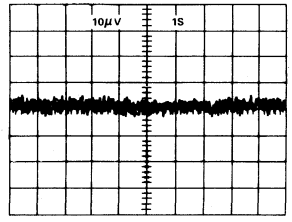


OUTPUT WIDEBAND NOISE VS. BANDWIDTH

OUTPUT VOLTAGE TRIM VS. RS



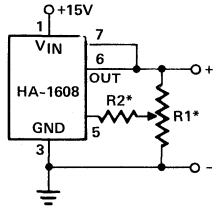
OUTPUT VOLTAGE TRIM VS. R_S



OUTPUT NOISE (0.1Hz TO 10Hz)

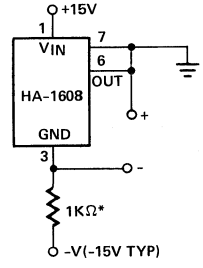
APPLICATIONS

TYPICAL HOOK-UP WITH OUTPUT TRIM



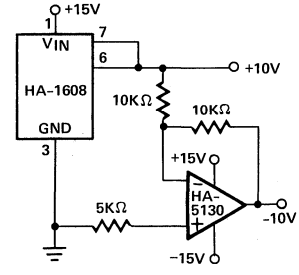
*NOTE: R_1 potentiometer value can be 10K to 100K R_2 can range from 10K to 2M .

NEGATIVE 10 VOLT REFERENCE



*NOTE: The value of R may reduce the output current available to less than that specified on the data sheet.

±10V REFERENCE



HARRIS

HA-2400/2404/2405

PRAM Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

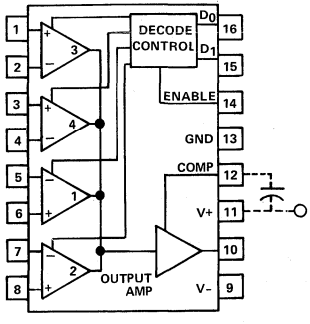
HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/ μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

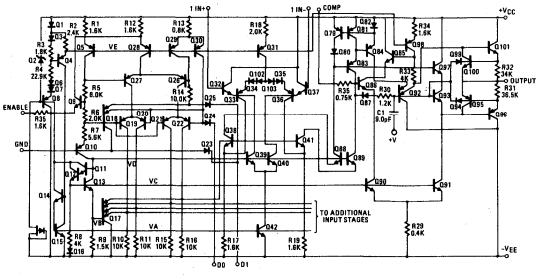


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	-0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected ($I_{SC} \leq \pm 33mA$)		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T^A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

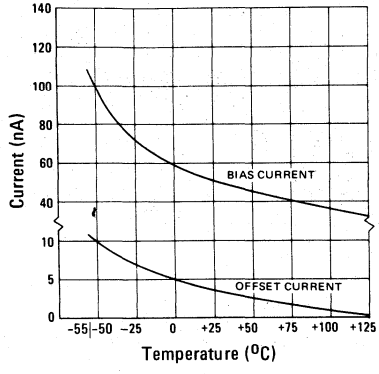
PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	HA-2400/HA-2404 LIMITS TYP.	HA-2400/HA-2404 LIMITS MAX.	HA-2405 LIMITS MIN.	HA-2405 LIMITS TYP.	HA-2405 LIMITS MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	9		4	9	mV
	Full			11			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C	20	40		20	40		MHz
(Note 4)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C	200	500		200	500		kHz
(Notes 4,5)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/μs
(Notes 4,7)	+25°C	6	8		6	8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5	2.5		1.5	2.5	μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full		1	1.5		1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak to peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10VDC$
11. $V_{SUPP} = \pm 10VDC$ to $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C.

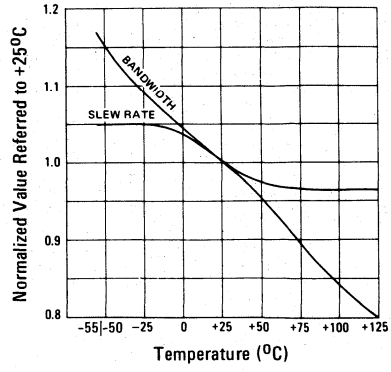
CHARACTERISTIC CURVES

V+ = +15V D. C., V- = -15V D. C., T_A = 25°C unless otherwise stated.

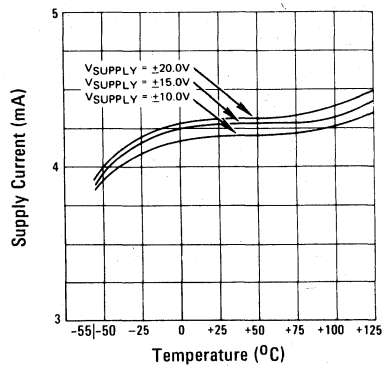
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



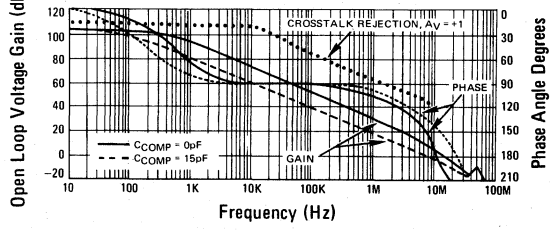
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



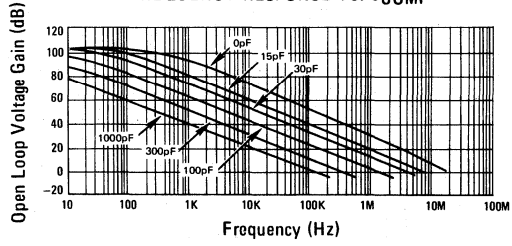
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



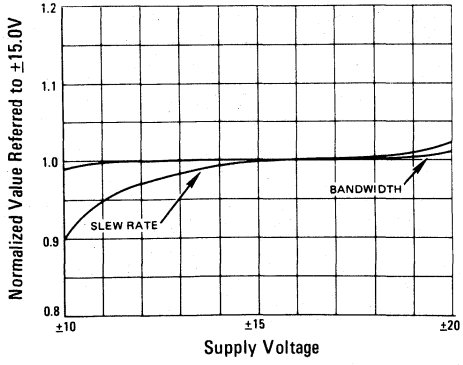
OPEN LOOP FREQUENCY AND PHASE RESPONSE



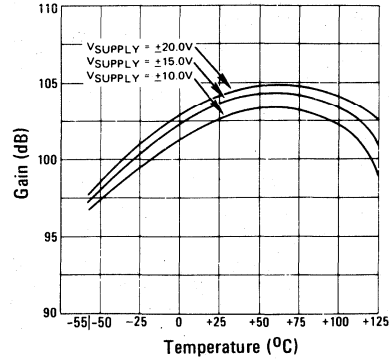
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE

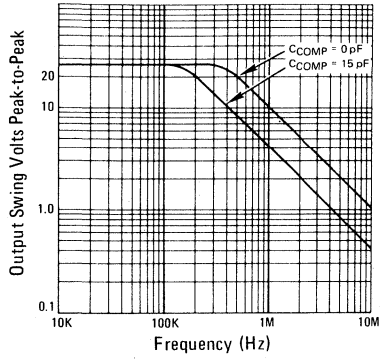


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

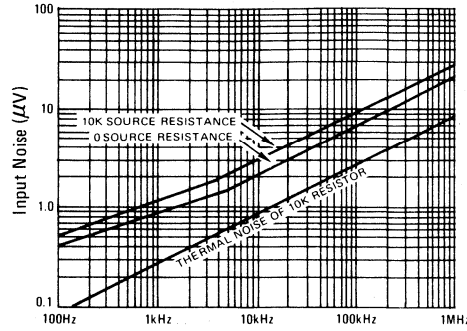


CHARACTERISTIC CURVES (continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

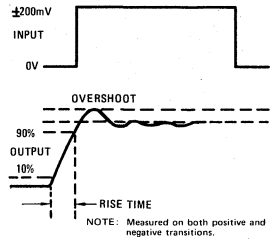


EQUIVALENT INPUT NOISE VS. BANDWIDTH

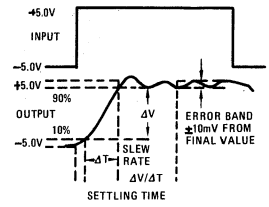


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

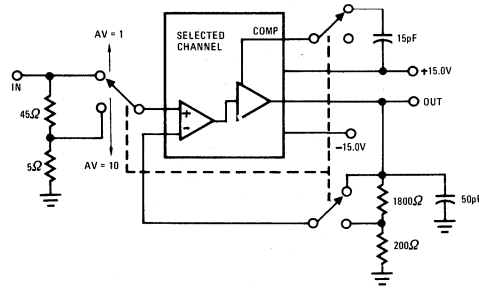
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

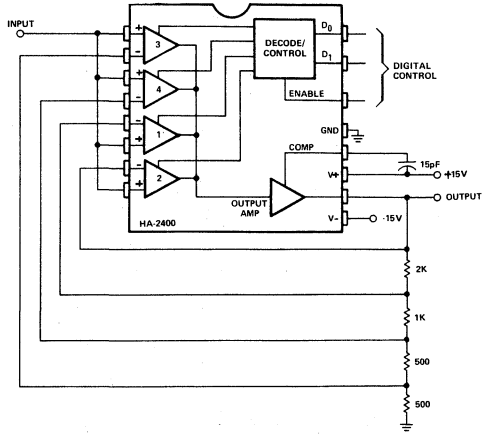


SLEW RATE AND TRANSIENT RESPONSE

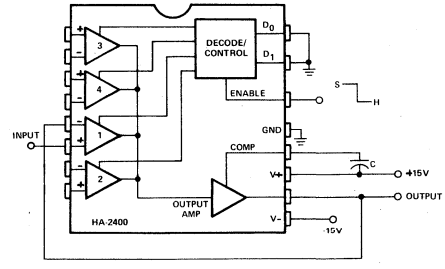


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A
$I_2 \approx 200 \times 10^{-9}$ A @ +25°C
$\approx 600 \times 10^{-9}$ A @ -55°C
$\approx 100 \times 10^{-9}$ A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

HARRIS

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 30V/μS
- FAST SETTLING — 330ns
- WIDE POWER BANDWIDTH — 500kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 50 MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

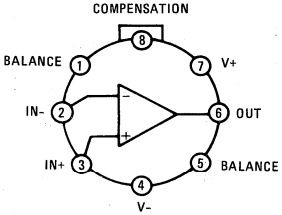
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

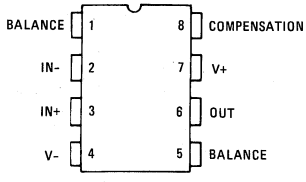
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

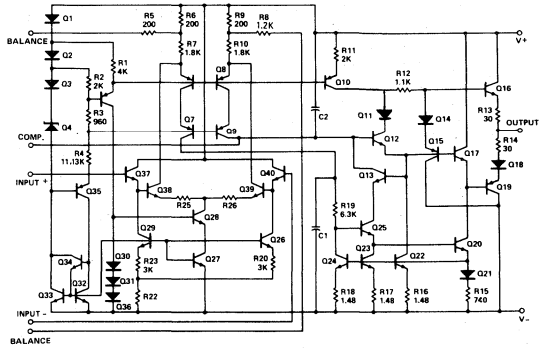
HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUTS

TOP VIEWS







SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±15.0V	HA-2500/2502	$-55^{o}C \leq T_A \leq +125^{o}C$
Peak Output Current	50mA	HA-2505	$0^{o}C \leq T_A \leq +75^{o}C$
Internal Power Dissipation	300mW	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

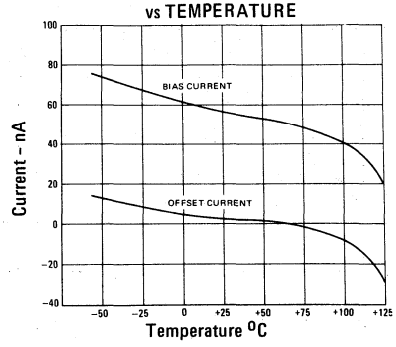
PARAMETER	TEMP.	HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISITCS											
Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARA.'S											
Large Signal Voltage Gain (Note 1, 4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1, 5, 8 & 12)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARA.'S											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms Page 2-31.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

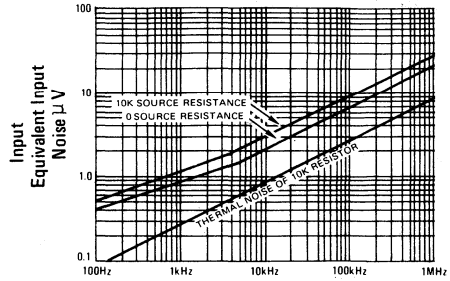
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

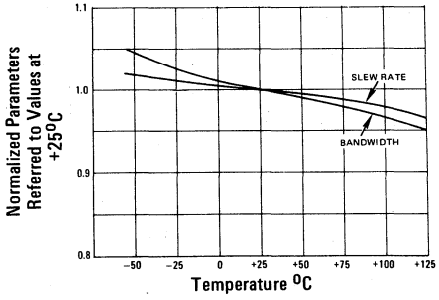
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



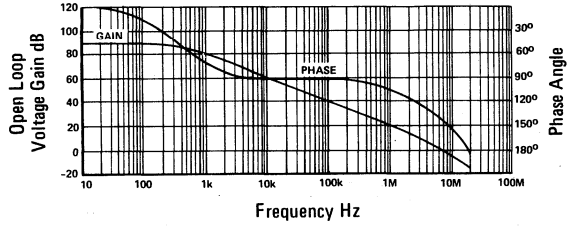
EQUIVALENT INPUT NOISE vs BANDWIDTH



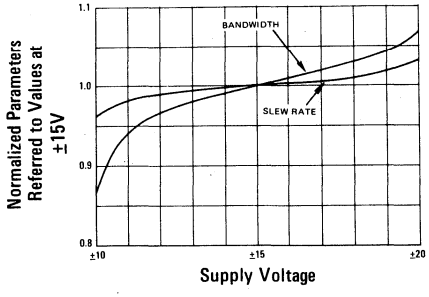
NORMALIZED AC PARAMETERS vs TEMPERATURE



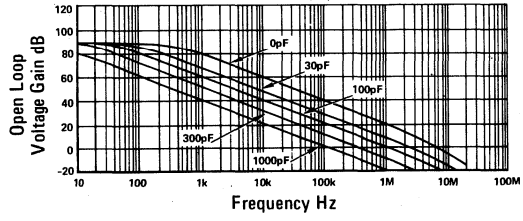
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

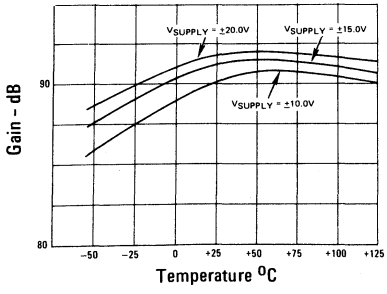


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

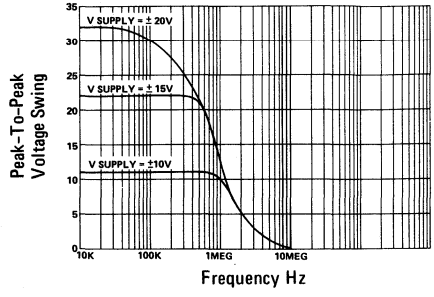


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

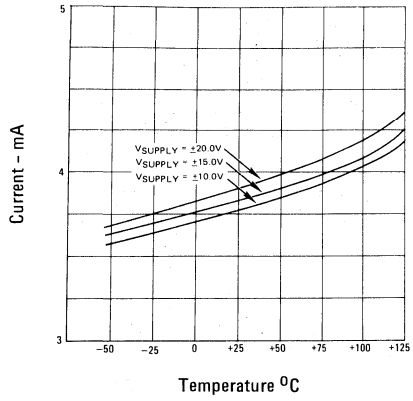
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



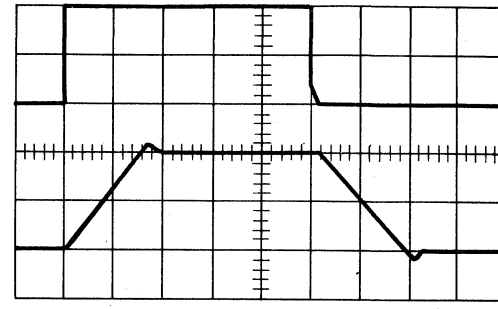
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



POWER SUPPLY CURRENT
vs TEMPERATURE



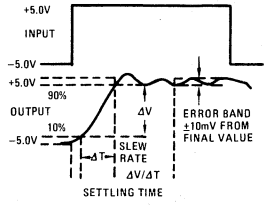
VOLTAGE FOLLOWER PULSE RESPONSE



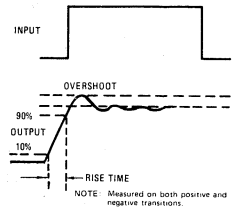
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

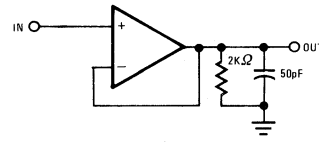
SLEW RATE AND
SETTLING TIME



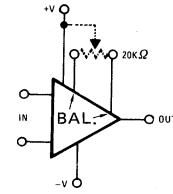
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
VOS ADJUSTMENT



HARRIS

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

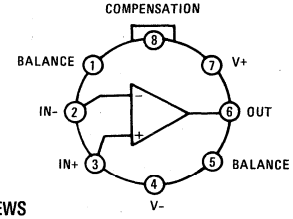
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

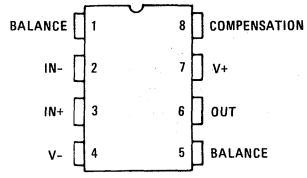
The $\pm$60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

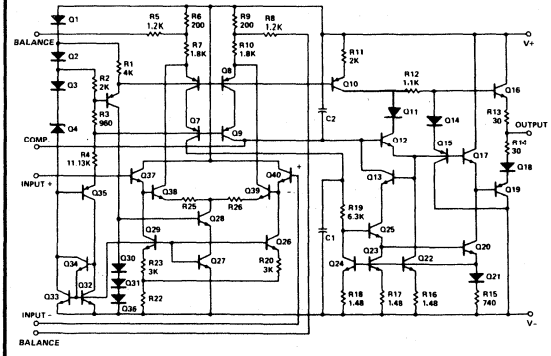
PINOUTS

TOP VIEWS





SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±15.0V	HA-2510/2512	$-55^{o}C \leq T_A \leq +125^{o}C$
Peak Output Current	50mA	HA-2515	$0^{o}C \leq T_A \leq +75^{o}C$
Internal Power Dissipation	300mW	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

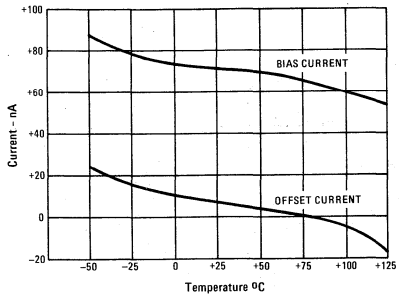
PARAMETER	TEMP.	HA-2510 -55°C to +125°C			HA-2512 -55°C to +125°C			HA-2515 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISITCS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARA.'S											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARA.'S											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms Page 2-35.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using: FPBW = S. R./$2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

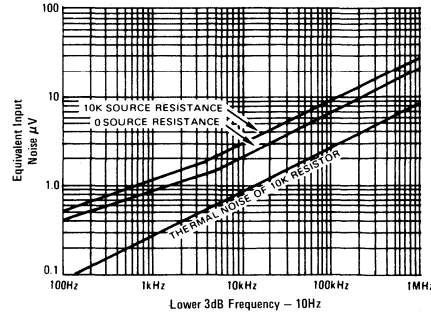
PERFORMANCE CURVES

V+ = 15V D. C., T_A = 25°C unless otherwise stated.

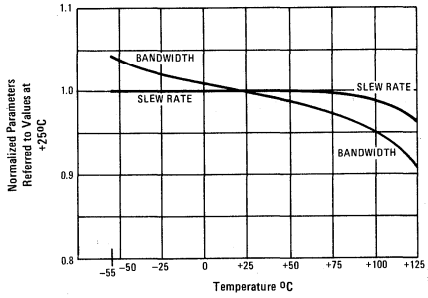
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



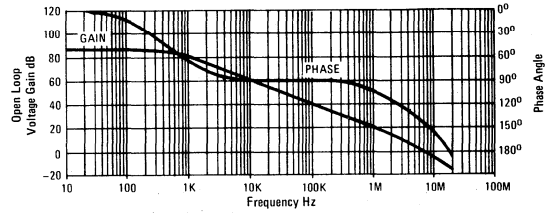
EQUIVALENT INPUT NOISE vs. BANDWIDTH



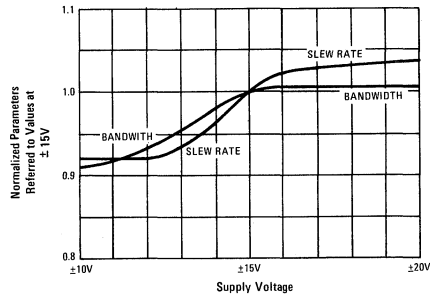
NORMALIZED AC PARAMETERS vs. TEMPERATURE



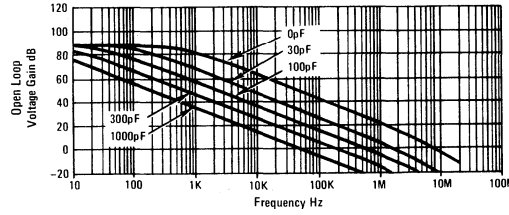
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

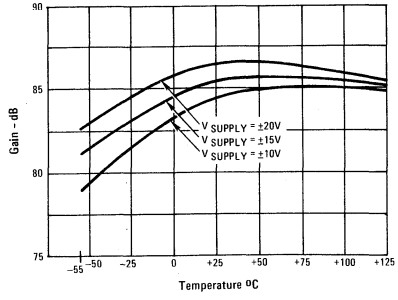


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

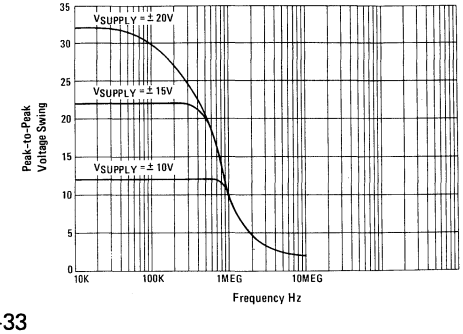


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

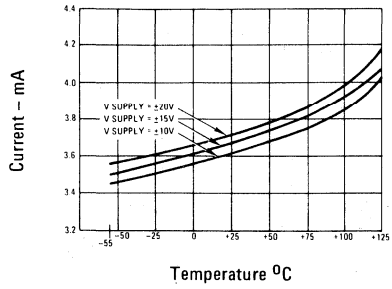


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

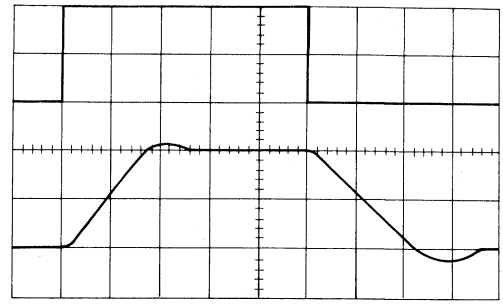


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



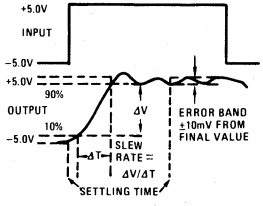
VOLTAGE FOLLOWER PULSE RESPONSE



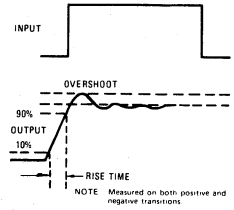
R_L = 2K Ω , C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
T_A = +25°C, V_S = ±15.0V

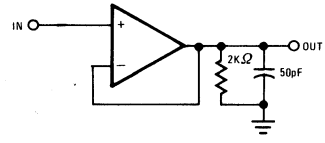
SLEW RATE AND
SETTLING TIME



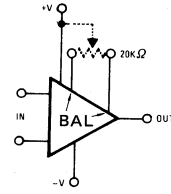
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
VOS ADJUSTMENT



HARRIS

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 200ns
- WIDE POWER BANDWIDTH — 2,000kHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

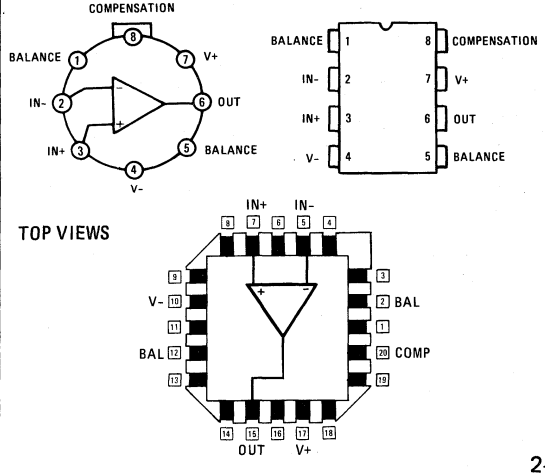
DESCRIPTION

HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

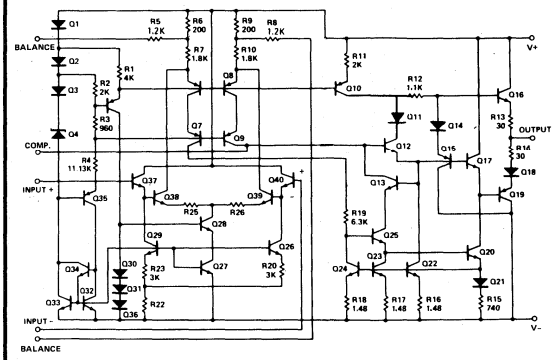
120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

PINOUTS



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Ranges:	
Differential Input Voltage	± 15.0V	HA-2520/HA-2522	$-55^oC \leq T_A \leq +125^oC$
Peak Output Current	50mA	HA-2525	$0^oC \leq T_A \leq +75^oC$
Internal Power Dissipation	300mW	Storage Temperature Range:	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS $V+ = +15V$ D. C., $V- = -15V$ D. C.

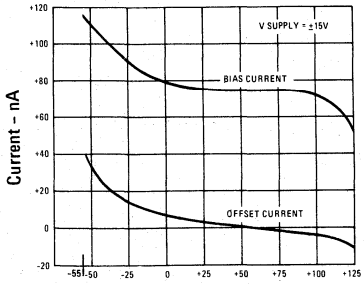
PARAMETER	TEMP	HA-2520 -55°C to +125°C			HA-2522 -55°C to +125°C			HA-2525 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	± 10.0			± 10.0			± 10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full		7.5K		5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	± 10.0	± 12.0		± 10.0	± 12.0		± 10.0	± 12.0		V
Output Current (Note 4)	+25°C	± 10	± 20		± 10	± 20		± 10	± 20		mA
Full Power Bandwidth (Notes 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	± 100	± 120		± 80	± 120		± 80	± 120		V/µs
Settling Time (Notes 1, 5, 8 &11)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See Transient Response Test Circuits and Waveforms Page 2-39
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S. R./$2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$

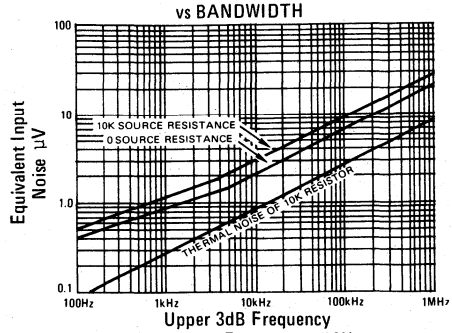
PERFORMANCE CURVES

V+ = 15V D. C., T_A = 25°C unless otherwise stated.

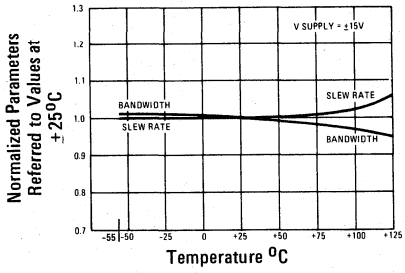
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



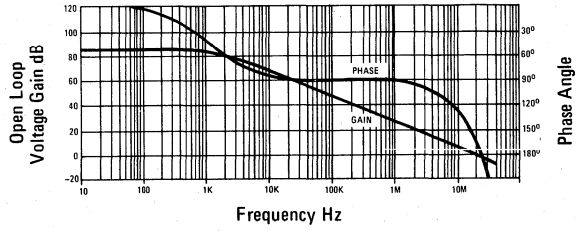
EQUIVALENT INPUT NOISE vs BANDWIDTH



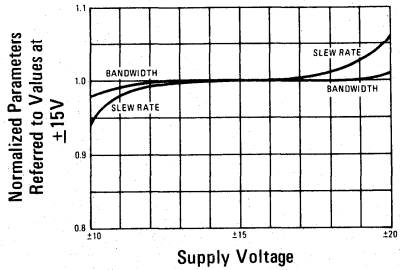
NORMALIZED AC PARAMETERS vs TEMPERATURE



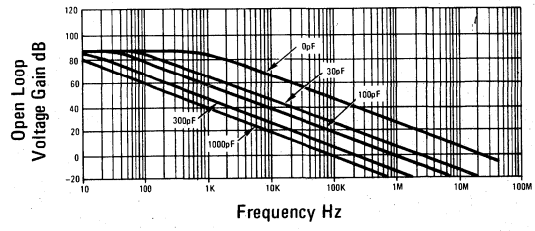
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



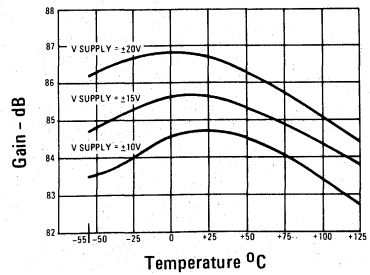
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



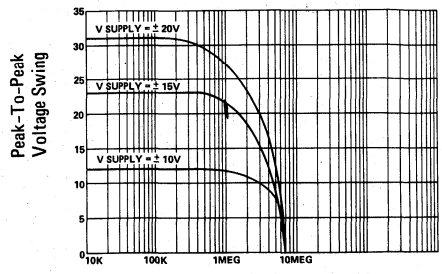
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

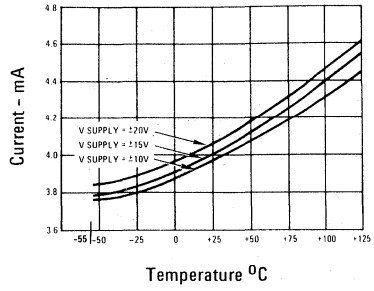


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

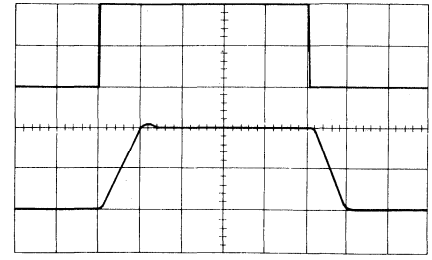


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



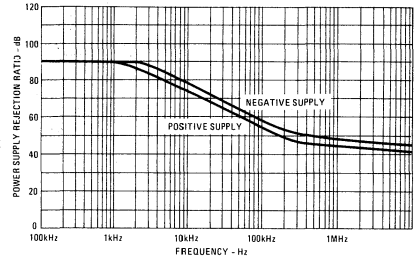
VOLTAGE FOLLOWER PULSE RESPONSE



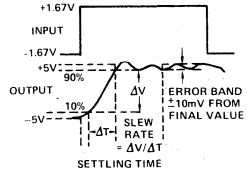
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

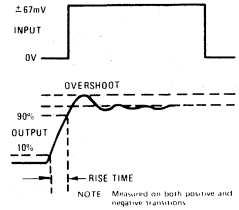
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



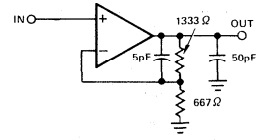
SLEW RATE AND SETTLING TIME



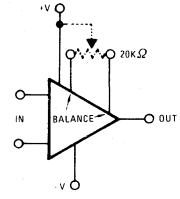
TRANSIENT RESPONSE



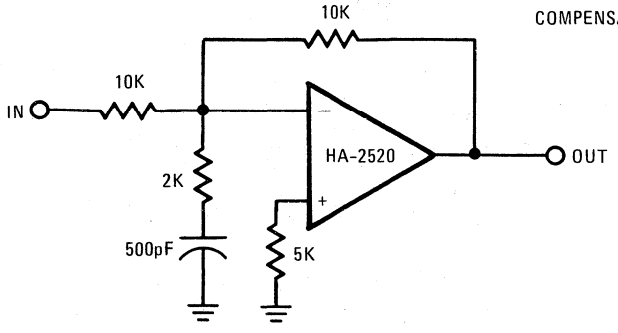
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED VOS ADJUSTMENT



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN

Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifiers

FEATURES

- VERY HIGH SLEW RATE — 600V/μs
- OPEN LOOP GAIN — 30kV/V
- WIDE GAIN-BANDWIDTH — 600MHz
- POWER BANDWIDTH — 9.5MHz
- LOW OFFSET VOLTAGE — 3mV
- INPUT VOLTAGE NOISE — 6nV / $\sqrt{\text{Hz}}$
- OUTPUT VOLTAGE SWING — $\pm$10V

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- RF OSCILLATORS

GENERAL DESCRIPTION

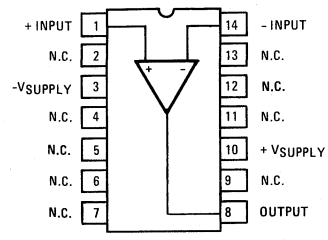
The Harris HA-2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency Bipolar dielectric isolation process and features dynamic parameters never before available from a truly differential device.

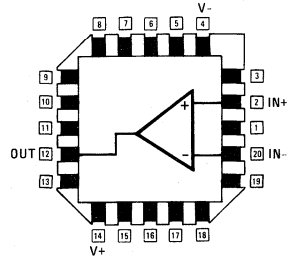
With a 600V/ μs slew rate and a 600MHz gain-band-width-product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full $\pm$10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

The HA-2539 is available in the 14 pin CERDIP. The HA-2539-2 denotes -55°C to +125°C operation while the HA-2539-5 operates over the 0°C to +75°C range.

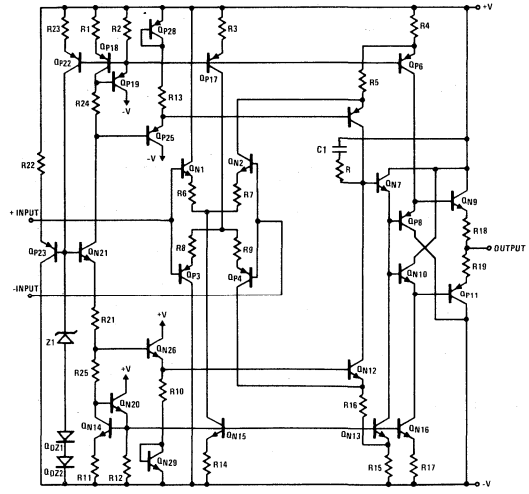
PINOUTS

TOP VIEWS





SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2539-2)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-2539-5)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

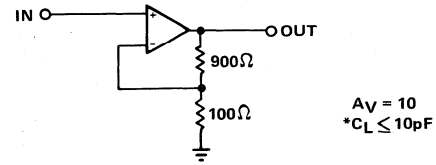
		HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Voltage Noise (f = 1kHz, $R_g = 0\Omega$)	+25°C		6			6		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		600			600		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		7			7		ns
Overshoot	+25°C		15			15		%
Slew Rate	+25°C	550	600		550	600		V/µs
Settling Time: 10V Step to 0.1%	+25°C		200			200		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. R_L = 1KΩ, VO = ± 10V
4. V_{CM} = ± 10V
5. V_O = 90mV.
6. A_V = 10.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5 VDC to ±15 VDC

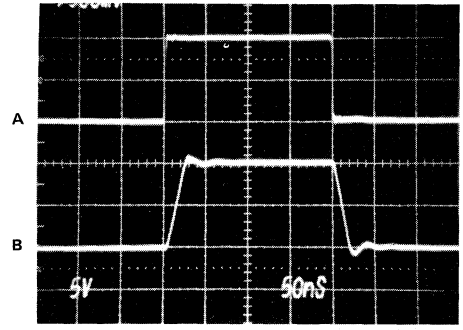
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT *



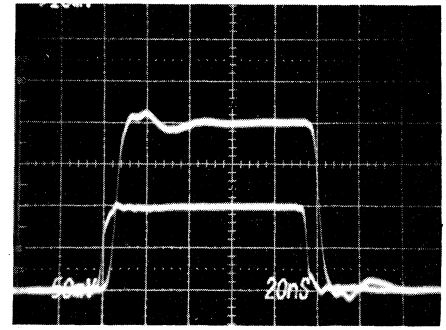
LARGE SIGNAL RESPONSE

Vertical Scale: A=0.5V/Div., B=5.0V/Div.
Horizontal Scale: Time: 50ns/Div.

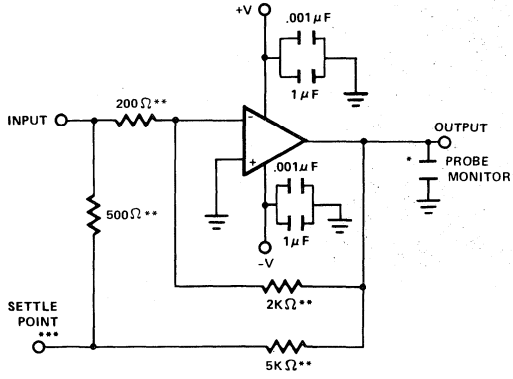


SMALL SIGNAL RESPONSE

Vertical Scale: Input=10mV/Div., Output=50mV/Div.
Horizontal Scale: 20ns/Div.



SETTLING TIME TEST CIRCUIT



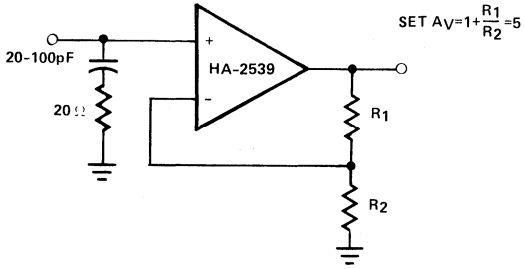
* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

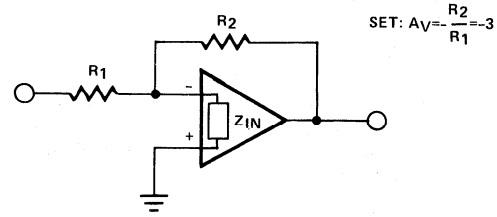
*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FREQUENCY COMPENSATION

COMPENSATION BY OVERDAMPING

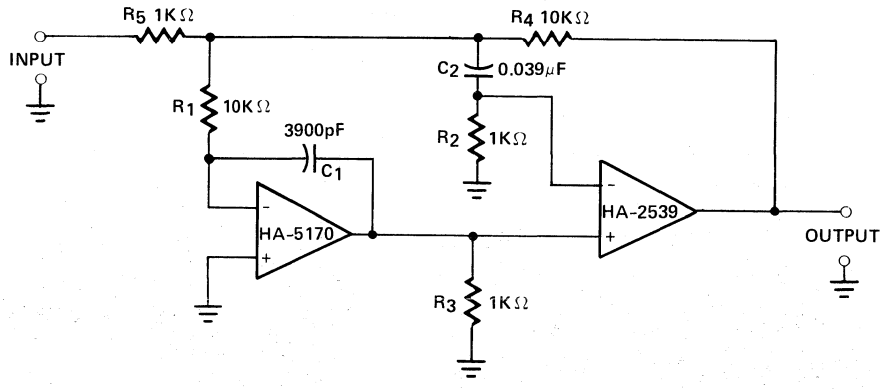


STABILIZATION USING Z_{IN}



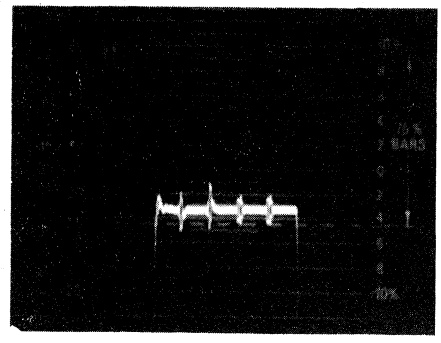
REDUCING DC ERRORS

COMPOSITE AMPLIFIER

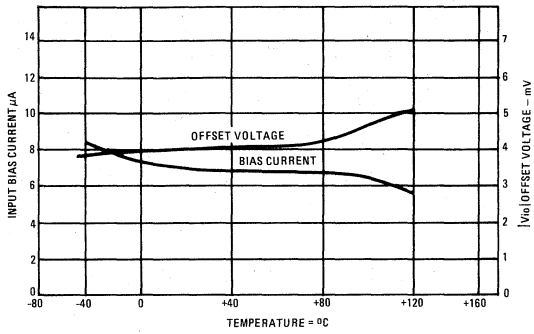


DIFFERENTIAL GAIN ERROR (3%)

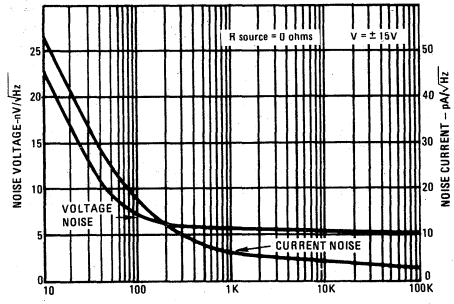
HA-2539 20dB VIDEO GAIN BLOCK



INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE

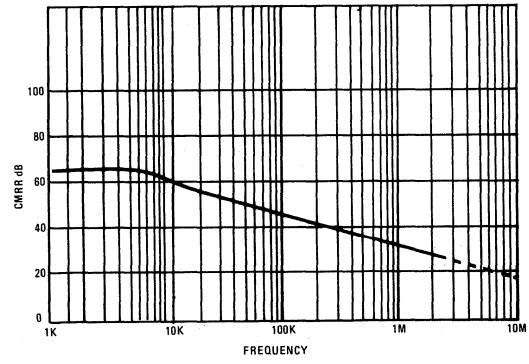


INPUT NOISE VOLTAGE AND NOISE CURRENT VS FREQUENCY

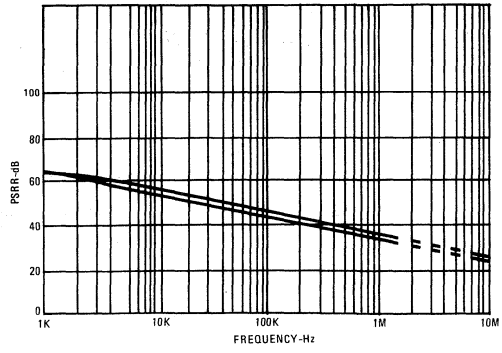


BROADBAND NOISE (0.1Hz to 1mHz)
Vertical Scale: 10μV/Div.
Horizontal Scale: 50ms/Div.

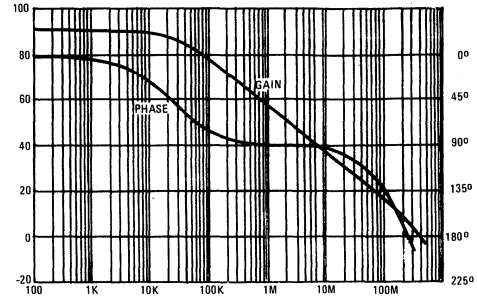
COMMON MODE REJECTION RATIO VS FREQUENCY



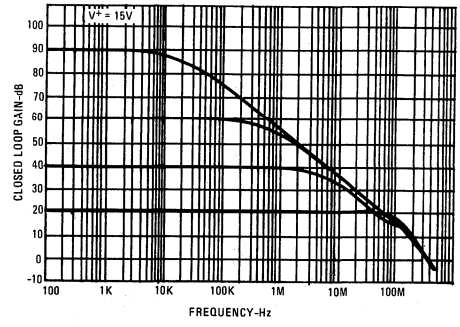
POWER SUPPLY REJECTION RATIO VS FREQUENCY



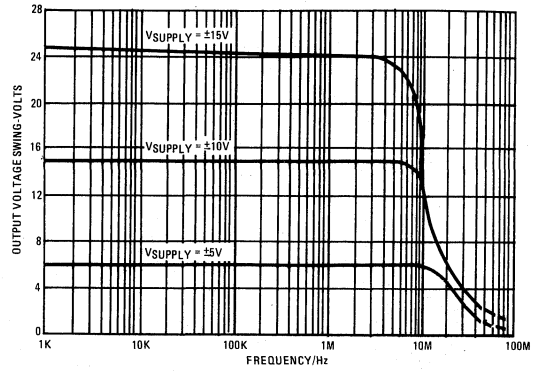
OPEN LOOP GAIN/PHASE VS FREQUENCY HA-2539



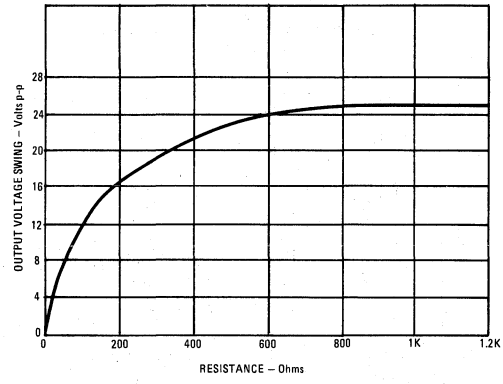
CLOSED LOOP FREQUENCY RESPONSE
FOR VARIOUS CLOSED LOOP GAINS



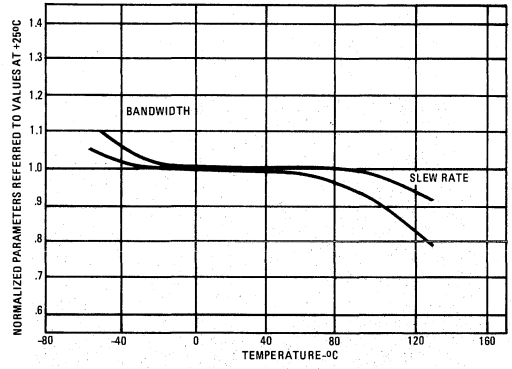
OUTPUT VOLTAGE SWING
VS. FREQUENCY



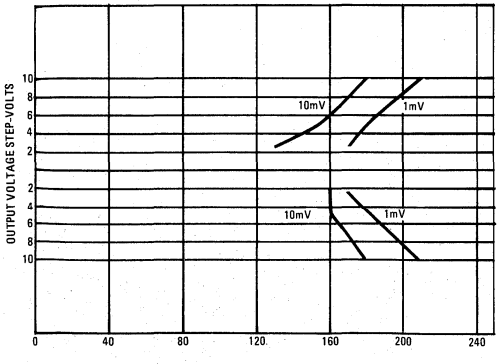
OUTPUT VOLTAGE SWING
VS. LOAD RESISTANCE



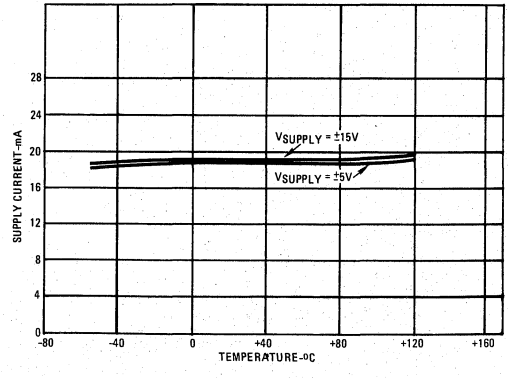
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



SETTLING TIME FOR VARIOUS
OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT VS.
TEMPERATURE AND SUPPLY VOLTAGE



HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifiers

FEATURES

- VERY HIGH SLEW RATE — 400V/μs
- FAST SETTLING TIME — 200ns
- WIDE GAIN-BANDWIDTH — 400MHz
- POWER BANDWIDTH — 6MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 6V/$\sqrt{Hz}$
- OUTPUT VOLTAGE SWING — $\pm$10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS

GENERAL DESCRIPTION

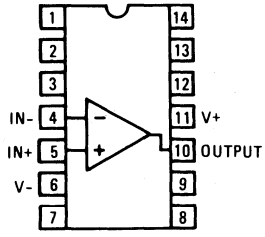
The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1K ohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

A 400V/ μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 250ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

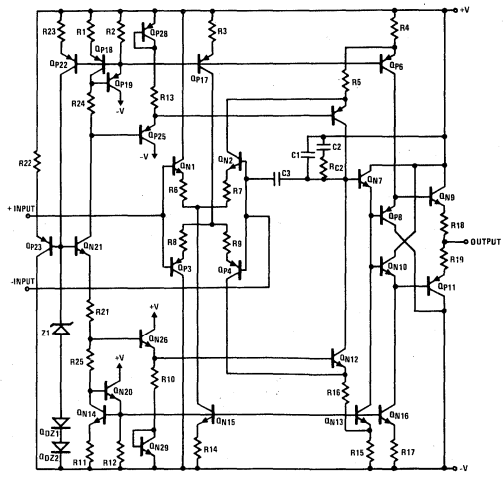
The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

PINOUT

TOP VIEW



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2540-2)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-2540-5)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

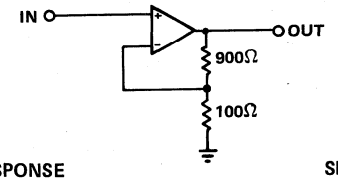
		HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		6			6		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		400			400		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5.5	6		5.5	6		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		14			14		ns
Overshoot	+25°C		5			5		%
Slew Rate	+25°C	350	400		350	400		V/µs
Settling Time: 10V Step to 0.1%	+25°C		200			200		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. R_L = 1KΩ, VO = ±10V
4. V_{CM} = ±10V
5. V_O = 90mV.
6. A_V = 10.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5 VDC to ±15 VDC

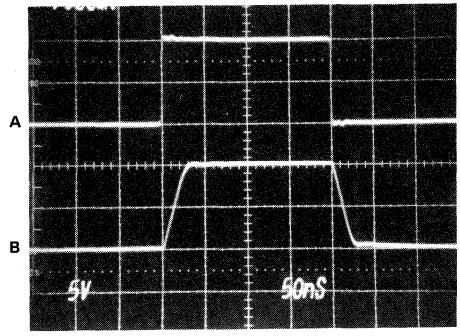
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE
TEST CIRCUIT*

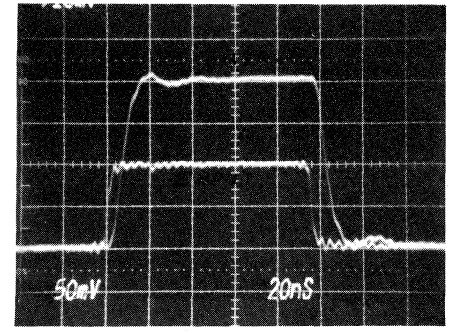


A_V = 10
*$C_L \leq$ 10pF

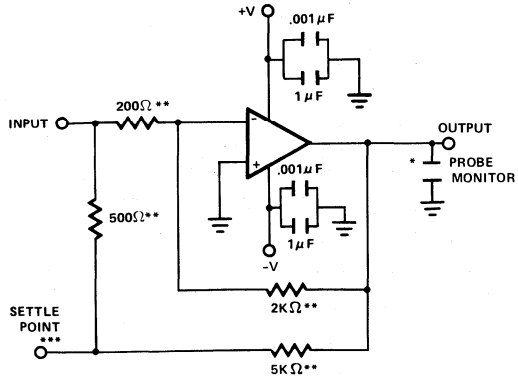
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A=0.5v/Div., B=5.0V/Div.)
Horizontal Scale: (Time: 50ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: Input=10mV/Div.; Output=50mV/Div.
Horizontal Scale: 20ns/Div.



SETTLING TIME TEST CIRCUIT

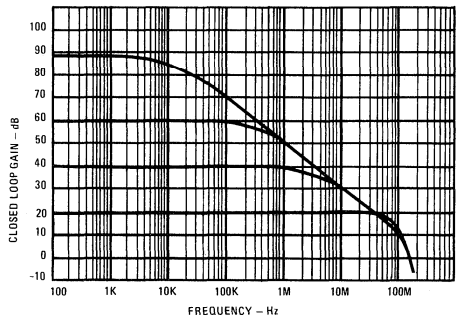


* Load Capacitance should be less than 10pF.

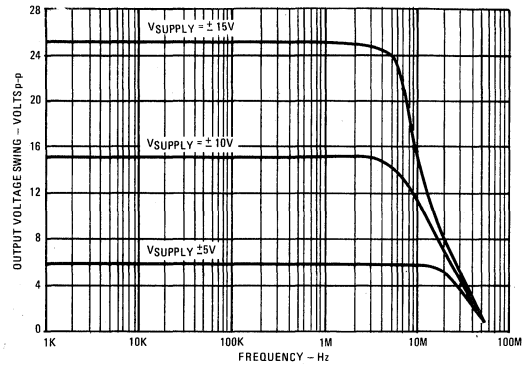
** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

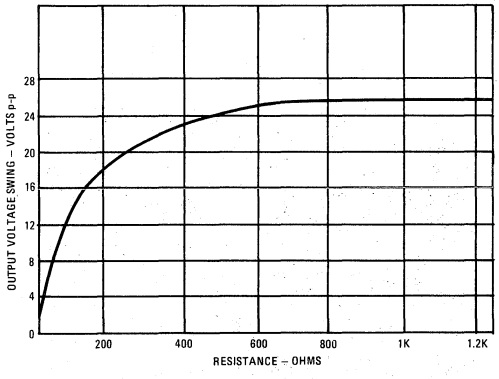
CLOSED LOOP FREQUENCY RESPONSE



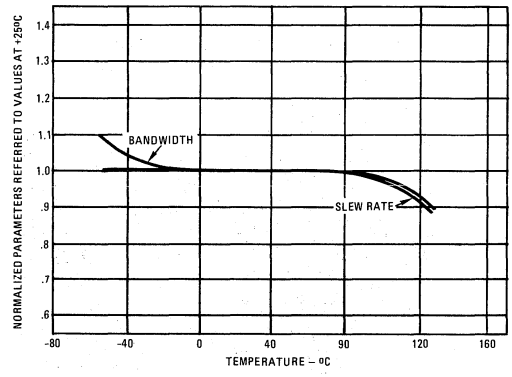
OUTPUT VOLTAGE SWING VS. FREQUENCY



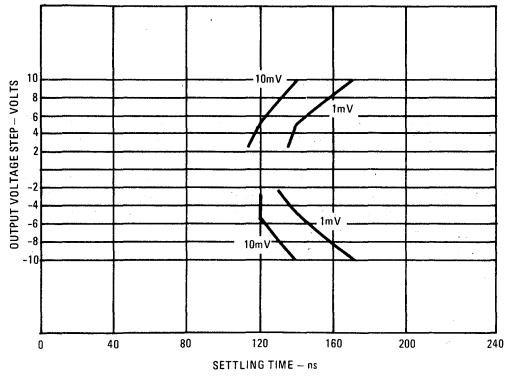
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



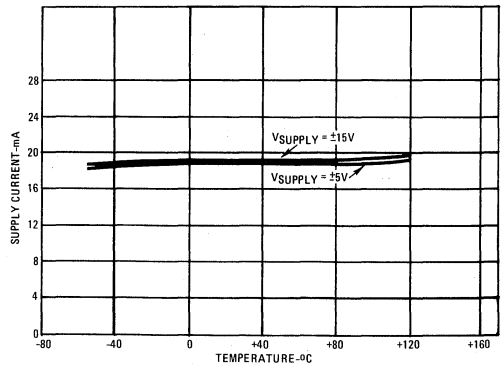
NORMALIZED AC PARAMETERS VS. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

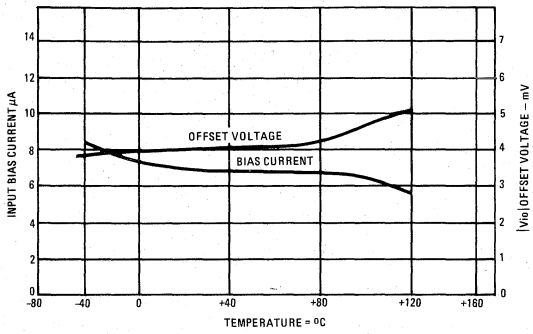


POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE

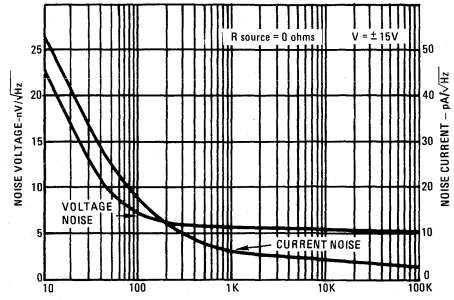


PERFORMANCE CURVES

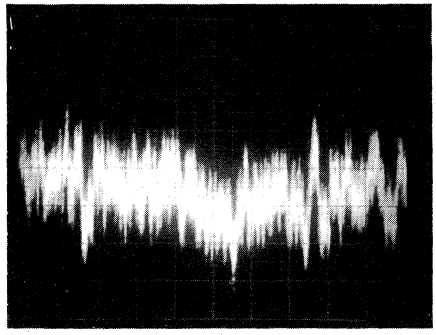
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



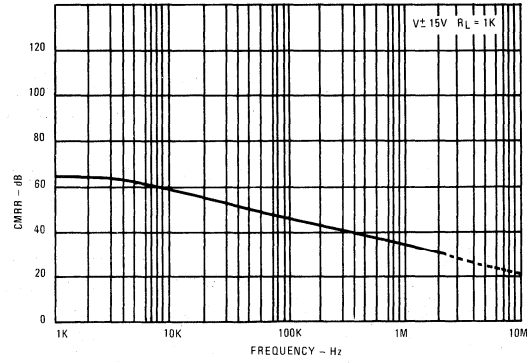
INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY



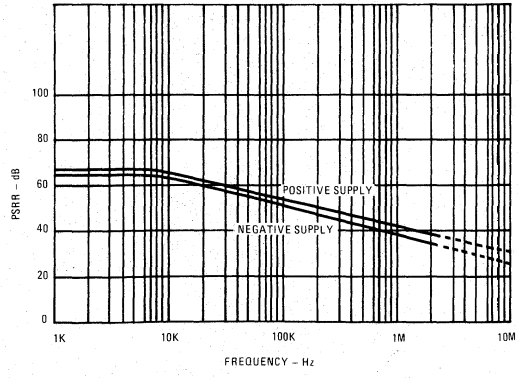
BROADBAND NOISE (0.1Hz TO 1MHz)
Vertical Scale: 10 μV/Div.
Horizontal Scale: 50ms/Div.



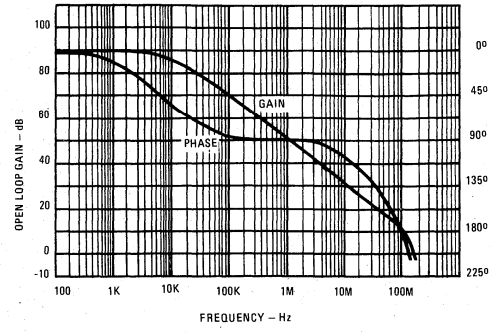
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY

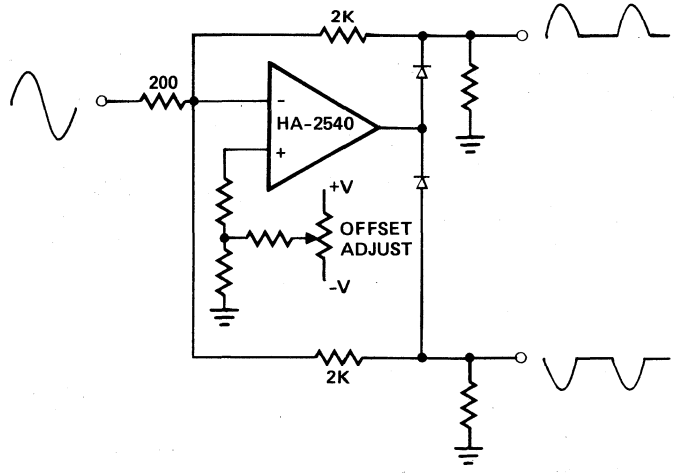


OPEN LOOP GAIN/PHASE VS. FREQUENCY HA-2540

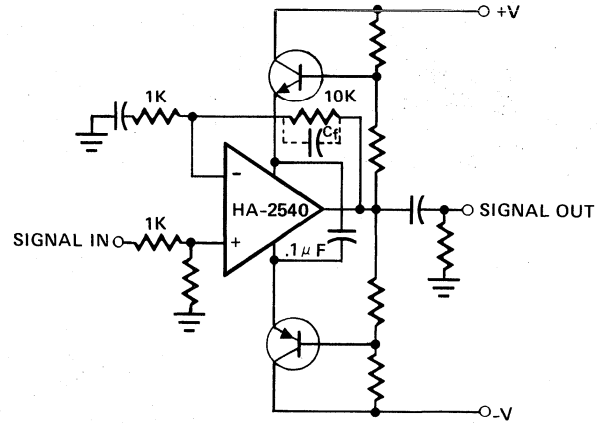


WIDEBAND SIGNAL SPLITTER

With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING



HARRIS

ADVANCE

HA-2541

Wideband, Fast Settling Operational Amplifiers

FEATURES

- UNITY GAIN STABILITY
- FAST SETTLING TIME (.1%) 80ns
- HIGH SLEW RATE 300V/μs
- UNITY GAIN BANDWIDTH 40MHz
- POWER BANDWIDTH 5MHz
- OUTPUT VOLTAGE SWING ±10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED A/D INPUT BUFFER

DESCRIPTION

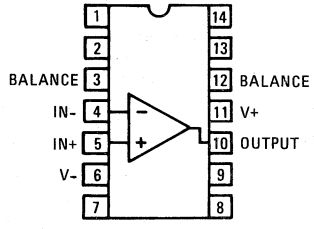
The HA-2541 is an internally compensated bipolar operational amplifier which represents the latest addition to the Harris series of high speed, wideband op amps. Featuring unity gain stable operation, the HA-2541 is ideally suited for video and pulse applications which often require stable amplifier response at low closed loop gains.

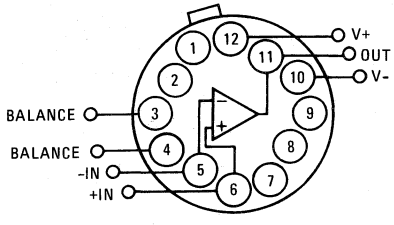
The HA-2541 is unique in that it does not trade-off dynamic performance for stability. The characteristics of many wideband amplifiers regress back into the range of a general purpose amplifier when compensated for unity gain operation. But features such as 300V/μs slew rate and 40MHz unity gain bandwith clearly show that this is not the case for the HA-2541. These features, along with 80ns settling time, make this product an excellent choice for high speed data acquisition systems.

Packaged in a 12 pin (TO-8) can or 14 lead plastic D.I.P., the HA-2541 is pin compatible with the HA-2540 and HA-5195 wideband op amps.

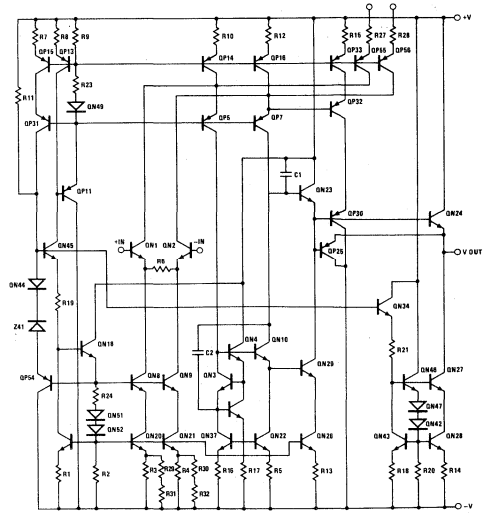
PINOUTS

TOP VIEWS





SCHEMATIC



HARRIS

ADVANCE

HA-2542

Wideband, High Slew Rate High Output Current Operational Amplifiers

FEATURES

- STABLE AT GAINS OF 2 OR GREATER
- VERY WIDEBAND 60MHz
- HIGH SLEW RATE 350V/μs
- HIGH OUTPUT CURRENT 100mA
- POWER BANDWIDTH 5.5MHz
- OUTPUT VOLTAGE SWING ±10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- COAXIAL CABLE DRIVERS
- FAST SAMPLE – HOLD CIRCUITS
- HIGH FREQUENCY SIGNAL CONDITIONING CIRCUITS

DESCRIPTION

The HA-2542 is wideband, high slew rate, monolighic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

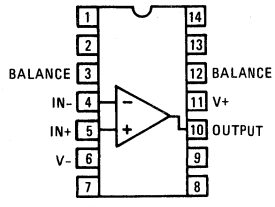
Utilizing the advantages of the Harris I.D. technology this amplifier offers 350V/μs slew rate, 60MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to gains of 2.

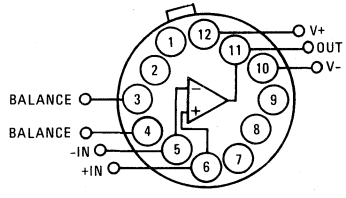
The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits with gain. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse/video amplifiers. Other applications utilizing HA-2524's advantages include wideband amplifiers and fast sample-hold circuits.

Packaged in a 12 pin (TO-8) can of 14 lead plastic D. I. P. the HA-2542 is pin compatible with the HA-2540, HA-2541 and HA-5190.

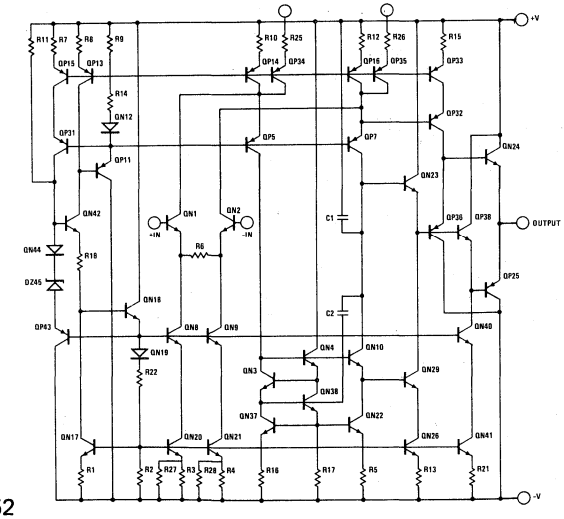
PINOUTS

TOP VIEWS





SCHEMATIC



HARRIS HA-2600/2602/2605

WideBand, High Impedance Operational Amplifiers

FEATURES

- WIDE BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

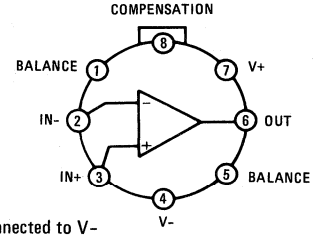
DESCRIPTION

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

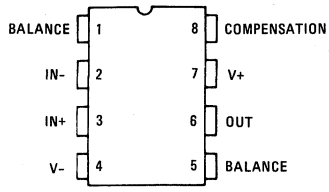
In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

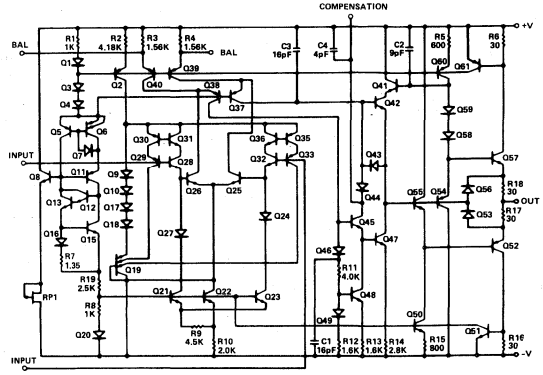
PINOUTS



Case Connected to V- TOP VIEWS



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Ranges:	
Differential Input Voltage	±12.0V	HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
Peak Output Current	Full Short Circuit Protection	HA-2605	$0^oC \leq T_A \leq +75^oC$
Internal Power Dissipation	300mW	Storage Temperature Range:	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

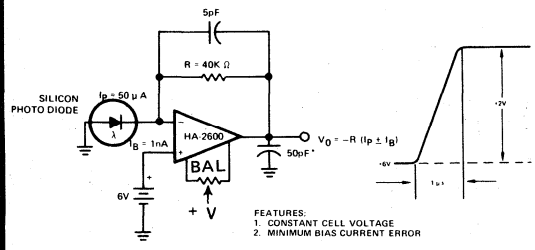
$V+ = +15V$ D. C., $V- = -15V$ D. C.

PARAMETER	TEMP	HA-2600 -55°C to +125°C			HA-2602 -55°C to +125°C			HA-2605 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 9)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 4, 10)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 7)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 6 & 7)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 5, 7 & 11)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 5, 7 &11)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $V_O < 90mV$
4. $V_O = \pm 10V$
5. $C_L = 100pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits & Waveforms Page 2-57.
9. $\Delta VS = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

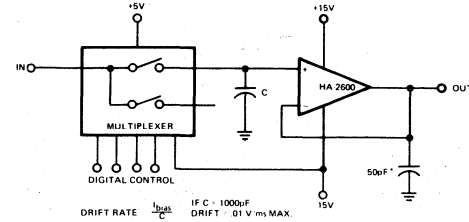
TYPICAL APPLICATIONS

PHOTO-CURRENT TO VOLTAGE CONVERTER



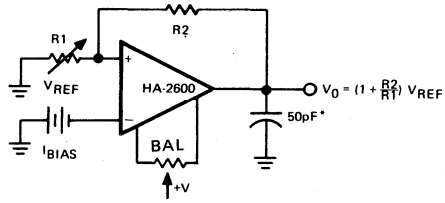
FEATURES:
1. CONSTANT CELL VOLTAGE
2. MINIMUM BIAS CURRENT ERROR

SAMPLE – AND – HOLD



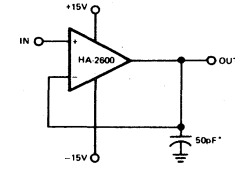
DRIFT RATE $\frac{I_{bias}}{C}$ IF C = 1000pF
DRIFT = .01 V/ms MAX.

REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. MINIMUM BIAS CURRENT IN REFERENCE CELL
2. SHORT-CIRCUIT PROTECTION

VOLTAGE FOLLOWER



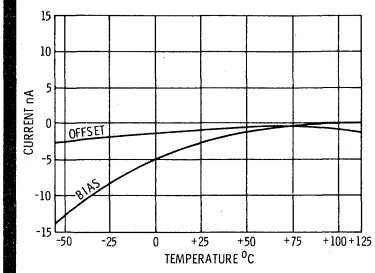
1.000 GAIN 0.9999
Z_{in} = -10^{12} MIN.
Z_{out} = .01 MAX.

SLEW RATE = 4V/μs MIN.
B.W. = 12MHz TYP.
OUTPUT SWING = ± 10V MIN. TO 50kHz

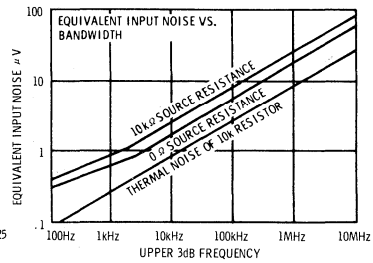
*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

PERFORMANCE CURVES

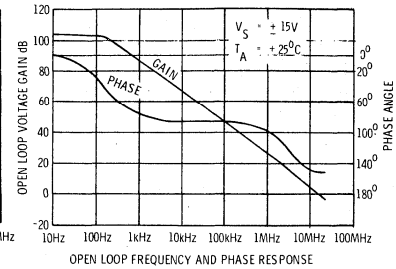
V+ = 15V D. C., T_A = 25°C unless otherwise stated.



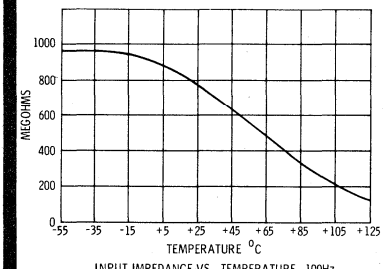
INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE



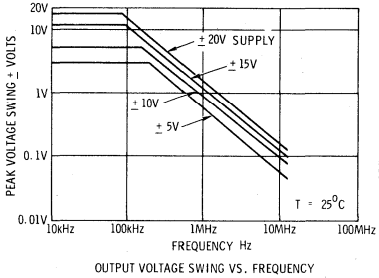
BROADBAND NOISE CHARACTERISTICS



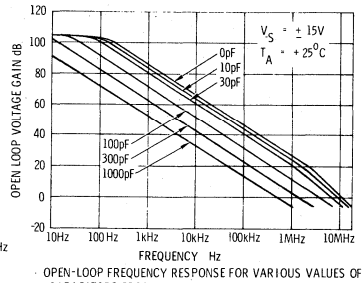
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

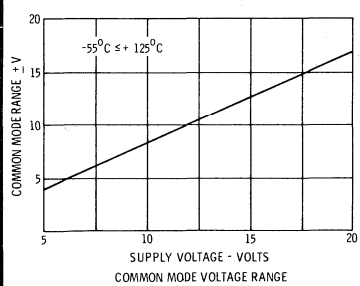


OUTPUT VOLTAGE SWING VS. FREQUENCY

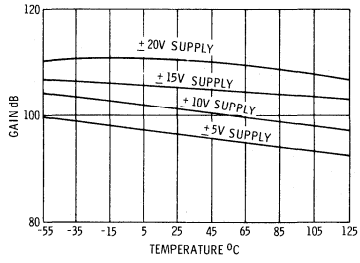


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

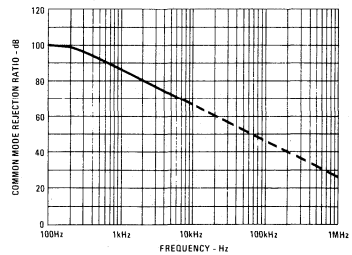
Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.



COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE

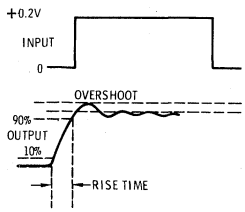


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE



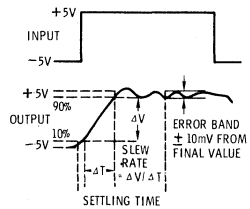
COMMON MODE REJECTION RATIO
VS. FREQUENCY

TRANSIENT RESPONSE

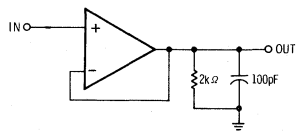


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

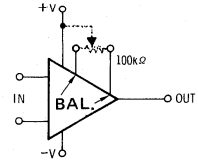
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED VOS ADJUSTMENT



HARRIS HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

FEATURES

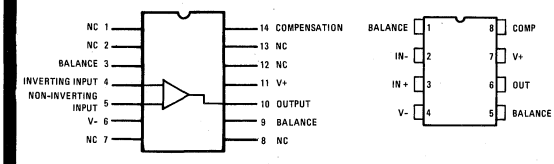
- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

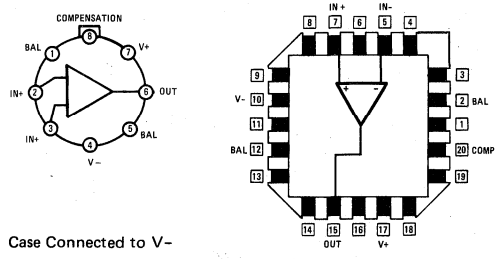
APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

PINOUTS

TOP VIEWS





Case Connected to V-

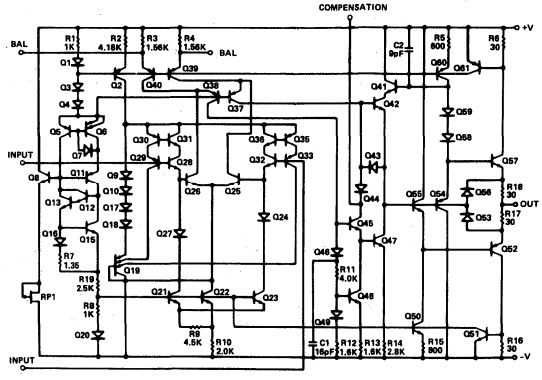
DESCRIPTION

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

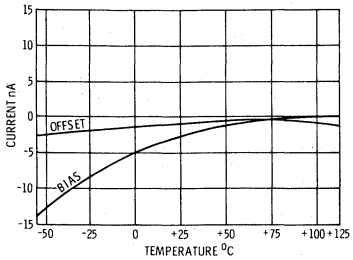
ELECTRICAL CHARACTERISTICS $V^+ = +15$ VDC, $V^- = -15$ VDC

		HA-2620 −55°C to +125°C			HA-2622 −55°C to +125°C			HA-2625 0°C to +75°C			
PARAMETER	TEMPERATURE	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

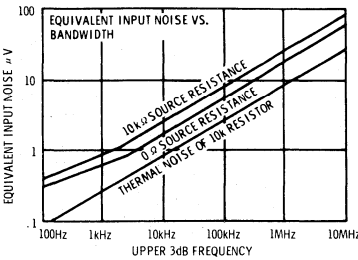
NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

TYPICAL PERFORMANCE CURVES

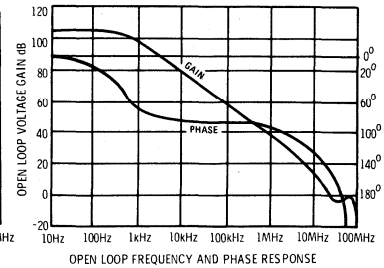
V+ = +15V D. C., V- = -15V D. C., T_A = 25°C unless otherwise stated.



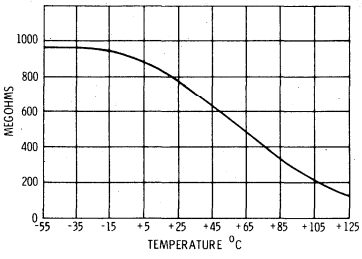
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



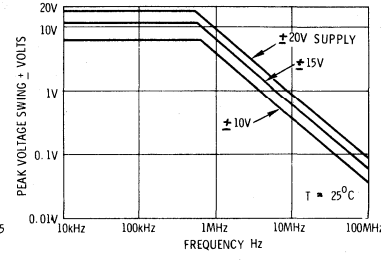
BROADBAND NOISE CHARACTERISTICS



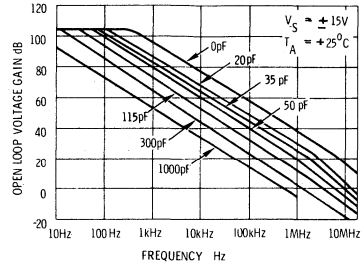
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

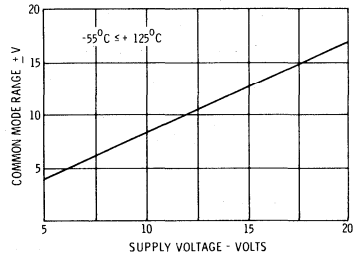


OUTPUT VOLTAGE SWING VS. FREQUENCY

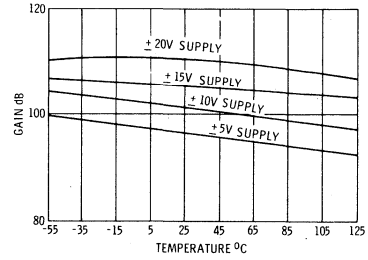


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM **COMPENSATION** PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain <5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

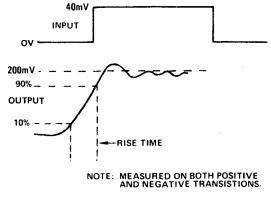


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



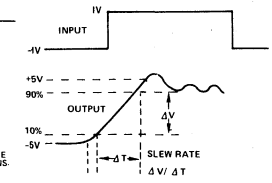
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

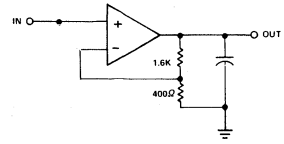


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSISTIONS.

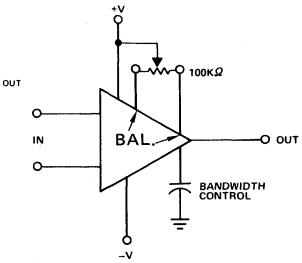
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE

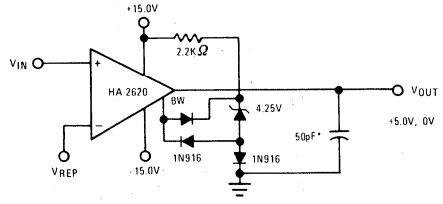


SUGGESTED VOS ADJUSTMENT AND COMPENSATION HOOK-UP

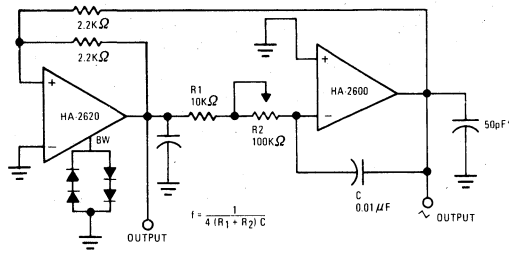


TYPICAL APPLICATIONS

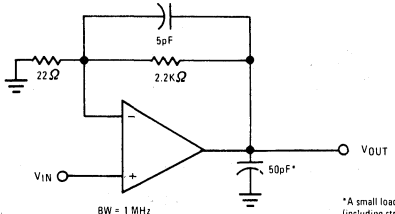
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS

HA-2630/2635

High Performance Current Booster

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

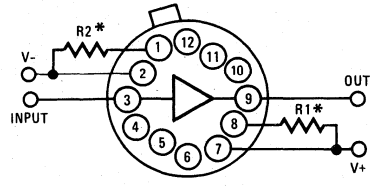
HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

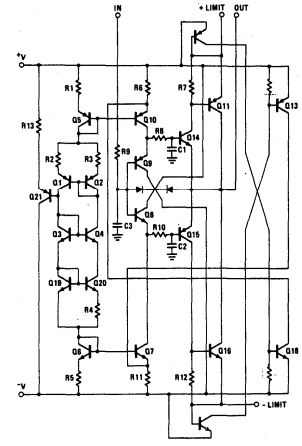
PINOUT

TOP VIEW



* Optional Current Limiting Resistor

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 40V
Input Voltage Range ± V Supply
Output Current (Note 2) ±700mA
Internal Power Dissipation (Note 6) Free Air: 1W
In Heat Sink: 4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

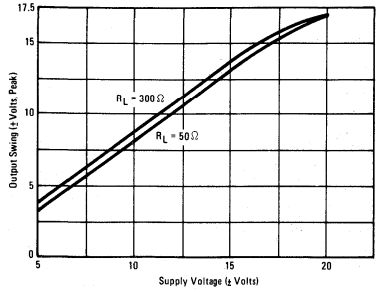
PARAMETER	TEMP.	HA-2630 $-55^{o}C$ to $+125^{o}C$ MIN.	TYP.	MAX.	HA-2635 $0^{o}C$ to $+75^{o}C$ MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12		±10	±12		V
Output Current (Note 1)	Full	± 300	± 400		± 300	± 400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

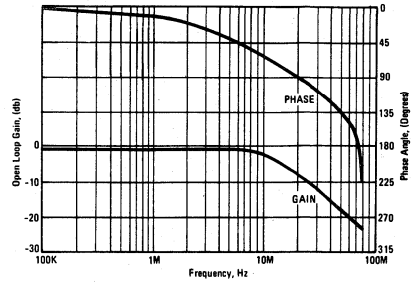
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

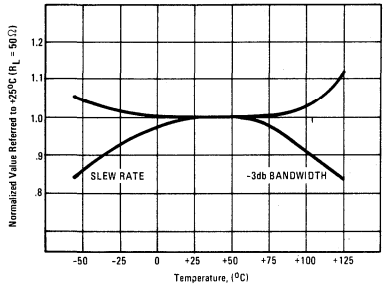
OUTPUT SWING
(R_{LIMIT} = 0Ω)



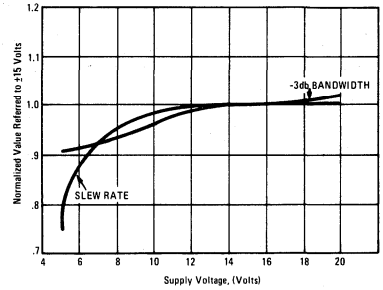
OPEN LOOP FREQUENCY AND
PHASE RESPONSE (R_L = 50Ω, C_L ≈10pf)



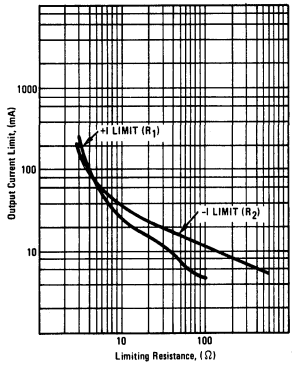
NORMALIZED AC PARAMETERS vs.
TEMPERATURE (R_L = 50Ω)



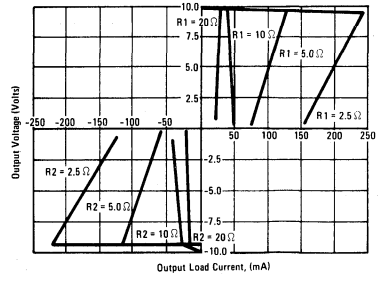
NORMALIZED AC PARAMETERS vs.
SUPPLY VOLTAGE (R_L = 50Ω)



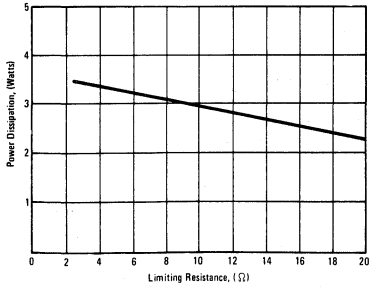
OUTPUT CURRENT LIMITING vs.
LIMITING RESISTANCE



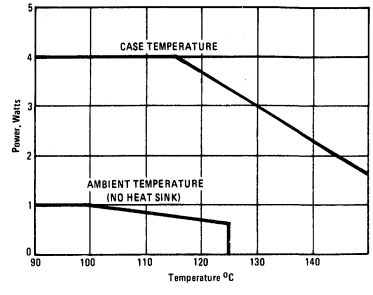
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE
WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V

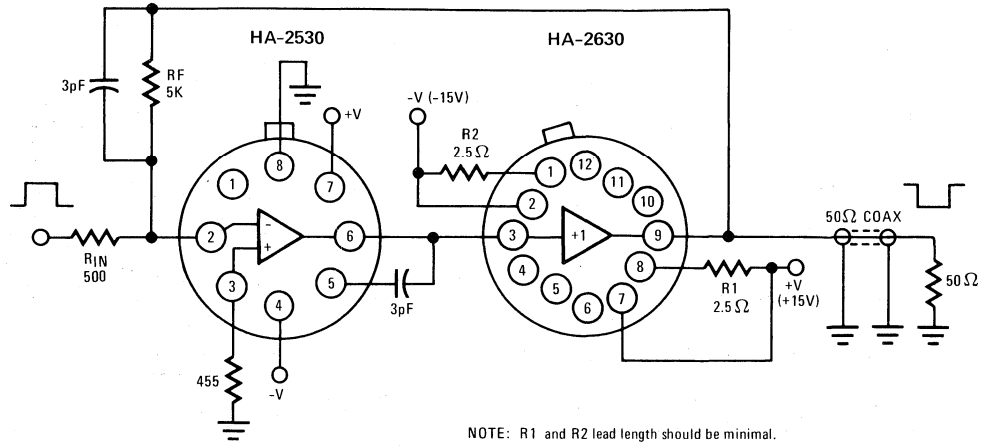


MAXIMUM ALLOWABLE INTERNAL
POWER DISSIPATION vs. TEMPERATURE



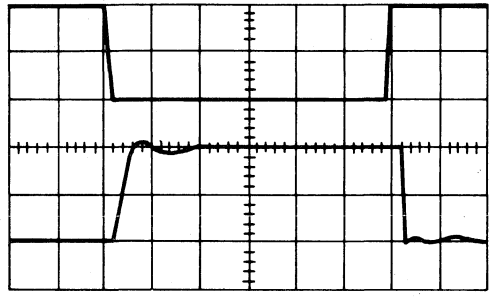
TYPICAL APPLICATION

20dB, 5MHz VIDEO COAXIAL LINE DRIVER



NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

HARRIS

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

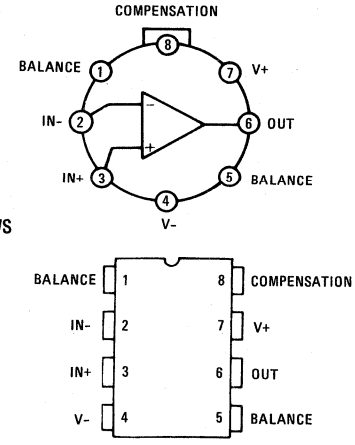
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

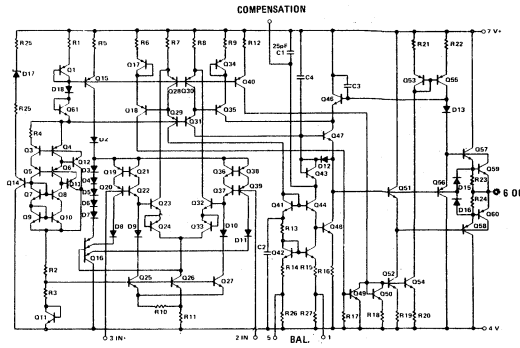
HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUTS

TOP VIEWS



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

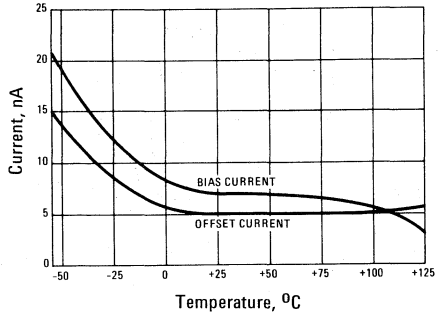
PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance **(Note 10)**	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35			±35			V
Output Current **(Note 9)**	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth **(Notes 3 &11)**	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	**100**		60	**100**	ns
Overshoot (Notes 4, 6)	+25°C		15	**30**		15	**40**	%
Slew Rate (Note 6)	+25°C	**±3**	**±5**		**±2.5**	**±5**		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.

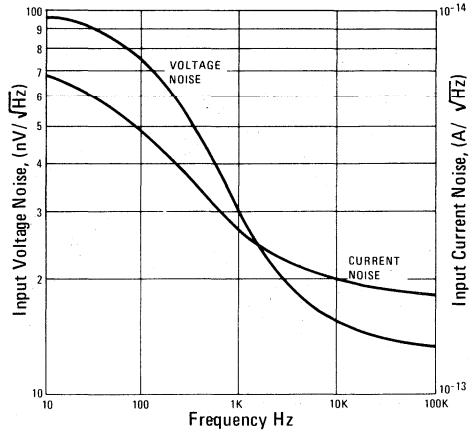
PERFORMANCE CURVES

V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

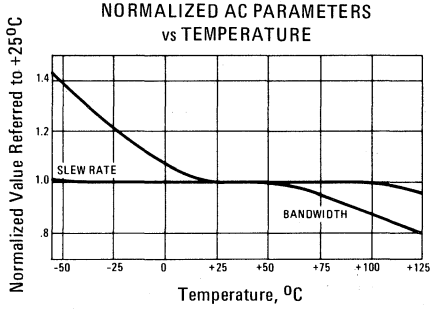
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



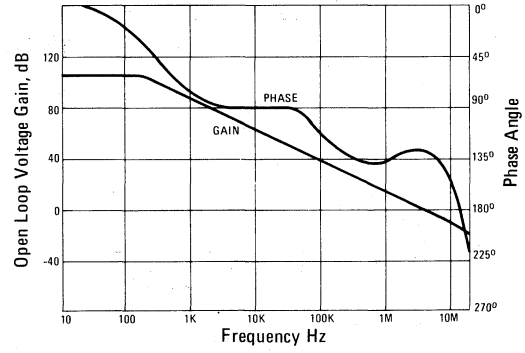
INPUT NOISE CHARACTERISTICS



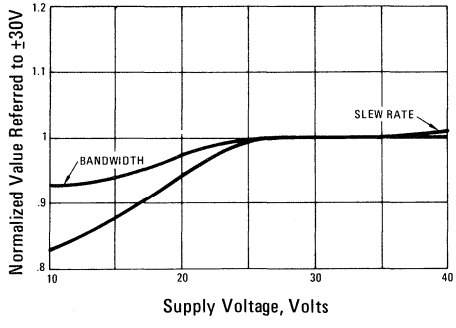
NORMALIZED AC PARAMETERS vs TEMPERATURE



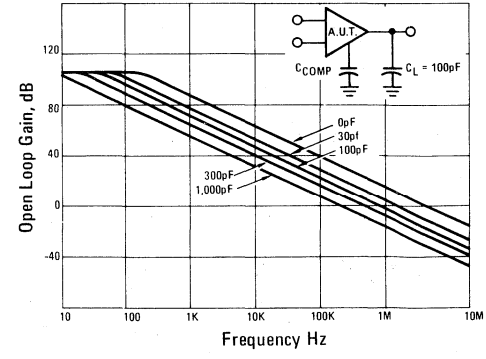
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



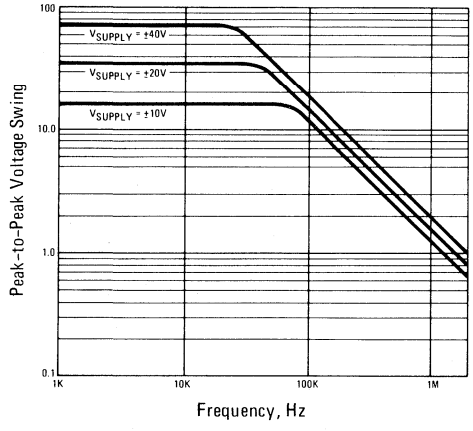
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



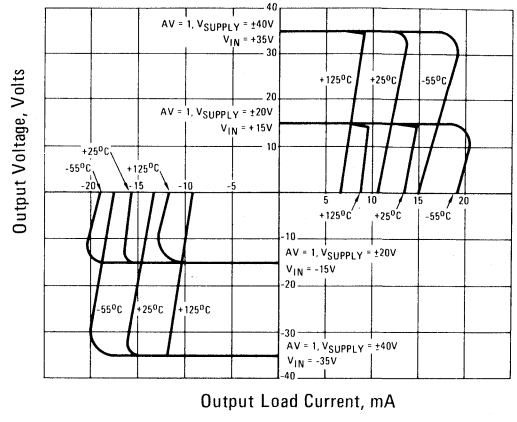
NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

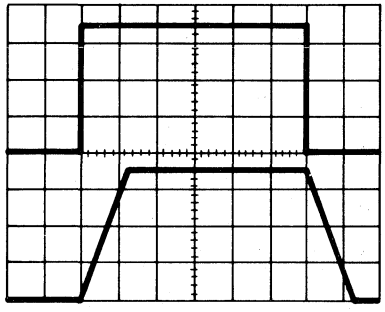


OUTPUT CURRENT CHARACTERISTIC



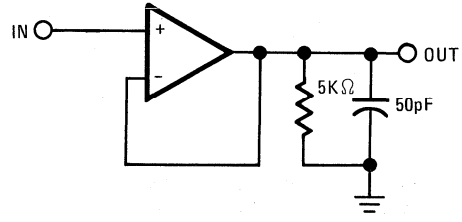
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE

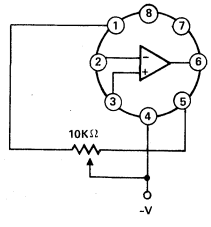


R_L = 5K, C_L = 50pF
Vertical = 10V/Div.
Horizontal = 5µs/Div.
T_A = +25°C
V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



SUGGESTED VOS ADJUSTMENT



HARRIS

HA-2650/2655

Dual High Performance Operational Amplifier

Not Recommended For New Designs See HA-5102

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AVG. OFFSET VOLTAGE DRIFT — 8μV/^{o}C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — $\pm$2V TO $\pm$20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

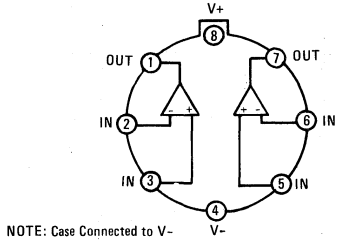
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μsec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhnaced by front-end performance that includes 1.5mV offset voltage, 8μV/^{o}C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500M input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

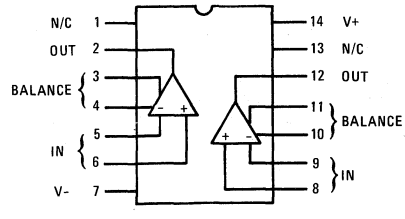
HA-2650/2655 are offered in 14 pin DIP and metal TO-99 packages and are also available in dice form. HA-2650 is specified form -55^{o}C to +125^{o}C. HA-2655 operates from 0^{o}C to +75^{o}C.

PINOUTS

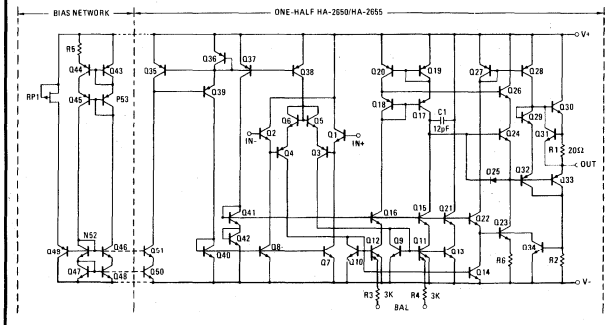
TOP VIEWS



NOTE: Case Connected to V-



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	$-55^oC \leq T_A \leq +125^oC$	
HA-2655	$0^oC \leq T_A \leq +75^oC$	
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$	

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

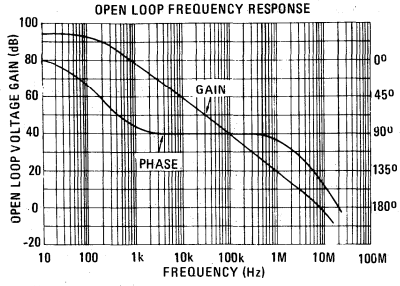
PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 -55°C to +125°C TYP.	HA-2650 -55°C to +125°C MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 0°C to +75°C TYP.	HA-2655 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 & 10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	40		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

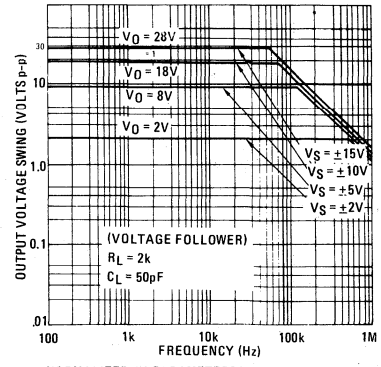
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

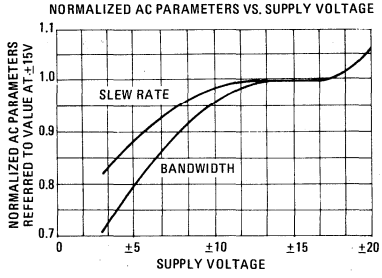
OPEN LOOP FREQUENCY RESPONSE



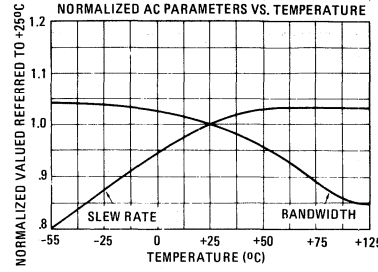
OUTPUT VOLTAGE SWING VS. FREQUENCY



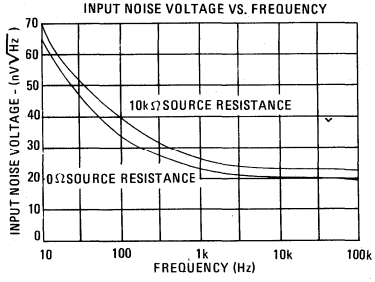
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



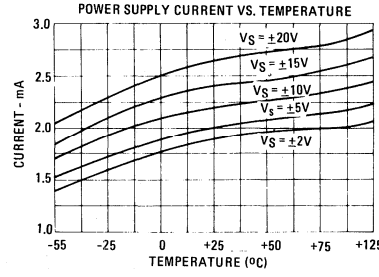
NORMALIZED AC PARAMETERS VS. TEMPERATURE



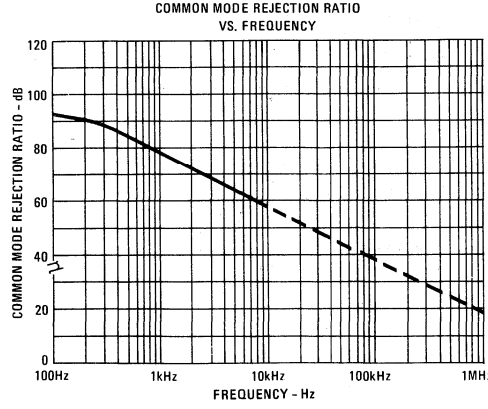
INPUT NOISE VOLTAGE VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

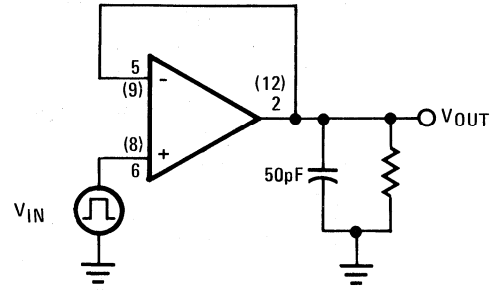


COMMON MODE REJECTION RATIO VS. FREQUENCY



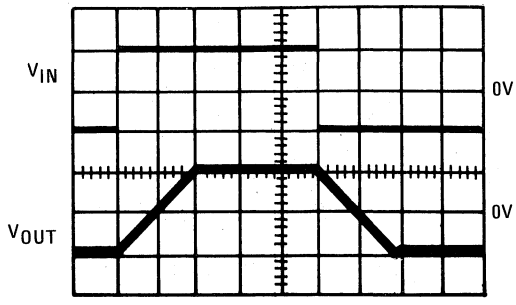
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

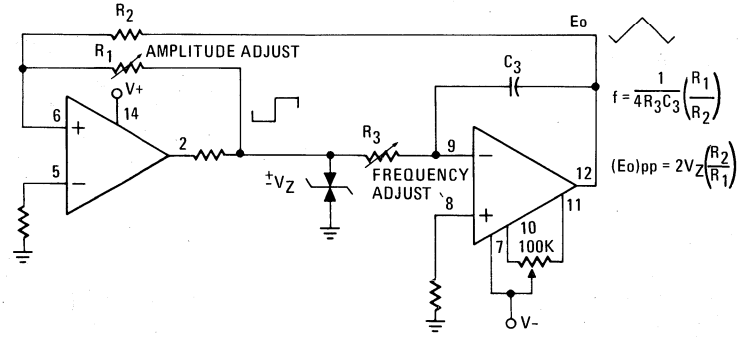
SLEWING WAVEFORM



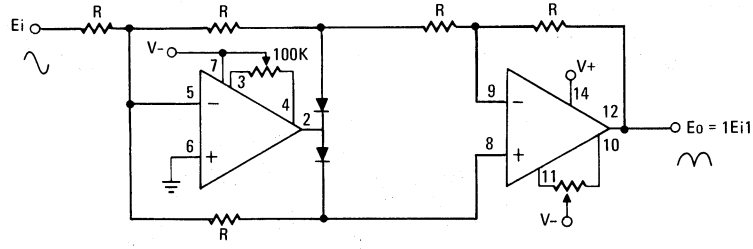
VERTICAL 5V/DIV. HORIZONTAL 1 μs/DIV.

TYPICAL APPLICATIONS

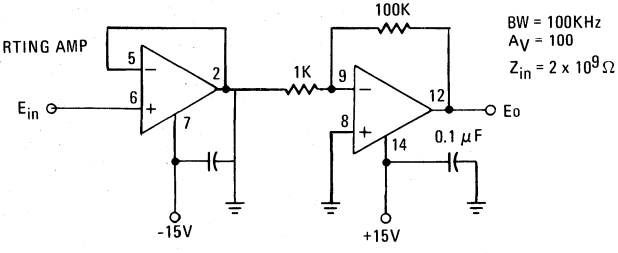
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

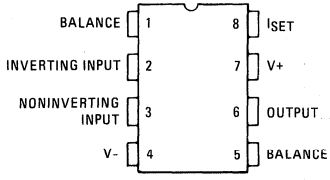
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

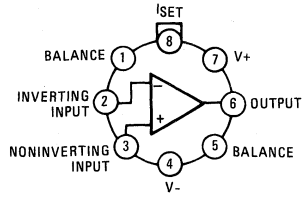
HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUTS

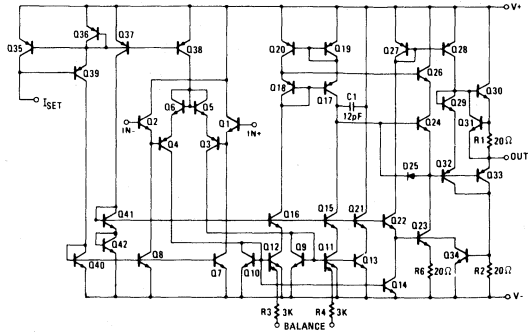
TOP VIEWS



Note: Case tied to V-



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±2.0			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V-- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	40K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	± 12	±13.5		± 12	±13.5		± 12	±13.5		± 12	±13.5		V
	Full	± 10			± 10			± 10			± 10			V
Output Current (Note 5)	25°C		± 0.5			± 5.0			± 0.5			± 5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

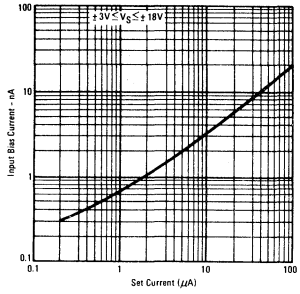
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

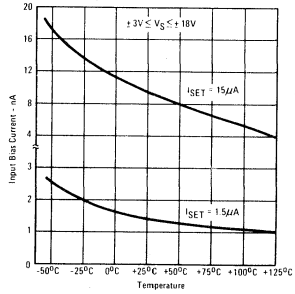
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

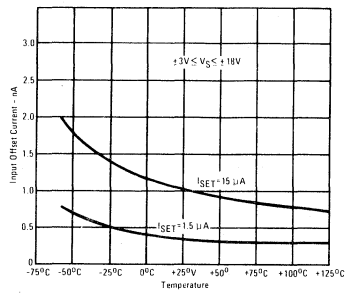
INPUT BIAS CURRENT
vs. SET CURRENT



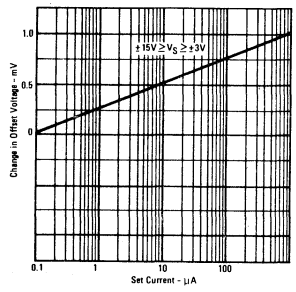
INPUT BIAS CURRENT
vs. TEMPERATURE



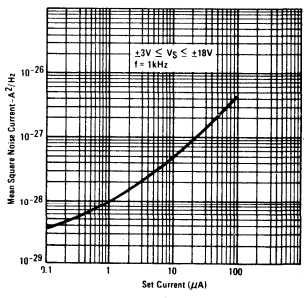
INPUT OFFSET CURRENT
vs. TEMPERATURE



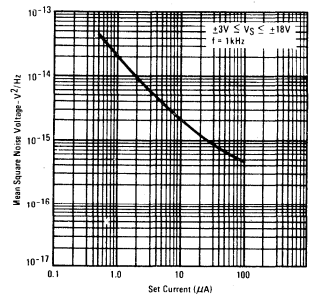
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



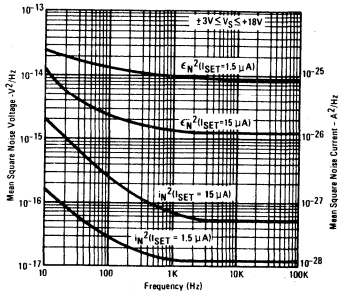
INPUT NOISE CURRENT
vs. I_{SET}



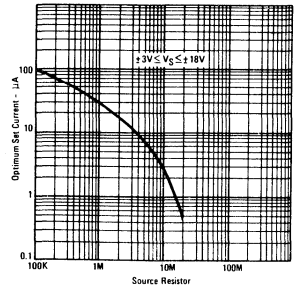
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



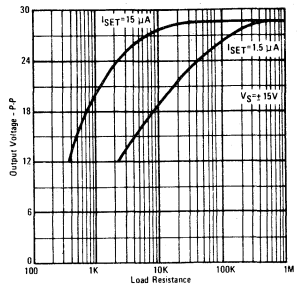
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



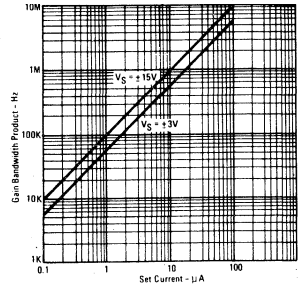
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

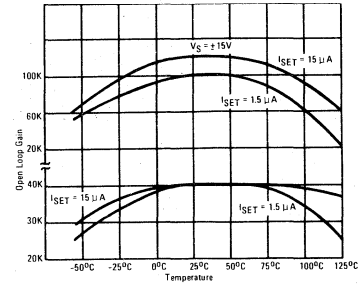
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



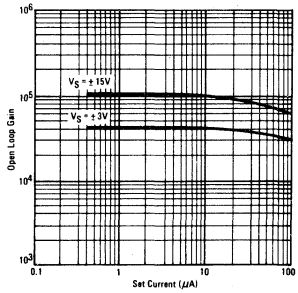
GAIN BANDWIDTH PRODUCT vs. I_{SET}



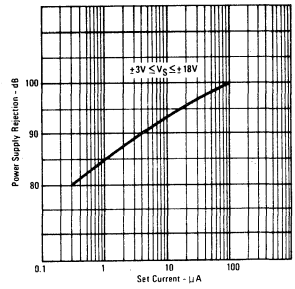
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



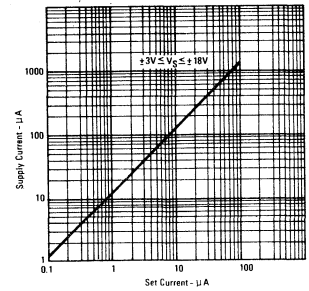
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



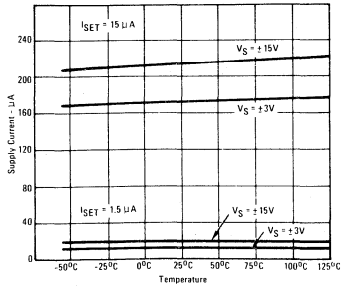
POWER SUPPLY REJECTION vs. I_{SET}



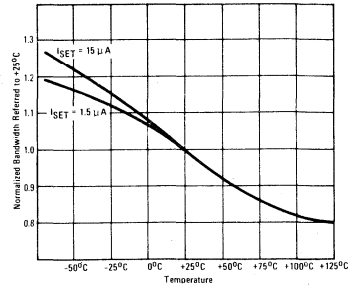
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE

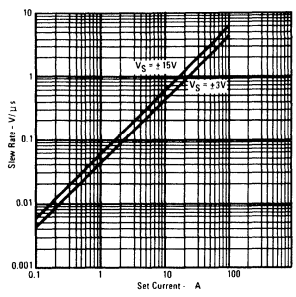


NORMALIZED BANDWIDTH vs. TEMPERATURE

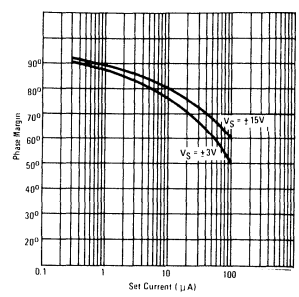


PERFORMANCE CURVES

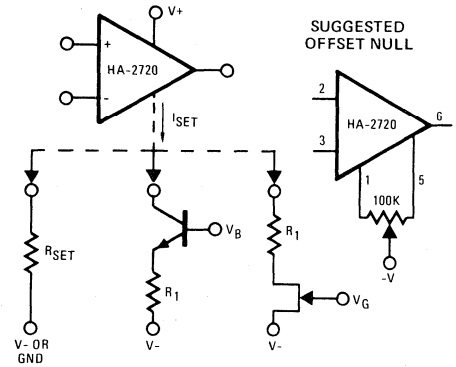
SLEW RATE vs. I_{SET}



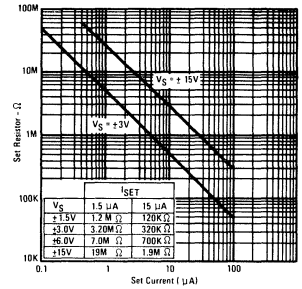
PHASE MARGIN vs. SET CURRENT



TYPICAL BIASING CIRCUITS

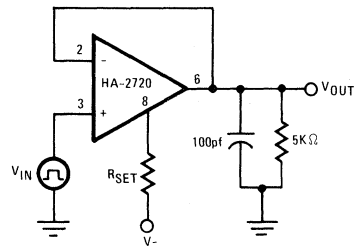


SET CURRENT VS. SET RESISTOR

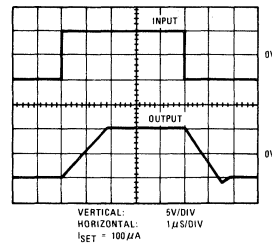


V_S	I_{SET} 1.5 µA	15 µA
±1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



HARRIS

HA-2730/35

Not Recommended For New Designs See HA-5142

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

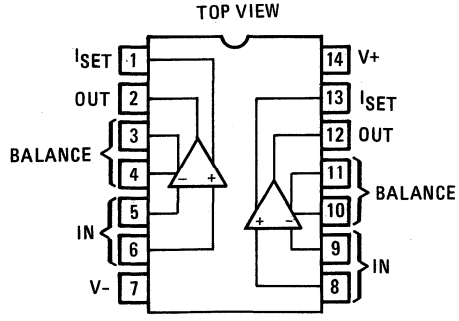
DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

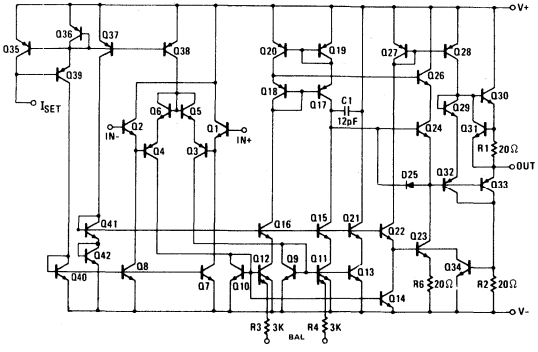
HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side) V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±2.0			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Each Side) V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	40K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	± 12	±13.5		± 12	±13.5		± 12	±13.5		± 12	±13.5		V
	Full	± 10			± 10			± 10			± 10			V
Output Current (Note 5)	25°C		± 0.5			± 5.0			± 0.5			± 5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

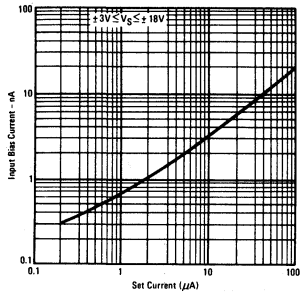
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

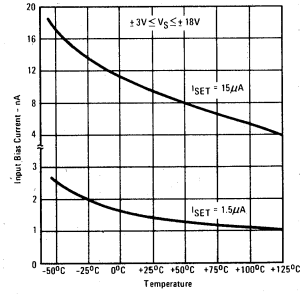
10. This parameter value based upon design calculations.

UNLESS OTHERWISE NOTED: $T_A = 25^0C$, $V_S = \pm 15VDC$

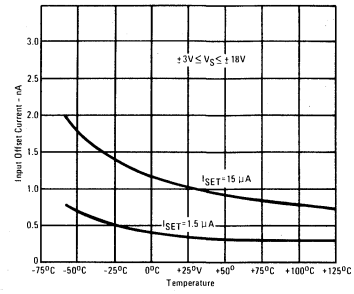
INPUT BIAS CURRENT
vs. SET CURRENT



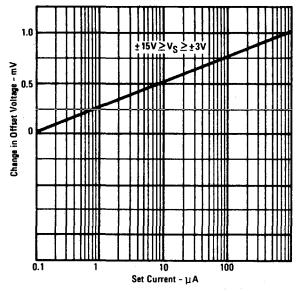
INPUT BIAS CURRENT
vs. TEMPERATURE



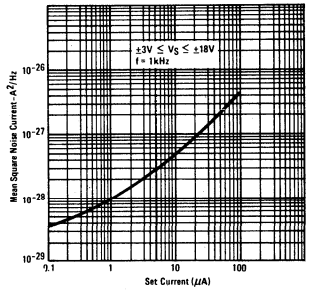
INPUT OFFSET CURRENT
vs. TEMPERATURE



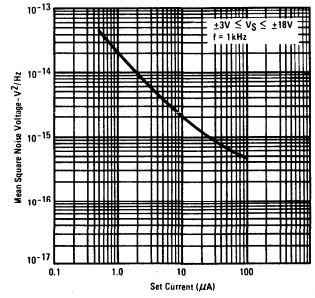
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



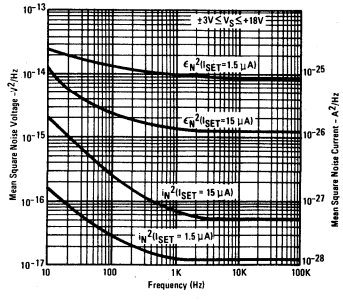
INPUT NOISE CURRENT
vs. I_{SET}



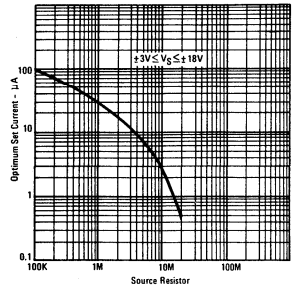
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



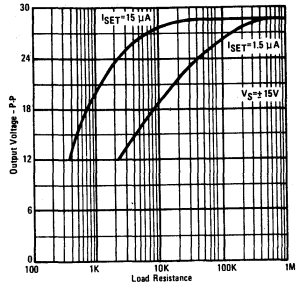
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



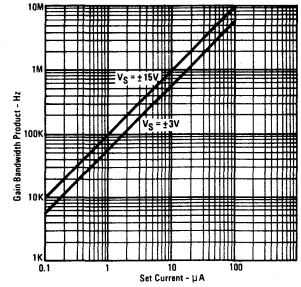
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

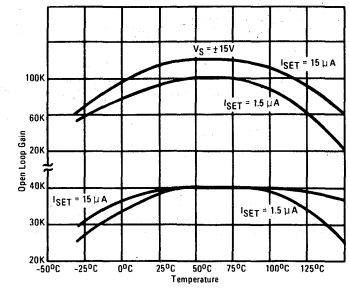
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



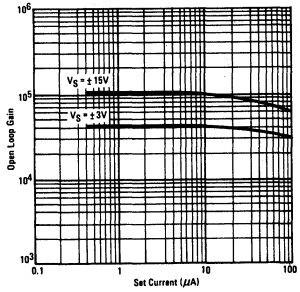
GAIN BANDWIDTH PRODUCT vs. I_{SET}



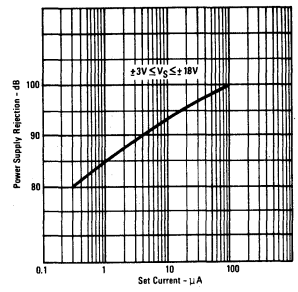
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



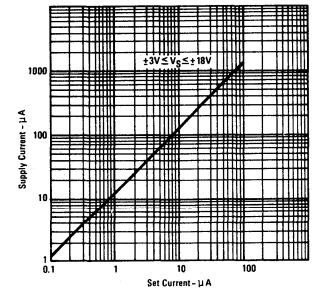
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



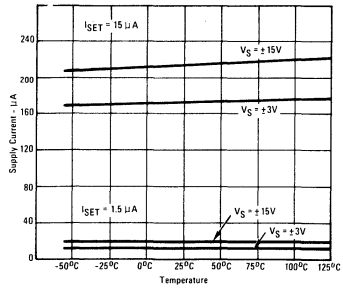
POWER SUPPLY REJECTION vs. I_{SET}



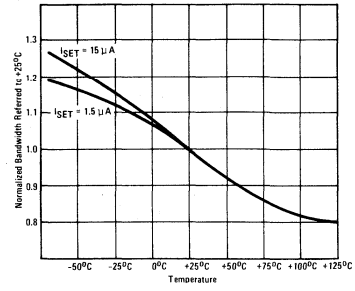
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE

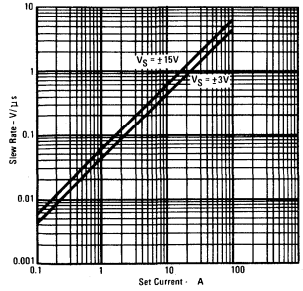


NORMALIZED BANDWIDTH vs. TEMPERATURE

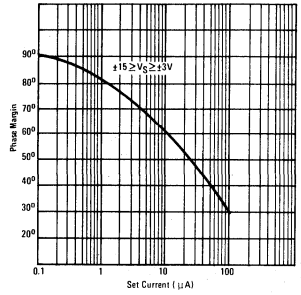


PERFORMANCE CURVES

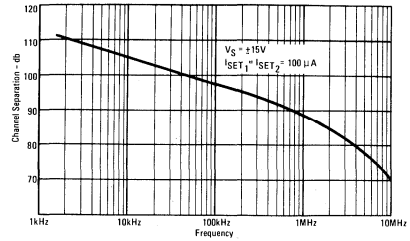
SLEW RATE vs. I_{SET}



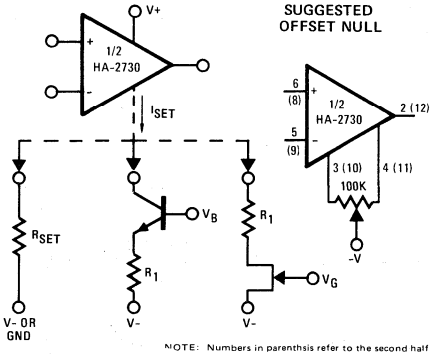
PHASE MARGIN vs. SET CURRENT



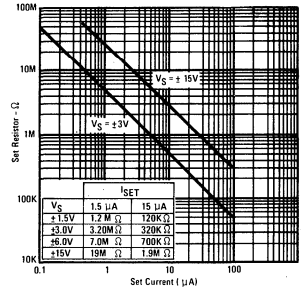
CHANNEL SEPARATION vs. FREQUENCY



TYPICAL BIASING CIRCUITS

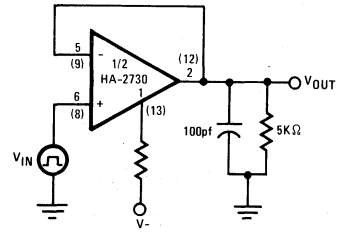


SET CURRENT VS. SET RESISTOR



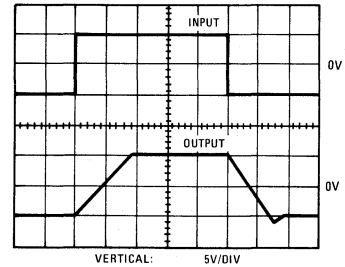
I_{SET}		
V_S	1.5 µA	15 µA
±1.5V	1.2 M Ω	120K Ω
±3.0V	3.20M Ω	320K Ω
±6.0V	7.0M Ω	700K Ω
±15V	19M Ω	1.9M Ω

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



NOTE: Numbers in parenthsis refer to the second half.

SLEWING WAVEFORM



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

HARRIS

HA-2740

Quad Programmable Operational Amplifier

Not Recommended For New Designs See HA-5144

FEATURES

- WIDE PROGRAMMING RANGE
  - ► SLEW RATE 0.06 to 6V/μs
  - ► BANDWIDTH 5KHz to 10MHz
  - ► BIAS CURRENT 0.4 to 50nA
  - ► SUPPLY CURRENT 1μA to 1.5mA
- WIDE POWER SUPPLY RANGE $\pm$1.2 to $\pm$18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

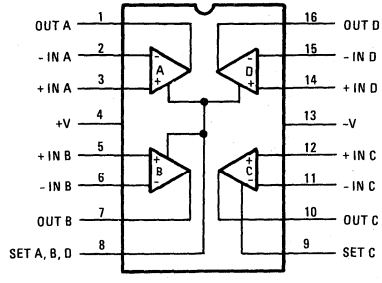
The Harris HA-2740 programmable amplifier is an internally compensated monolithic device offering a wide range of performance, that can be controlled by adjusting the circuit "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA-2740 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. The HA-2740 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting programming current.

A major advantage of the HA-2740 is that operating characteristics remain virtually constant over a wide supply range ($\pm$1.2V to $\pm$15V), allowing the amplifier to offer maximum performance in almost any system including battery-operated equipment. A primary application for the HA-2740 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, the HA-2740 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

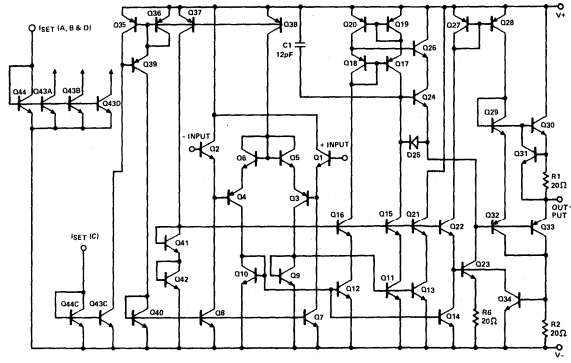
The HA-2740-2 is guaranteed over -55°C to +125°C. The HA-2740-5 is specified from 0°C to +75°C. Both parts are available in a 16 pin dual-in-line package.

PINOUT

TOP VIEW



SCHEMATIC



(1/4) HA-2740

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 3)	500mW
Differential Input Voltage	±30.0V	Maximum Junction Temperature	175°C
Input Voltage (Note 2)	±15.0V	Operating Temperature Range:	
I_{SET} (Current at I_{SET})	500μA	HA-2740-2	$-55°C \leq T_A \leq +125°C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ -2.0V \leq V_{SET} \leq V+$	HA-2740-5	$0°C \leq T_A \leq +75°C$
		Storage Temperature Range	$-65°C < T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = +3.0V, V- = -3.0V

		HA-2740-2 -55°C to +125°C						HA-2740-5 0°C to +75°C						
		I_{SET}=1.5μA			I_{SET}=15μA			I_{SET}=1.5μA			I_{SET}=15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 4)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 5 &12)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 6)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 4)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Channel Seperation (Note 7)	25°C		105			105			105			105		dB
Output Current (Note 8)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 9)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 9)	25°C		5			10			5			10		%
Slew Rate (Note 10)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 11)	Full			100			100			150			150	μV/V

SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = 15V D. C.

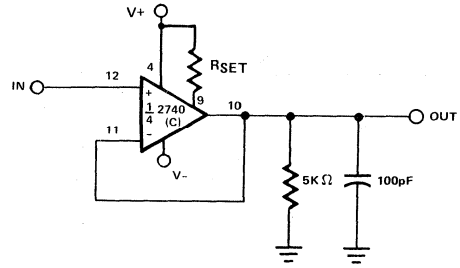
PARAMETER	TEMP.	HA-2740-2 -55°C to +125°C						HA-2740-5 0°C to 75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 4)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 5&12)	25°C	30	100K		30	120K		25K	100K		25K	120K		V/V
	Full	20			20			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 4)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Channel Separation (Note 7)	+25°C		105			105			105			105		dB
Output Current (Note 8)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K		500				2K		500			
Output Short-Circuit Current	25°C		3.7		19			3.7			19			mA
TRANSIENT RESPONSE														
Rise Time (Note 9)	25°C		2.0		0.2			2.0			0.2			μs
Overshoot (Note 9)	25°C		5		1.5			5			15			%
Slew Rate (Note 10)	25°C		0.1		0.8			0.1			0.8			V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		25			250			25			250		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 11)	Full			100			100			150			150	μV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. θ_{jA} = 97°C/W, θ_{jC} = 30°C/W.
4. This parameter based upon design calculations.
5. V_{SUPPLY} = ±3.0V, T=±25°C and Full; V_{SUPPLY} = ±15.0V, T=+25°C, T=Full; I_{SET} = 1.5μA, R_L = 75KΩ, R_L = 75KΩ; I_{SET} = 15μA, R_L = 5KΩ, R_L = 75KΩ
6. V_{CM} = ±1.5V; V_{CM} = ±5.0V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f=10kHz, V_{IN}=200mV peak to peak, Rs = 1KΩ.
8. V_O = ±2.0V; V_O = ±10.0V
9. ← AV = +1, V_{IN} = 200mV, R_L = 5K, C_L = 100pF →
10. V_O = ±2.0V; V_O = ±10.0V; R_L = 20K; R_L = 5K
11. ΔV = ±1.5V; ΔV = ±5.0V
12. V_O = ±1.0V; V_O = ±10.0V

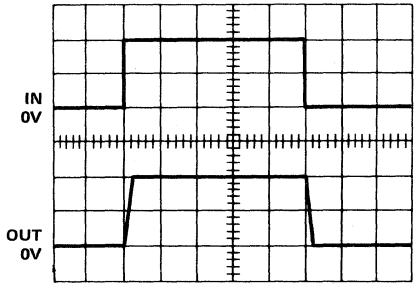
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



LARGE SIGNAL RESPONSE

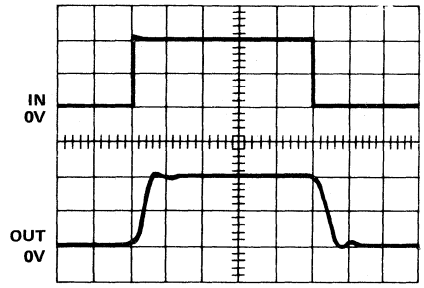
VOLTS: Input A: 5V/Div.,
Output B: 5V/Div.
TIME: 50μs/Div.



VERTICAL: 5V/Div.
HORIZONTAL: 50μs/Div.

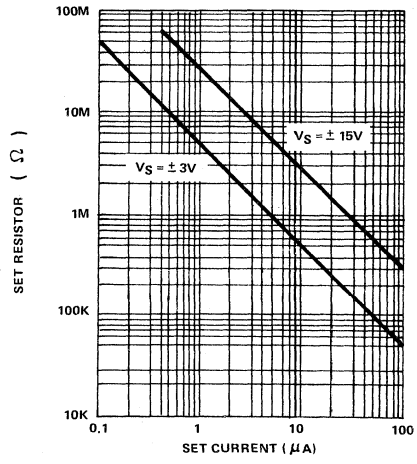
SMALL SIGNAL RESPONSE

VOLTS: Input A: 100mV/Div.,
Output B: 100mV/Div.
TIME: 1μs/Div.



VERTICAL: 100mV/Div.
HORIZONTAL: 1μs/Div.

SET CURRENT vs. SET RESISTOR

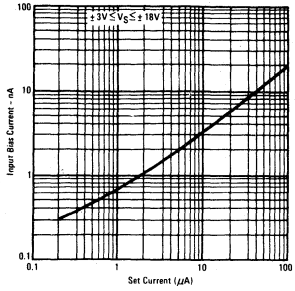


	ISET	
VS	1.5μA	15μA
± 1.5V	1.2MΩ	120KΩ
± 3.0V	3.20MΩ	320KΩ
± 6.0V	7.0MΩ	700KΩ
± 15V	19MΩ	1.9MΩ

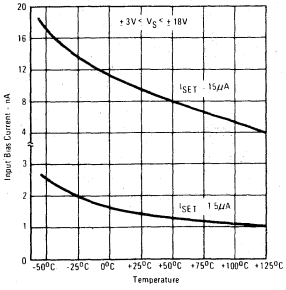
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

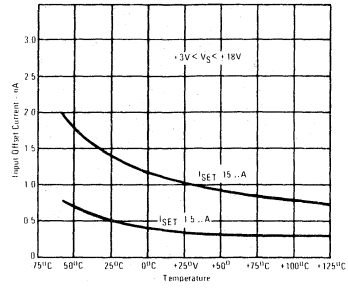
INPUT BIAS CURRENT vs. SET CURRENT



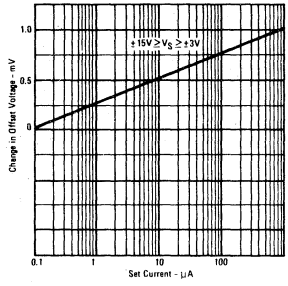
INPUT BIAS CURRENT vs. TEMPERATURE



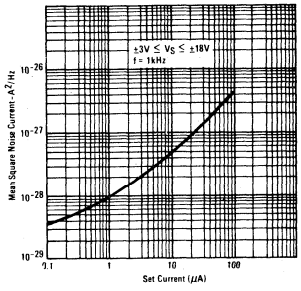
INPUT OFFSET CURRENT vs. TEMPERATURE



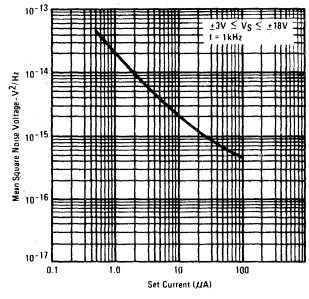
CHANGE IN OFFSET VOLTAGE vs. I_{SET} (UNNULLED)



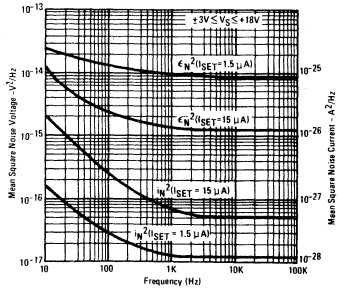
INPUT NOISE CURRENT vs. I_{SET}



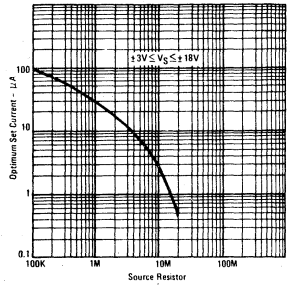
INPUT NOISE VOLTAGE vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY



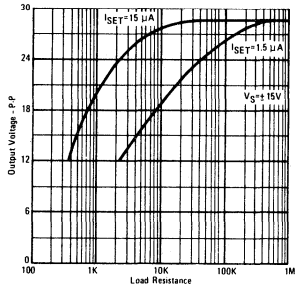
OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR



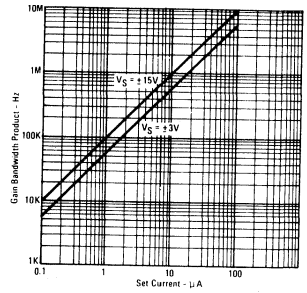
PERFORMANCE CURVES (Continued)

UNLESS OTHERWISE NOTED: $T_A = 25^0C$, $V_S = \pm 15VDC$

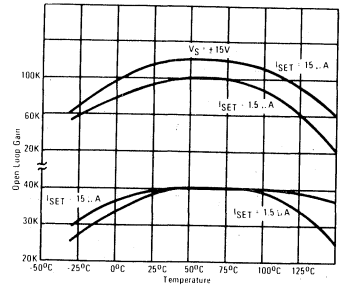
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



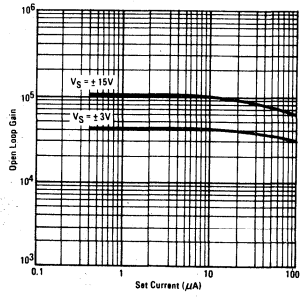
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



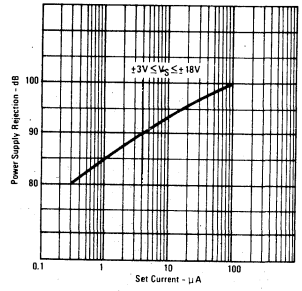
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



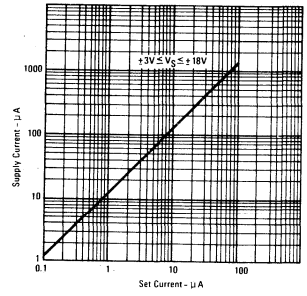
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



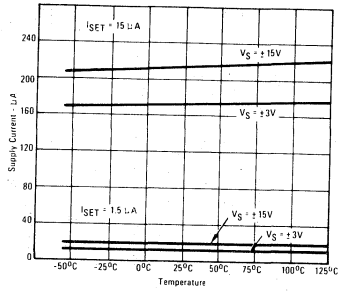
POWER SUPPLY REJECTION
vs. I_{SET}



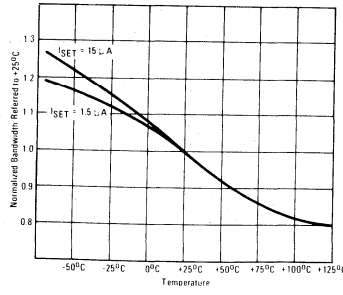
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE

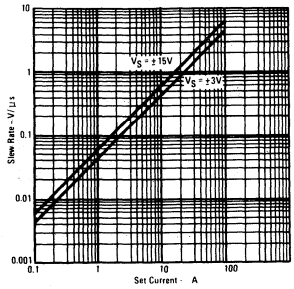


NORMALIZED BANDWIDTH
vs. TEMPERATURE

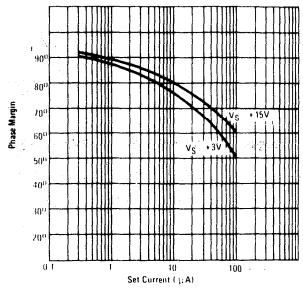


PERFORMANCE CURVES (Continued)

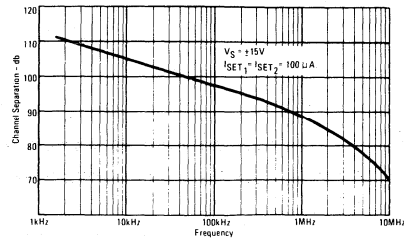
SLEW RATE vs. I_{SET}



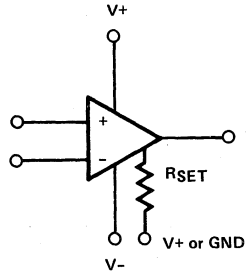
PHASE MARGIN vs. SET CURRENT



CHANNEL SEPARATION vs. FREQUENCY



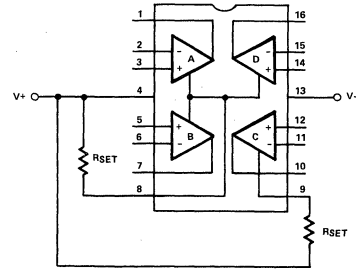
TYPICAL BIASING METHODS



A. DUAL SUPPLY, R_{SET} TO V+

$$I_{SET\,(A,B,D)} = I_{SET\,(A)} = I_{SET\,(B)} = I_{SET\,(D)}$$

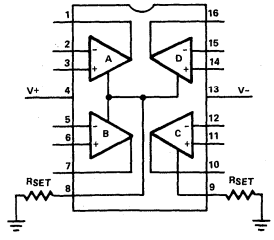
$$I_{SET} = \frac{\text{Total Supply Voltage} - .6V}{R_{SET}}$$



IF V- = 0V, Then $I_{SET} = \frac{V+ - .6V}{R_{SET}}$

B. DUAL SUPPLY, R_{SET} TO GROUND

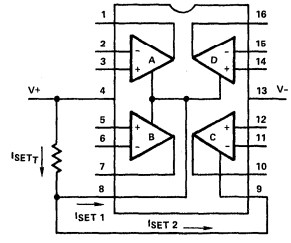
$$I_{SET} = \frac{|V-| - .6V}{R_{SET}}$$



C. MULTIPLE AMPLIFIER CONTROL USING SINGLE R_{SET}

$$I_{SET_T} = \frac{\text{Total Supply Voltage} - .6V}{R_{SET}}$$

$$I_{SET_{1...N}} = \frac{I_{SET_T}}{N}$$ where N = number of set pins tied together



$$I_{SET_{TOTAL}} = I_{SET1} + I_{SET2}$$

HARRIS

HA-4156

High Performance Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6 V/μS (TYP.)
- BANDWIDTH — 3.5 MHz (TYP.)
- INPUT VOLTAGE NOISE (f = 1KHz) — 9 NV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5 mV (TYP.)
- INPUT BIAS CURRENT — 60 nA (TYP.)
- SUPPLY RANGE — $\pm$2V to $\pm$20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

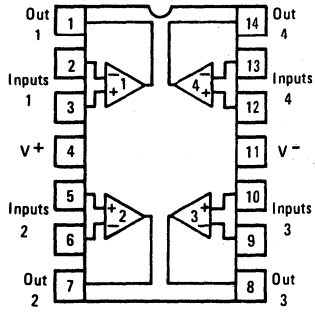
DESCRIPTION

The HA-4156 contains four general purpose operational amplifiers on a monolithic chip. The performance of each amplifier is equal to or better than the 741 type amplifier in all respects. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

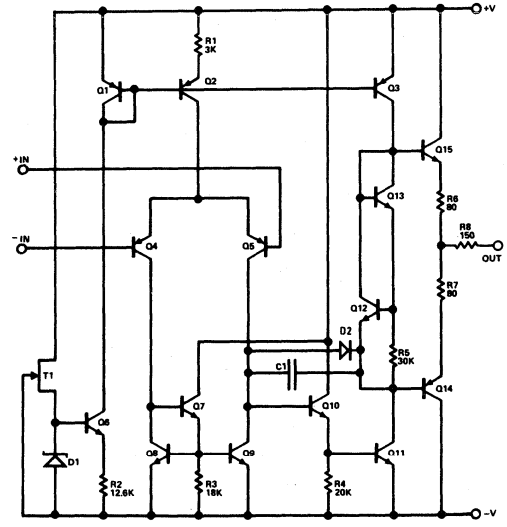
The HA-4156-5 is guaranteed over 0°C to +75°C.

PINOUT

TOP VIEW



SCHEMATIC



(¼) HA-4156

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 3)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-4156-5	$0°C \leq T_A \leq +75°C$
Input Voltage (Note 1)	±15.0V		
Output Short Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V kHz

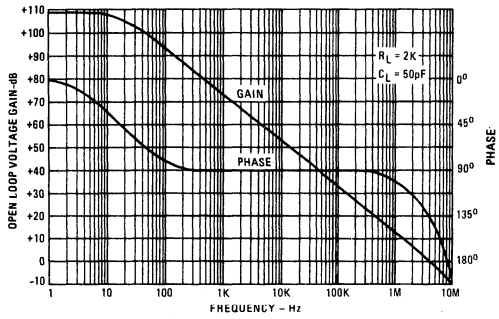
PARAMETER	TEMP.	HA-4156-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	Full		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5		µV/°C
Bias Current	+25°C		60	300	nA
	Full			400	nA
Offset Current	+25°C		30	50	nA
	Full			100	nA
Common Mode Range	Full	±12			V
Differential Input Resistance	+25°C		5		MΩ
Input Voltage Noise (f = 1kHz)	+25°C		9		$NV/\sqrt{Hz}$
(f = 20Hz to 20kHz)	+25°C		1.4	2.0	µVRMS
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 4)	+25°C	25K	50K		V/V
	Full	15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			dB
	Full	74			dB
Channel Separation (Note 5)	+25°C		-108		dB
Small Signal Bandwidth	+25°C	2.8	3.5		kHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C	20	25		kHz
Output Current (Note 6)	Full	±5	±15		mA
Output Resistance	+25°C		300		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		75	140	ns
Overshoot	+25°C		30	40	%
Slew Rate	+25°C	1.3	±1.6		V/µs
POWER SUPPLY CHARACTERISTICS					
Supply Current (I^+ or I^-)	+25°C			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

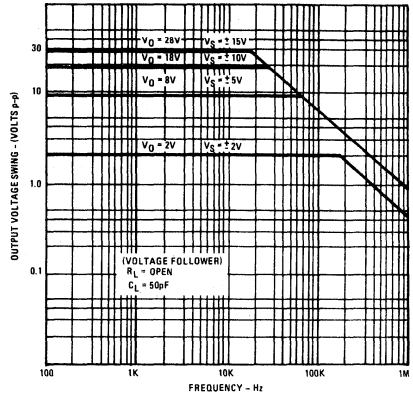
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = 25°C Unless Otherwise Stated.

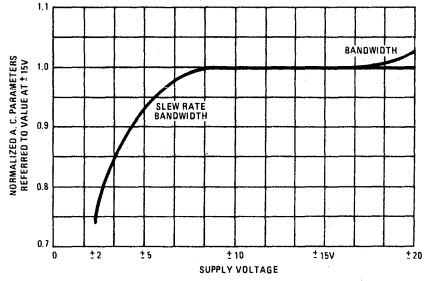
OPEN LOOP FREQUENCY RESPONSE



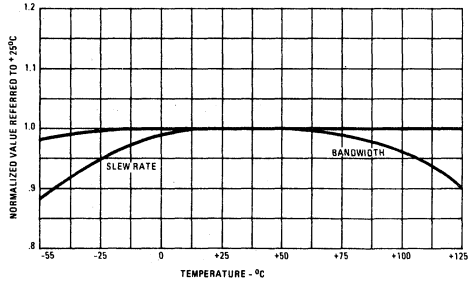
OUTPUT VOLTAGE SWING VS. FREQUENCY



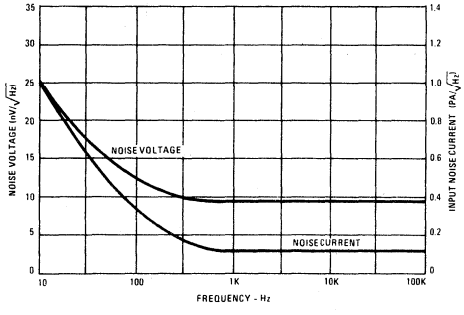
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



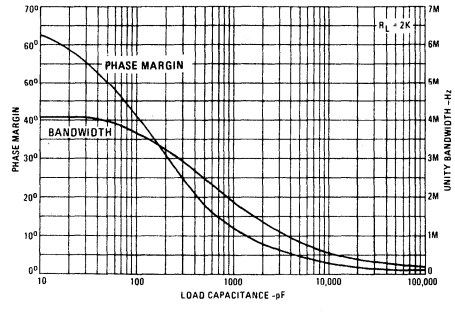
NORMALIZED AC PARAMETERS VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY

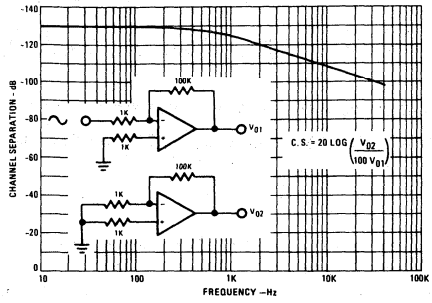


SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE

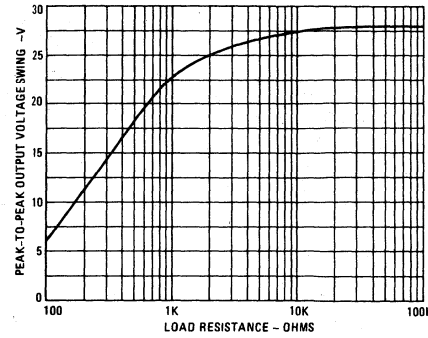


PERFORMANCE CURVES (cont'd.)

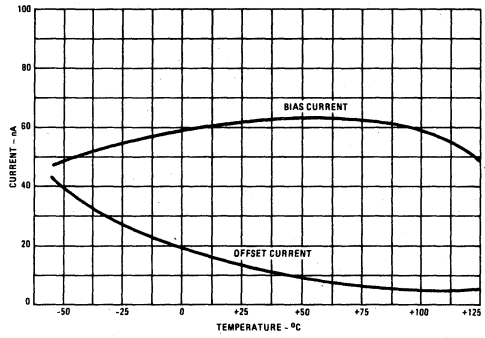
CHANNEL SEPARATION VS. FREQUENCY



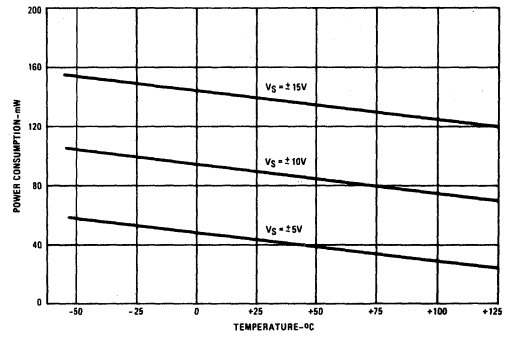
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

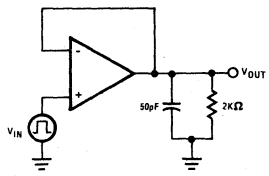


POWER CONSUMPTION VS. TEMPERATURE

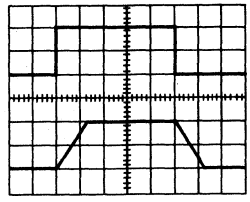


PULSE RESPONSE

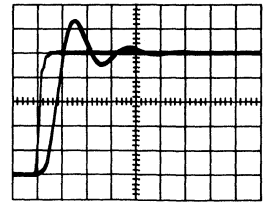
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5μs/Div)



TRANSIENT RESPONSE (Volts: 10mv/Div , Time: 100ns/Div)



HARRIS

HA-4600/02/05

High Performance Quad Operational Amplifier

Not Recommended For New Designs See HA-5104

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

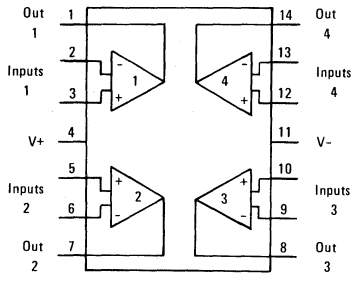
The HA-4600 series are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

A wide range of applications can be achieved by using the features made available by the HA-4600 series. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/ μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

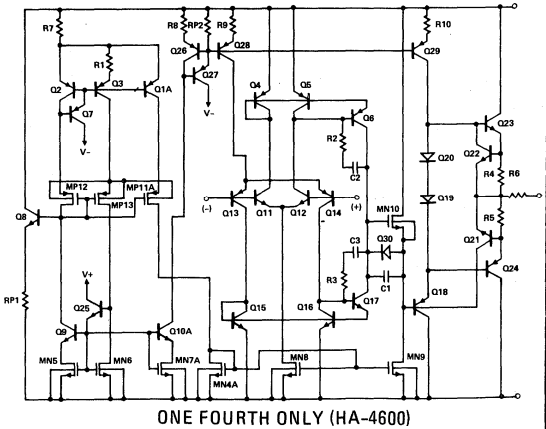
The HA-4600 series are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4600/4602-2 is specified from -55°C to +125°C and HA-4600/4605-5 is specified over 0°C to +75°C range.

PINOUT

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4600)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4600/4602-2	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4600/4605-5	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
		Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

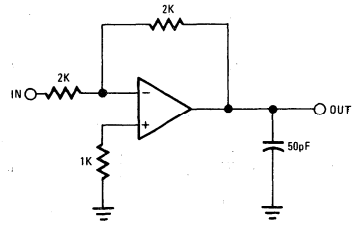
		HA-4600-2 HA-4600-5			HA-4602-2 HA-4605-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50	150		50	150	ns
Overshoot	+25°C		30	45		30	45	%
Slew Rate	+25°C	±2	±4		±1	±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

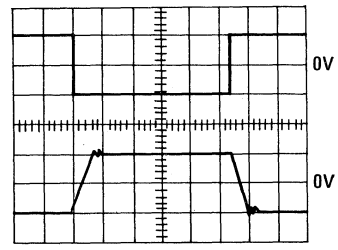
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

TEST CIRCUITS

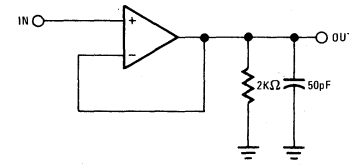
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

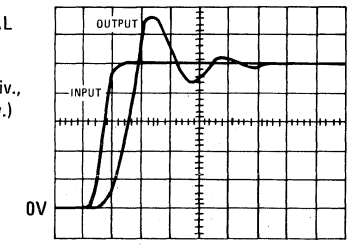




VERT. 5V/DIV.
HORZ. 5 μs/DIV.

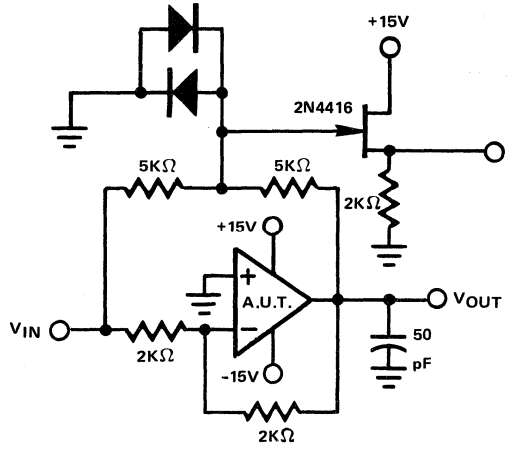
SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)





HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT

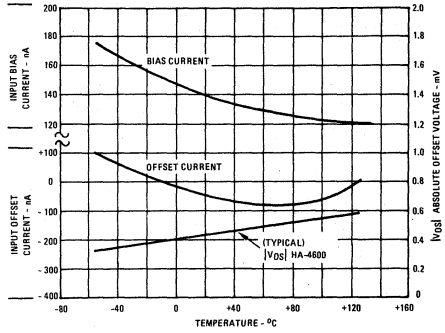


- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

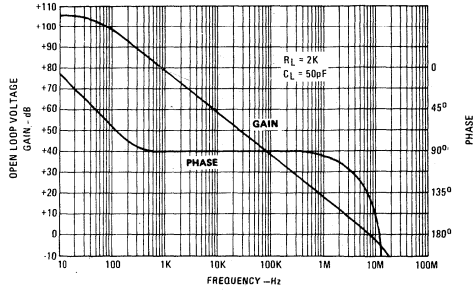
PERFORMANCE CURVES

$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$ Unless Otherwise Stated.

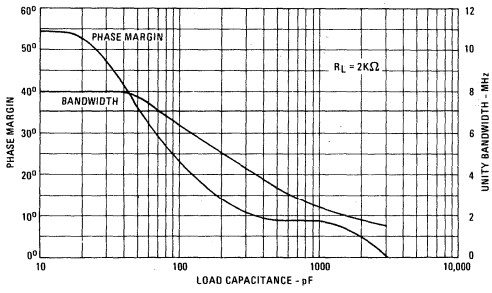
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



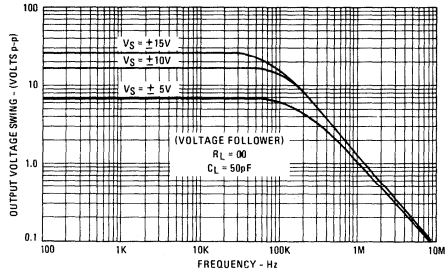
OPEN LOOP FREQUENCY RESPONSE



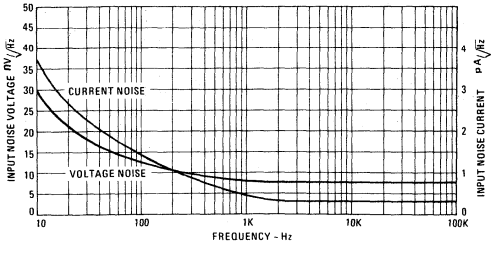
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



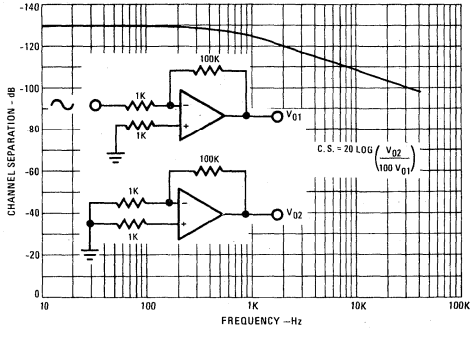
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



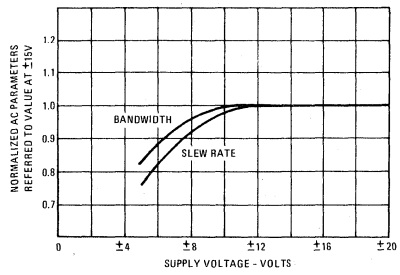
INPUT NOISE VS. FREQUENCY



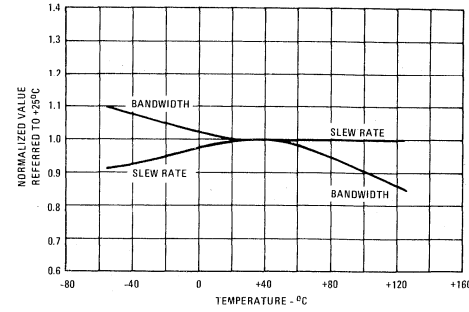
CHANNEL SEPARATION VS. FREQUENCY



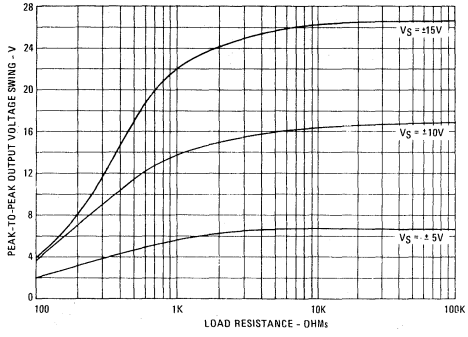
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



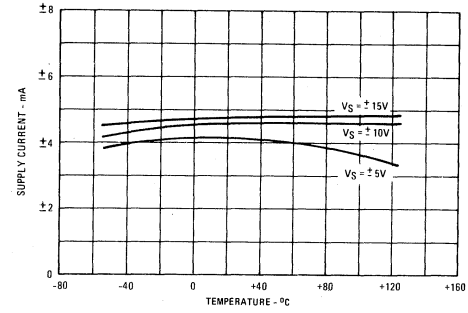
NORMALIZED AC PARAMETERS VS. TEMPERATURE



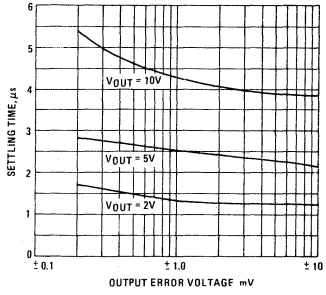
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



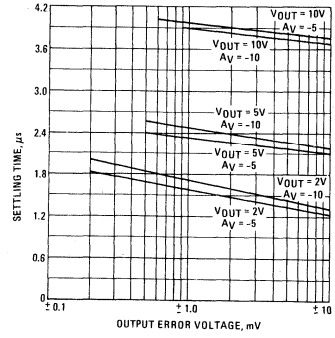
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



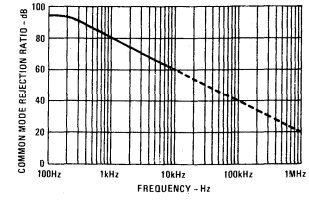
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



HA-4602 - COMMON MODE REJECTION RATIO VS. FREQUENCY



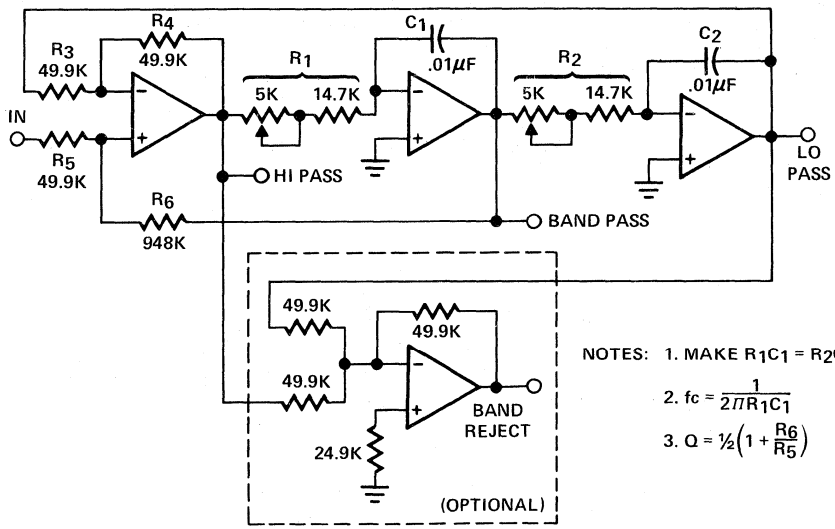
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

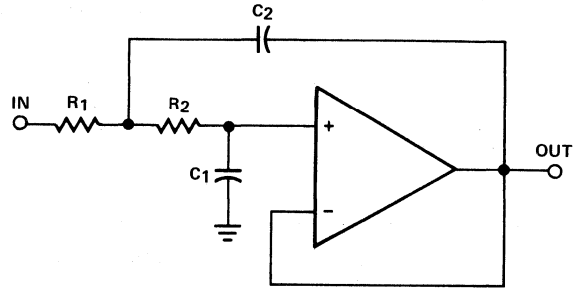
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

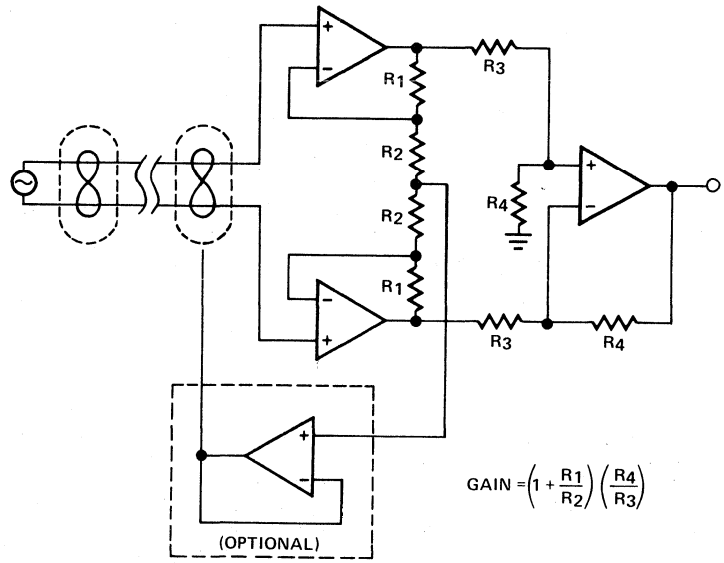
1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

HARRIS

HA-4620/22/25

Wideband, High Performance Quad Operational Amplifier

Not Recommended For New Designs See HA-5114

FEATURES

- Wide Gain Bandwidth Product — 70MHz
- High Slew Rate — ±20V/μs
- Low Offset Voltage — 0.3mV
- Fast Settling (0.01%, 10V Step) — 2.5μs
- Total Harmonic Distortion — <.01% to 30kHz
- Low Drift — 2μV/°C
- Low Power Consumption — 35mW/Amp
- Supply Range — ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

DESCRIPTION

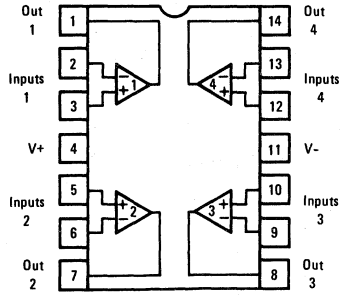
The HA-4620 series are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4620 series offers 0.3mW offset voltages and 2μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and $8nV\sqrt{Hz}$ noise voltage. For fast accurate data acquisition systems HA-4620 series offer 20V/μs slew rate and settling time of 2.5μsecs to 0.1% 10V step.

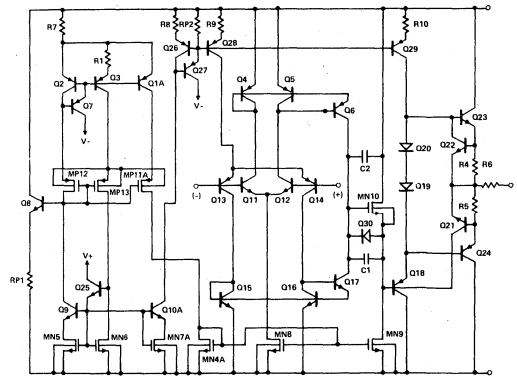
HA-4620 series are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. HA-4620/4622-2 is specified from -55°C to +125°C and HA-4620/4625-5 is specified over 0°C to +75°C range.

PINOUT

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4620)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C unless otherwise stated

Voltage between V+ and V- Terminals	40.0V
Differential Input Voltage	±7V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration (Note 3)	Indefinite
Power Dissipation (Note 4)	880mW
Operating Temperature Ranges:	
HA-4620/22-2	$-55^oC \leq T_A \leq +125^oC$
HA-4620/25-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

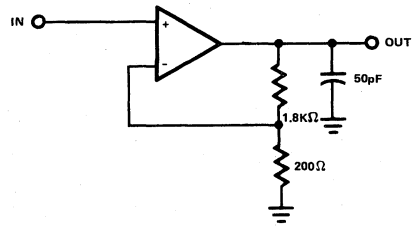
		HA-4620-2 HA-4620-5			HA-4622-2 HA-4625-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 9)	+25°C		260			260		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38	60		38		ns
Overshoot	+25°C		45	60		45		%
Slew Rate	+25°C	±12	±20		±12	±20		V/µs
Settling Time (Note 10)			2.5			2.5		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

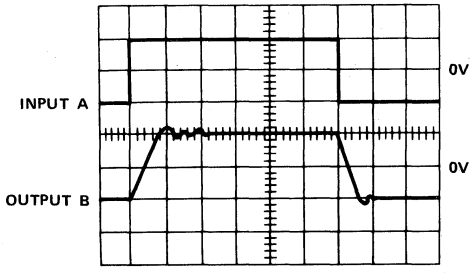
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages $< \pm$ 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/^{o}C above $T_A = +25^{o}C$.
5. $V_{OUT} = \pm 10V$, $R_L = 2K\Omega$
6. $\Delta V = \pm 5.0V$.
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; $R_S = 1k\Omega$. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. $A_V = 10$; $R_L = 2K$; $C_L \leq 10pF$.
9. Full power bandwidth is guaranteed by equation:
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V \text{ Peak}}$$
10. Output current is measured with $V_{OUT} = \pm 5V$.
11. Refer to Test Circuits section of the data sheet.
12. Setting time is measured to 0.1% of final value for a 1 volt input step, and $A_V = -10$.

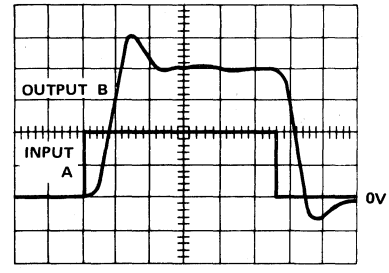
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



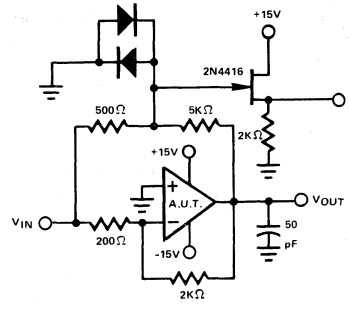


VOLTS: Input A: .5V/Div., Output B: 5V/Div.
TIME: 500ns/Div.



VOLTS: Input A: .01V/Div., Output B: 50mV/Div.
TIME: 50ns/Div.

SETTLING TIME CIRCUIT

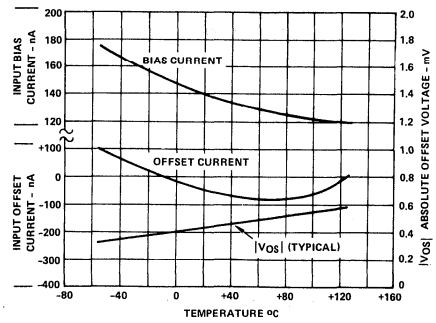


- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

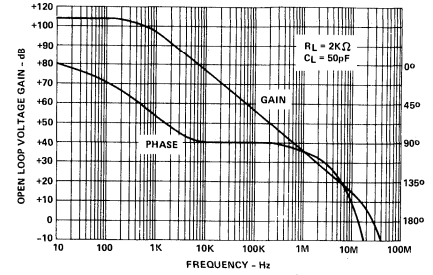
TYPICAL PERFORMANCE CURVES

V+ = +15V, T_A = +25°C Unless otherwise stated.

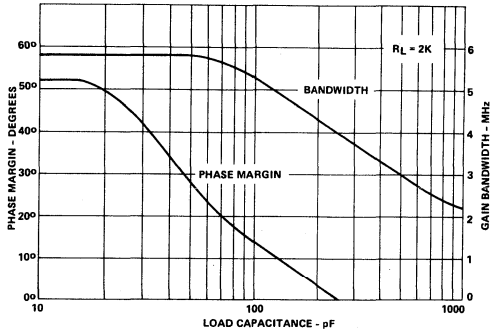
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



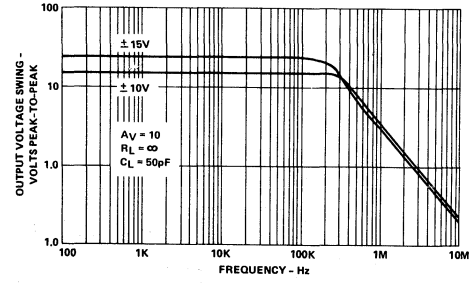
OPEN LOOP FREQUENCY RESPONSE



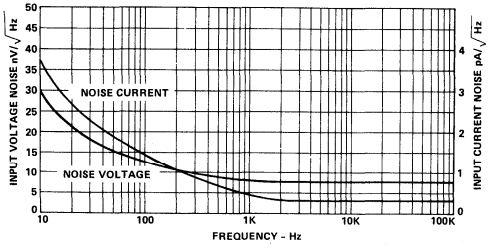
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



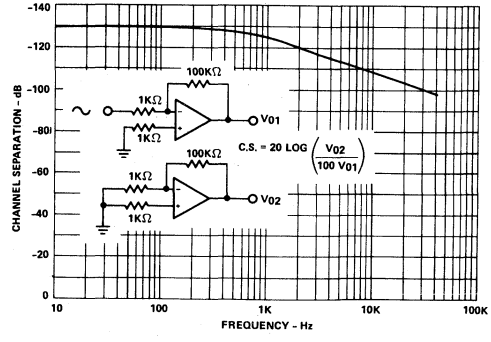
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



INPUT NOISE vs. FREQUENCY

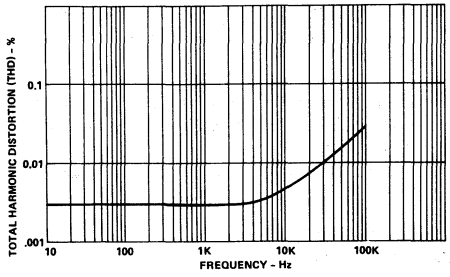


CHANNEL SEPARATION vs. FREQUENCY

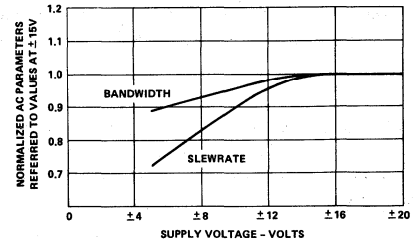


TYPICAL PERFORMANCE CURVES (Continued)

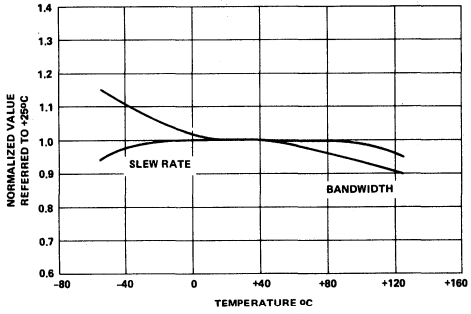
TOTAL HARMONIC DISTORTION VS. FREQUENCY



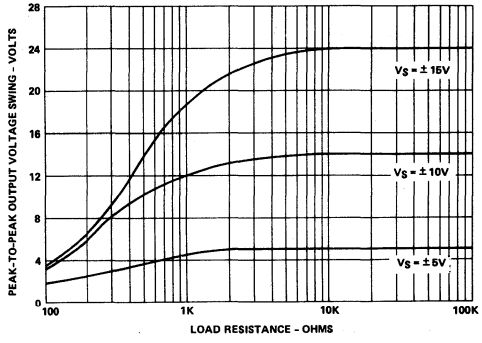
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



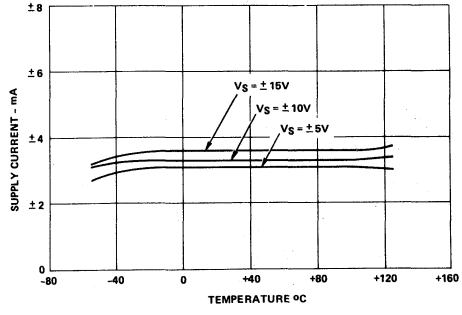
NORMALIZED AC PARAMETERS VS. TEMPERATURE



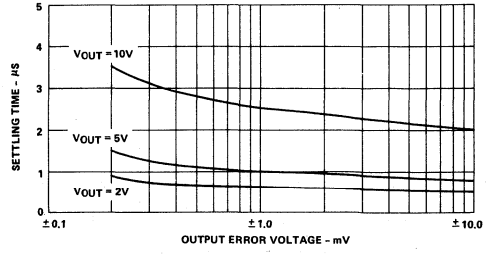
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -10)



APPLYING THE HA-4622/4625

1. POWER SUPPLY DISSIPATION: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible. If several amplifier sections are connected in series, it is recommended that every third or fourth section be decoupled.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a noninverting A_V = 10 configuration with the (+) input tied to ground in order to optimize performance of devices being used.

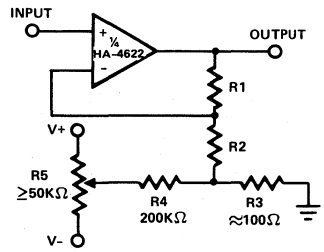
3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

4. When driving heavy capacitive loads (>100pF), a small value resistor should be connected in series with the output and inside the feedback loop.

APPLICATIONS

SUGGESTED METHODS FOR OFFSET NULLING

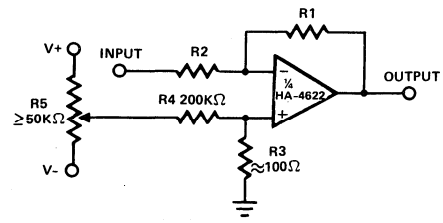
NON-INVERTING AMPLIFIER



NON-INVERTING AND INVERTING AMPLIFIERS RANGE OF ADJUSTMENT DETERMINED BY PRODUCT OF VSUPPLY AND R3/R4 RATIO

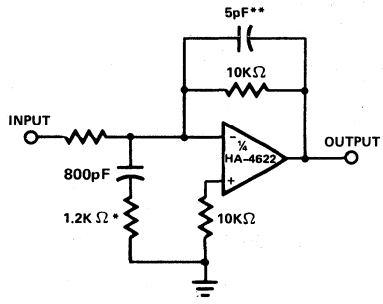
$$A_V = 1 + \frac{R1}{R2 + R3}$$

INVERTING AMPLIFIER

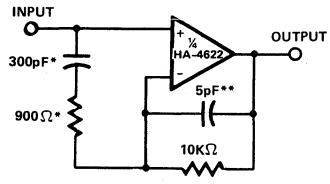


SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

INVERTING



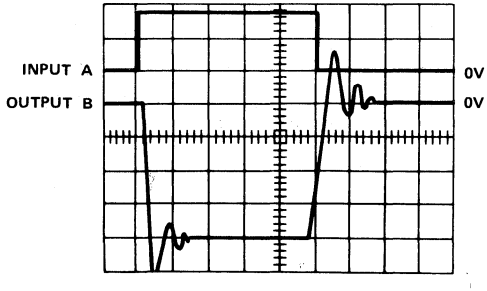
NON-INVERTING

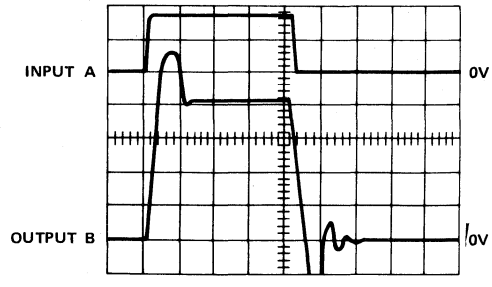


* VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME

** OPTIONAL

LARGE SIGNAL RESPONSE





VOLTS: Input A: 5V/Div., Output B: 2V/Div.
TIME: 1μs/Div.

HARRIS

HA-4640-1

High Temperature Quad Operational Amplifier

Preliminary

FEATURES

- CHARACTERIZED TO 300°C
- TESTED AT 200°C
- LOW INPUT OFFSET VOLTAGE 2mV
- BANDWIDTH 5MHz
- SLEW RATE 5V/μs
- STANDARD QUAD PINOUT

APPLICATIONS

- OIL WELL-LOGGING
- GEOTHERMAL WELL-LOGGING
- INDUSTRIAL PROCESS CONTROL
- ENGINE TESTING AND CONTROL

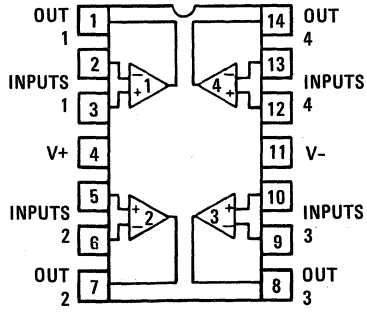
DESCRIPTION

The HA-4640-1 contains four general purpose operational amplifiers on a monolithic chip which was specifically designed to provide accurate signal processing capabilities for high temperature applications. The HA-4640-1 was designed and characterized for operation at ambient temperatures up to 300°C and is guaranteed-tested at 200°C (ambient). Typical applications for this amplifier include oil and geothermal well-logging instrumentation, industrial process control equipment, engine control and monitoring equipment and many other applications where operation in high temperature environments is required. The performance of each amplifier is equal to or better than 741 type amplifiers in most respects and is stable for closed loop gains greater than 10.

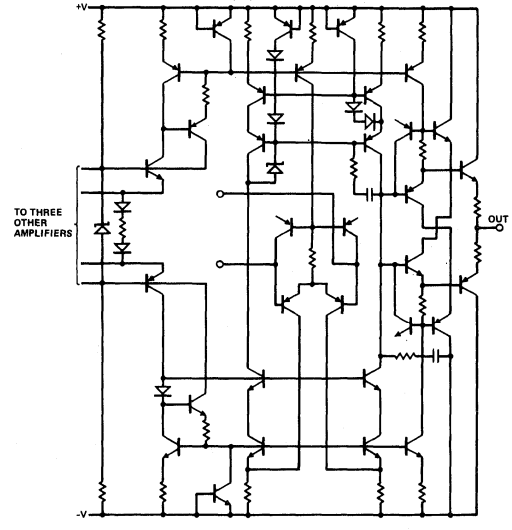
The HA-4640-1 is packaged in a 14-pin, hemetically sealed, cerdip with the standard quad op amp pinout shown below.

PINOUT

TOP VIEW



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V and V- Terminals	40.0V
Differential Input Voltage	±10V
Output Short Circuit Duration (Note 2)	Indefinite
Internal Power Dissipation	800mW
Operating Temperature Range	-55°C to 325°C
Storage Temperature Range	-65°C to 325°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

PARAMETER	TEMP.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
OFFSET VOLTAGE	-55°C to +25°C		2	8	mV
	200°C		4	12	mV
OFFSET VOLTAGE AVERAGE DRIFT	FULL		8		μV/°C
BIAS CURRENT	-55°C		1.5	5	μA
	25°C to 200°C		0.4	2	μA
OFFSET CURRENT	-55°C		0.5	2	μA
	25°C to 200°C		0.1	5	μA
COMMON MODE RANGE	FULL	±10	±13		V
DIFFERENTIAL INPUT SIGNAL	FULL			7	V
INPUT NOISE VOLTAGE (f = 1kHz)	25°C		8		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS					
LARGE SIGNAL VOLTAGE GAIN (R_L = 2K)	25°C to 200°C	20K	50K		V/V
(note 3) (R_L = 10K)	-55°C	20K	30K		V/V
COMMON MODE REJECTION RATIO (note 4)	25°C	80	100		dB
	FULL	60	80		dB
GAIN BANDWIDTH PRODUCT (A_V =10)	FULL	3	5		MHz
CHANNEL SEPARATION (note 5)	FULL	80	105		dB
OUTPUT CHARACTERISTICS					
OUTPUT VOLTAGE SWING (RL = 2K)	25°C to 200°C	±10	±12		V
(R_L = 10K)	-55°C	±10			
OUTPUT CURRENT (Vo = 10V)	25°C to 200°C	±5	8		mA
	-55°C	±1	±2		mA
TRANSIENT RESPONSE					
SLEW RATE (Vo = ±5V)	FULL	±2	±5		V/μs
POWER SUPPLY CHARACTERISTICS					
POWER SUPPLY REJECTION RATIO	FULL	70	86		dB
POWER SUPPLY CURRENT	FULL		5	8	mA

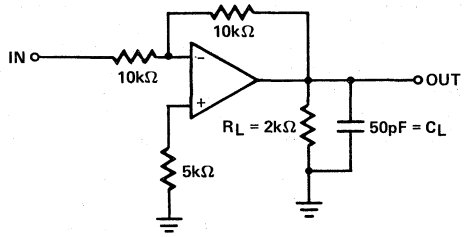
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Any one amplifier output may be shorted to ground indefinitely.
3. V_{OUT} = ±10V
4. ΔV = ±5V
5. Channel separation value is referred to the input of the amplifier. Input test conditions are f = 10KHz; V_{IN} = 200mV peak-to-peak; Rs = 1Kohms; A_{vcl} = 100.

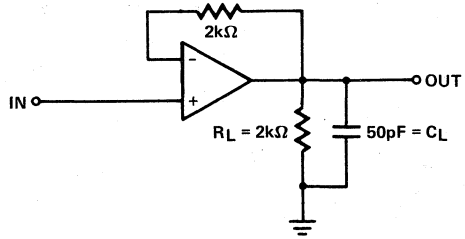
APPLICATION CIRCUITS

The HA-4640-1 is guaranteed to be stable for closed loop gains ≥ 10. However, when used in the unity gain configurations shown below the HA-4640-1 is capable of driving $2K\Omega/50pF$ loads and provide stable performance. When using low closed loop gains such as these, precautions should be taken to keep the input differential voltage below the 7.5V maximum to avoid degradation of the amplifier input stage. This is easily accomplished by either keeping the signal level below 7.5Vp-p or ensuring that the slew rate of the signal source is sufficiently low to guarantee a maximum differential input voltage of 7.5V.

INVERTING UNITY GAIN CONFIGURATION



UNITY GAIN BUFFER CONFIGURATION

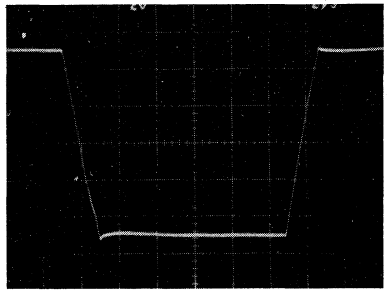


INVERTING CONFIGURATION

LARGE SIGNAL RESPONSE
(V_{IN} = +10 STEP, t_{RISE} = $t_{FALL} \approx 1\mu s$)

VERTICAL SCALE 5V/DIV.

HORIZONTAL SCALE 2μs/DIV.

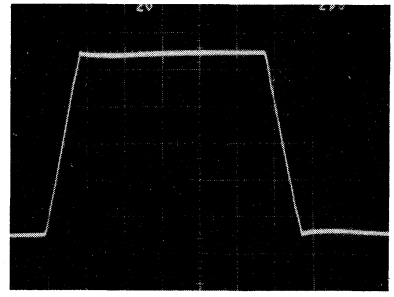


BUFFER CONFIGURATION

LARGE SIGNAL RESPONSE
(V_{IN} = +10V_{STEP}, t_{RISE} = $t_{FALL} \approx 1\mu s$)

VERTICAL SCALE 5V/DIV.

HORIZONTAL SCALE 2μs/DIV.

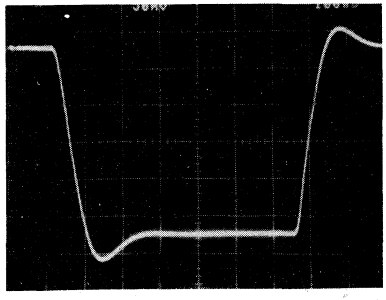


INVERTING CONFIGURATION

SMALL SIGNAL RESPONSE
(V_{IN} = +250mV STEP)

VERTICAL SCALE 50mV/DIV.

HORIZONTAL SCALE 100ns/DIV.

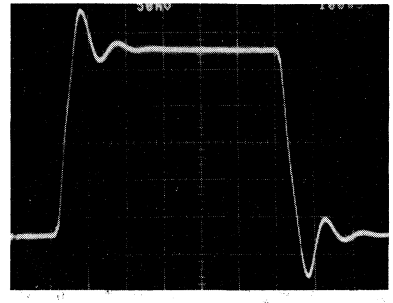


BUFFER CONFIGURATION

SMALL SIGNAL RESPONSE
(V_{IN} = +250mV STEP)

VERTICAL SCALE 50mV/DIV.

HORIZONTAL SCALE 100ns/DIV.



HARRIS

HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6V/μs (TYP.)
- BANDWIDTH — 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE — 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5mV (TYP.)
- INPUT BIAS CURRENT — 60nA (TYP.)
- SUPPLY RANGE — ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

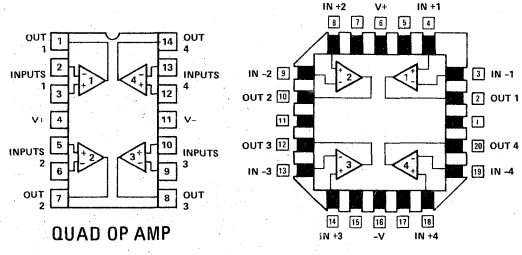
HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

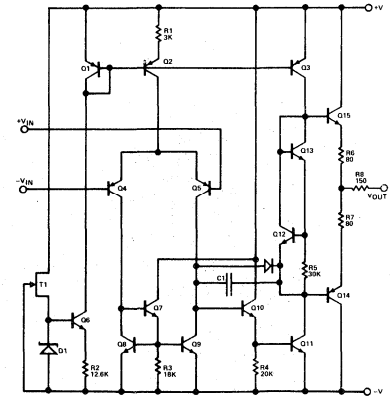
PINOUT

TOP VIEWS



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration (Note 2)	Indefinite
Power Dissipation For Epoxy Package. (Note 3)	880mW
Operating Temperature Range	
HA-4741-2	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-4741-5	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

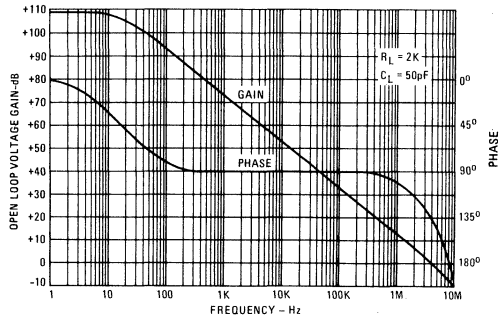
PARAMETER	TEMP.	HA-4741-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		4.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Voltage Noise (f = 1kHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
	+25°C	80			80			dB
Common Mode Rejection Ratio	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	-108		90	-108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 & 10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C			5.0			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K.
5. Referred to input; f = 10kHz, R_S = 1K.
6. V_{OUT} = ±10.
7. See Pulse Response Characteristics.
8. ΔV = ±5.0V.
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S. R./2π Vpeak.
10. R_L = 2K, C_L = 50pF.
11. V_{OUT} = ±200mV.
12. V_{OUT} = ±5V.

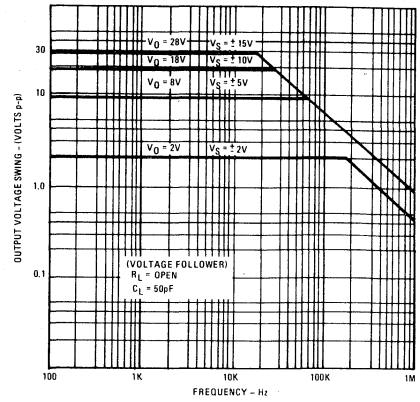
PERFORMANCE CURVES

$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

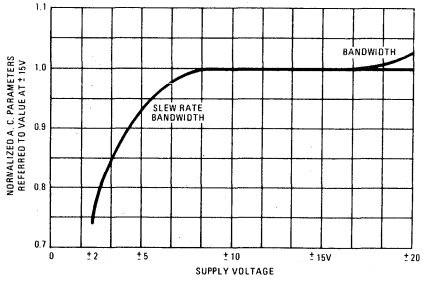
OPEN LOOP FREQUENCY RESPONSE



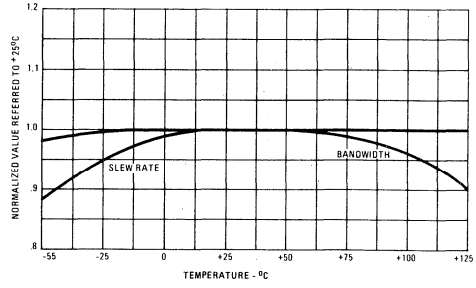
OUTPUT VOLTAGE SWING
VS. FREQUENCY



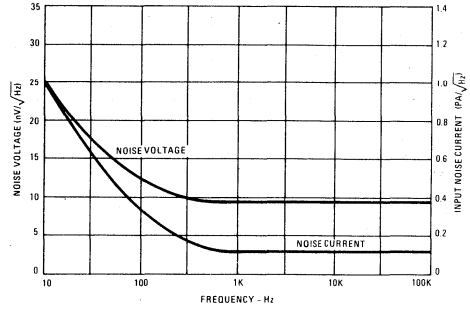
NORMALIZED AC PARAMETERS
VS. SUPPLY VOLTAGE



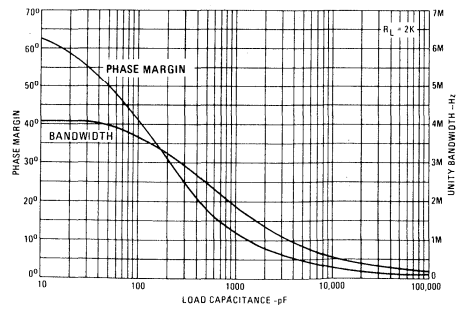
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY

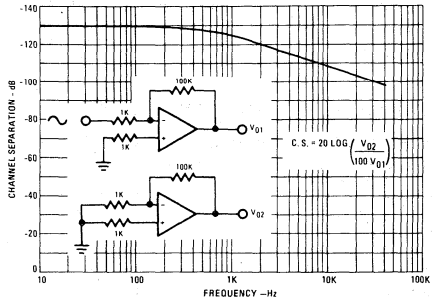


SMALL SIGNAL BANDWIDTH AND PHASE
MARGIN VS. LOAD CAPACITANCE

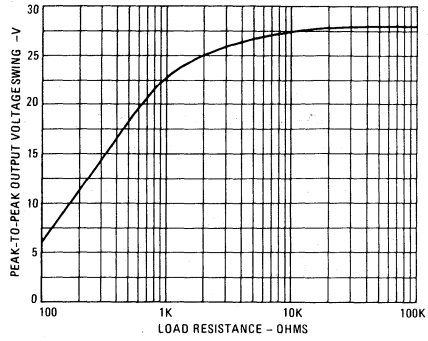


PERFORMANCE CURVES (Continued)

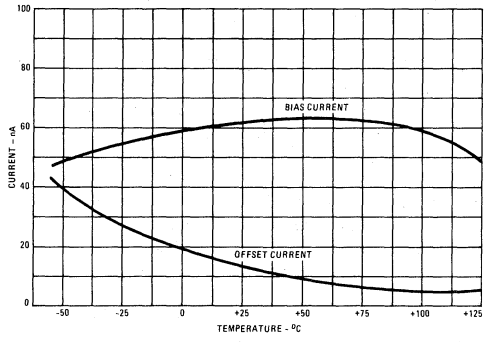
CHANNEL SEPARATION VS. FREQUENCY



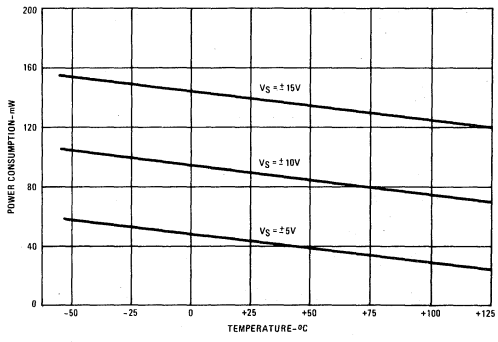
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

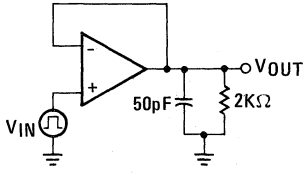


POWER CONSUMPTION VS. TEMPERATURE

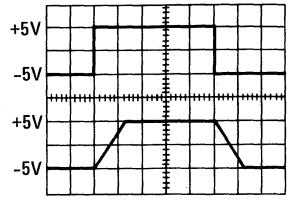


PULSE RESPONSE

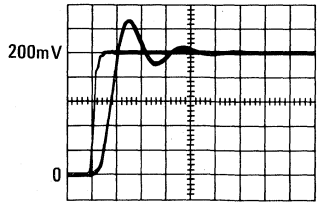
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5μs/Div)



TRANSIENT RESPONSE (Volts: 40mV/Div., Time: 100ns/Div.)



HA-4900/02/05

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

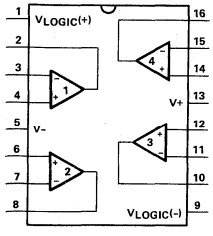
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

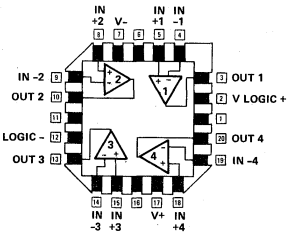
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range.

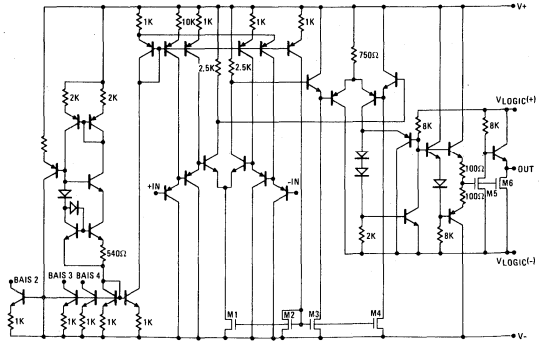
PINOUTS

TOP VIEWS





SCHEMATIC



ONE FOURTH ONLY (HA-4900 SERIES)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	880mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V- = -15.0V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = GND.

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			35			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		V+ -2.4	V-		V+ +2.4	V-		V+ +2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	20		6.5	20		7	20	mA
Supply Current , I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		2.0	4		2.0	4		2.0	4	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Minimum differential input voltage required to ensure a defined output state.

3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.

4. $R_S \leq 200$ ohms; $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter inludes the effects of offset voltage, offset current, common mode rejection, and voltage gain.

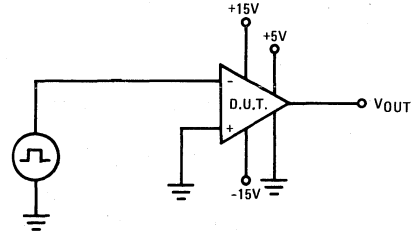
5. For $T_{pd}(1)$; 100mV input step, -5mV overdrive. For $T_{pd}(0)$; -100mV input step, 5mV overdrive. Frequency $\approx$ 100Hz; Duty Cycle $\approx$ 50%; Inverting input driven. See Test Circuit below.

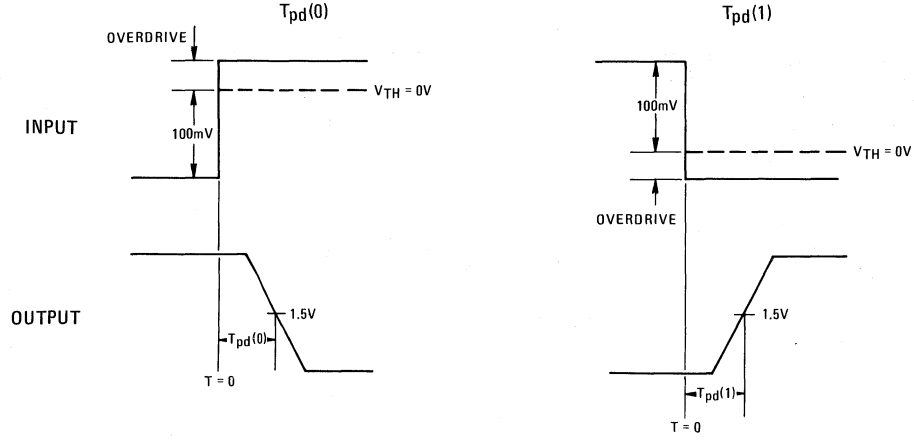
6. For V_{OH} and V_{OL}: $I_{Sink} = I_{Source} = 3.0$mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.

7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW which allows operation to +125°C; the combination +15V, -15V, 0V gives a T.P.D. of 450mW and an operating limit of T_A = +95°C.

8. Derate by 5.8mW/°C above T_A = +75°C.

RESPONSE TIME TEST CIRCUITS



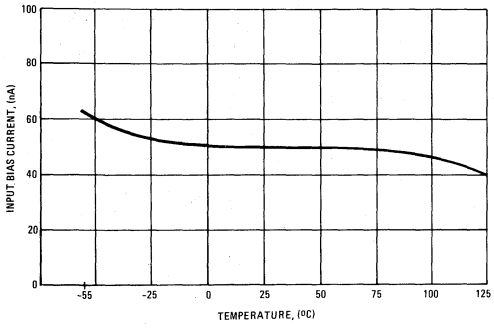


For input and output voltage waveforms for various input overdrives see Performance Curves.

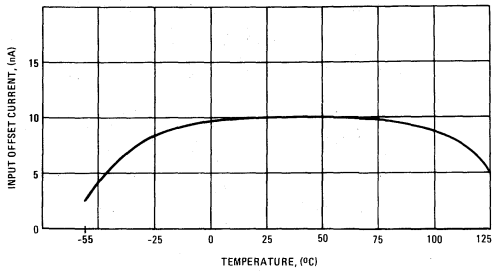
PERFORMANCE CURVES

$V+ = 15V$, $V- = -15V$, $V_{Logic}(+) = 5.0V$, $V_{Logic}(-) = 0V$, $T_A = +25^oC$, Unless Otherwise Stated.

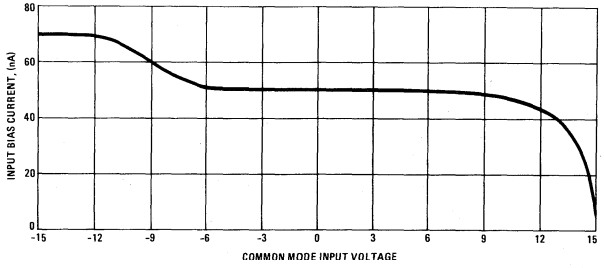
INPUT BIAS CURRENT vs. TEMPERATURE



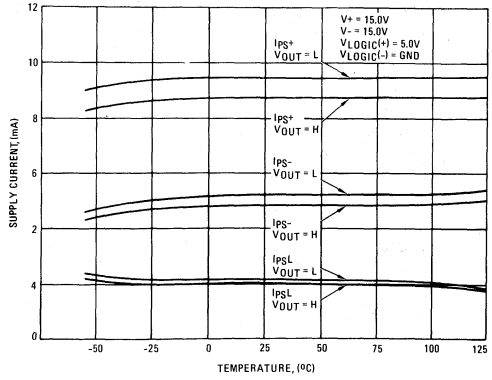
INPUT OFFSET CURRENT vs. TEMPERATURE



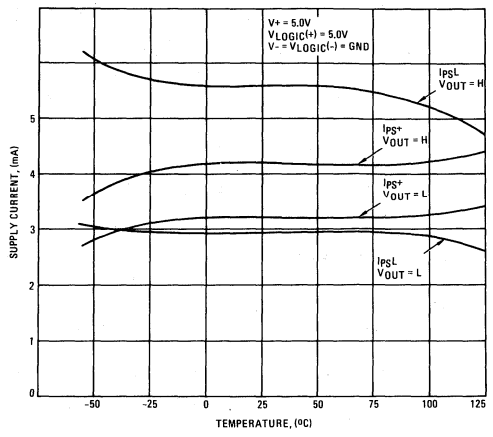
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.} = 0V$)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

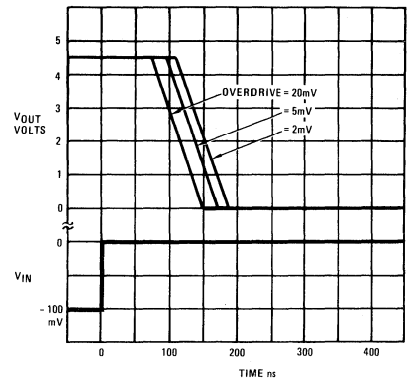


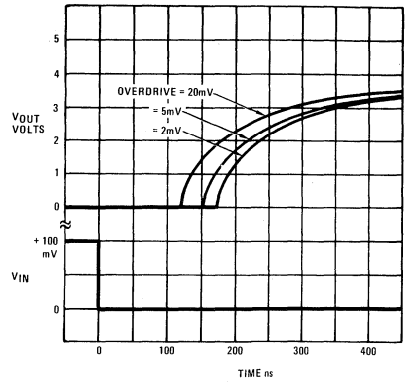
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



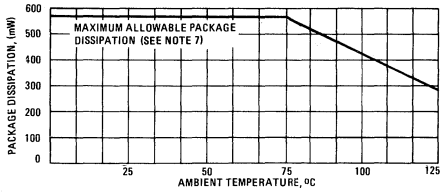
PERFORMANCE CURVES (Continued)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

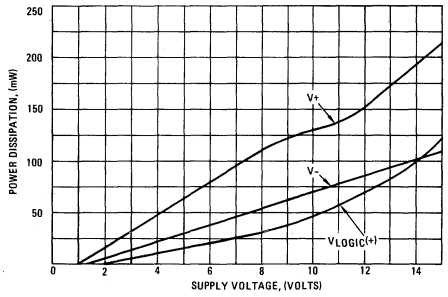




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900 SERIES COMPARATORS

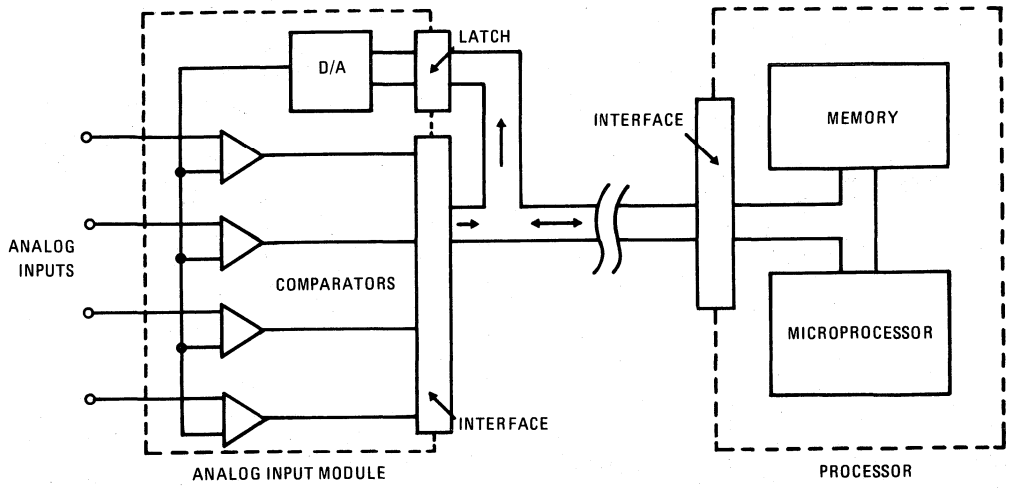
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to $<$ 5mA since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

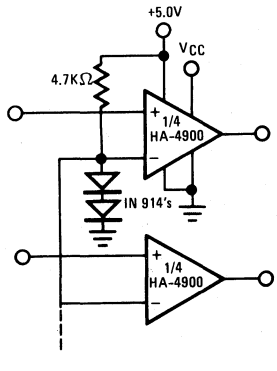
5. RESPONSE TIME: Fast rise time ($<$ 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.



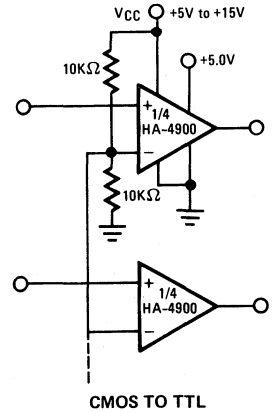
DATA ACQUISITION SYSTEM

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS

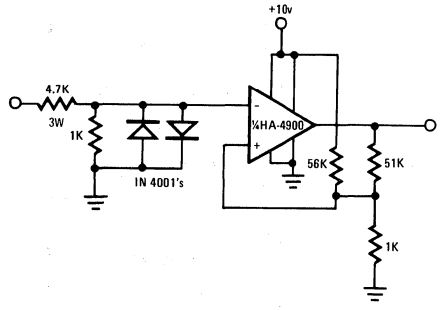


CMOS TO TTL

LOGIC LEVEL TRANSLATORS

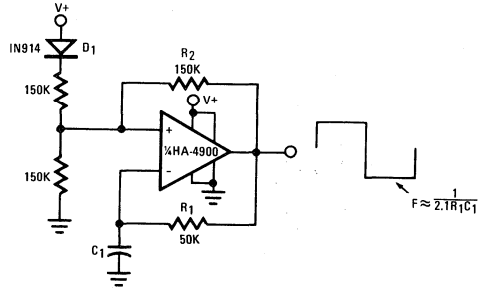
The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for V- and V_{Logic}-, these logic level translators will tolerate several volts of ground line differential noise.



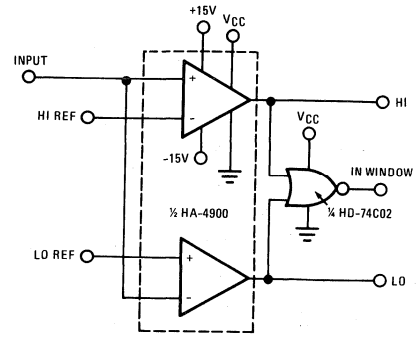
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



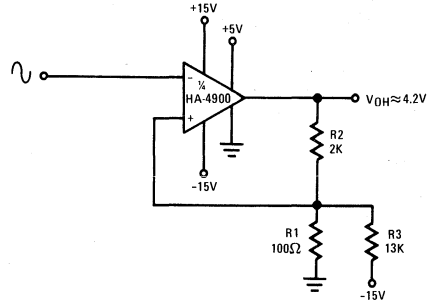
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



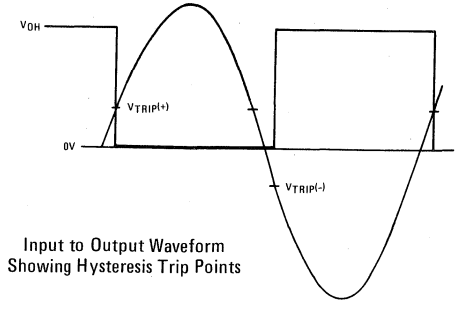
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

HARRIS

HA-5033

Video Buffer

FEATURES

- DIFFERENTIAL PHASE ERROR 0.1°
- DIFFERENTIAL GAIN ERROR 0.1%
- HIGH SLEW RATE (±15V) 1300V/μs
- WIDE BANDWIDTH (SMALL SIGNAL) 250MHz
- WIDE POWER BANDWIDTH DC to 65MHz
- FAST RISE TIME 3ns
- HIGH OUTPUT DRIVE ±10V WITH 100Ω LOAD
- WIDE POWER SUPPLY RANGE ±5V TO ±16V
- REPLACE COSTLY HYBRIDS

APPLICATIONS

- VIDEO BUFFER
- HIGH FREQUENCY BUFFER
- ISOLATION BUFFER
- HIGH SPEED LINE DRIVER
- IMPEDANCE MATCHING
- CURRENT BOOSTERS
- HIGH SPEED A/D INPUT BUFFERS

DESCRIPTION

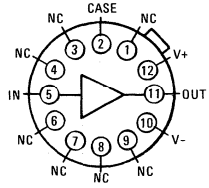
The HA-5033 is a unity gain monolithic I. C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce PNP transistors of lower frequency response, which results in a lower AC performance.

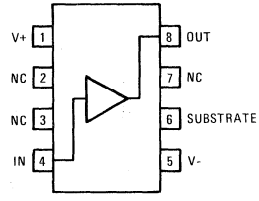
The HA-5033 is available in a 12 pin (TO-8) metal can or an 8 pin epoxy mini-dip. The HA-5033-2 is specified over the military temperature range of -55°C to +125°C. The HA-5033-5 is specified over the commercial temperature range of 0°C to +75°C.

PINOUTS

TOP VIEWS

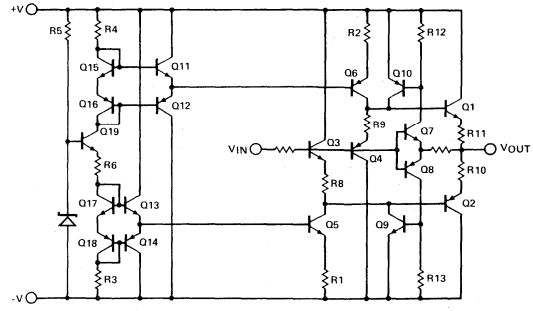


METAL CAN PACKAGE



MINI-DIP

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- pins	40V	Maximum Junction Temperature	200°C
Input Voltage	Equal to Supplies	Operating Temperature Range HA-5033-2	-55°C≤TA≤+125°C
Output Current (Peak)	±200mA	HA-5033-5	0°C≤TA≤+75°C
Internal Power Dissipation (Note 2)		Storage Temperature Range	-65°C≤TA≤+150°C
TO-8 (+25°C)	1.75W		
Mini-dip (+25°C)	1.95W		

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, unless otherwise specified.

PARAMETER	TEMP	-55°C TO +125°C			0°C TO +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	15		5	15	mV
	Full		6	25		6	25	mV
Average Offset Voltage Drift	Full		33			33		µV/°C
Bias Current	+25°C		20	35		20	35	µA
	Full		30	50		30	50	µA
Input Resistance	+25°C		1.5			1.5		MΩ
Input Capacitance	+25°C		1.6			1.6		pF
Input Noise Voltage (Note 3)	+25°C		20			20		µVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain $R_L = 100\Omega$	+25°C	.93			.93			V/V
$RL = 1K\Omega$	+25°C		.99			.99		V/V
$R_L = 100\Omega$	Full	.92			.92			V/V
-3dB Bandwidth	+25°C		250			250		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
$R_L = 100\Omega$	Full		±10			±10		V
$R_L = 1K\Omega$ (Note 4)	Full		±11			±11		V
Output Current	+25°C		±100			±100		mA
Output Resistance	+25°C		5			5		Ω
Full Power Bandwidth (Note 5)	+25°C		65			65		MHz
TRANSIENT RESPONSE								
Rise Time (Note 6)	+25°C		3			3		ns
Propagation Delay	+25°C		1			1		ns
Overshoot	+25°C		10			10		%
Slew Rate (Note 7)	+25°C	1.0	1.3		1.0	1.3		V/ns
Settling Time to .1%	+25°C		50			50		ns
Differential Phase Error (Note 8)	+25°C		.1			.1		degrees
Differential Gain Error (Note 8)	+25°C		.1			.1		%
POWER REQUIREMENTS								
Supply Current	+25°C		21	25		21	25	mA
	Full		21	30		21	30	mA
Power Supply Rejection Ratio	Full	54			54			dB
Harmonic Distortion (Note 9)	+25°C		<0.1			<0.1		%

NOTES

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. TO-8: θ_{JA} = 99°C/W, θ_{JC} = 31°C/W

   Recommended Heat Sinks for the TO-8:
   Thermalloy 2240A, θ_{SA} = 27°C/W
   IERC Up-TO8-48CB, θ_{SA} = 10°C/W

   Mini-dip: θ_{JA} = 90°C/W θ_{JC} = 27°C/W

3. 10Hz to 1MHz

4. $\pm V_{SUPPLY}$ ±15V.

5. V_O = 1 V_{RMS}, R_L = 1KΩ

6. V_O = 500mV

7. $\pm V_{SUPPLY}$ = ±15V, V_O = ±10V, R_L = 1KΩ.

8. Differential gain and phase error are non-linear signal distortions found in video systems and are defined as follows:

   Differential Gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level.

   Differential Phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level.

   Differential gain and phase error were too small to be measured with a Tektronix 520A NTSC Vector Scope.

9. V_{IN} = 1 V_{RMS}

OPERATING INSTRUCTIONS

LAYOUT CONSIDERATIONS

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin # 2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the epoxy mini-dip, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

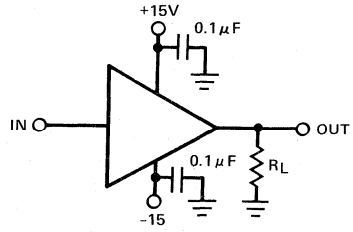
POWER SUPPLY DECOUPLING

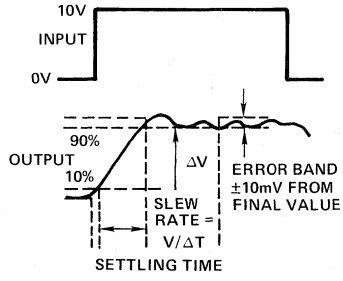
For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from .01 to .1 μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance.

It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

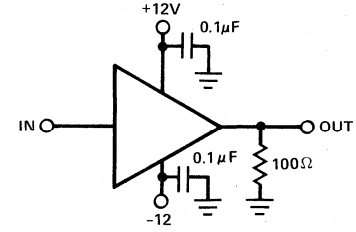
TEST CIRCUITS

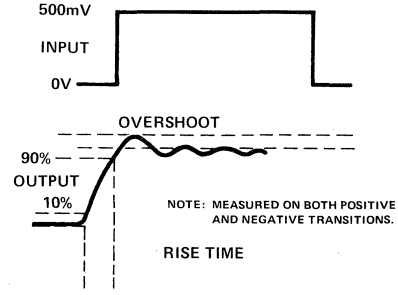
SLEW RATE AND SETTLING TIME



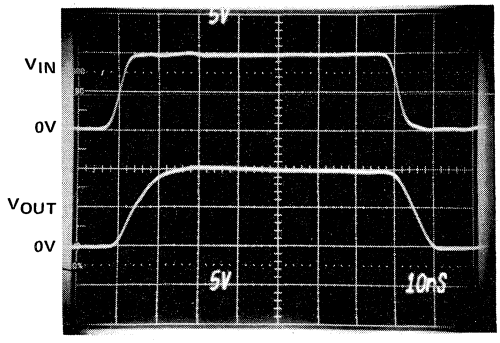


TRANSIENT RESPONSE

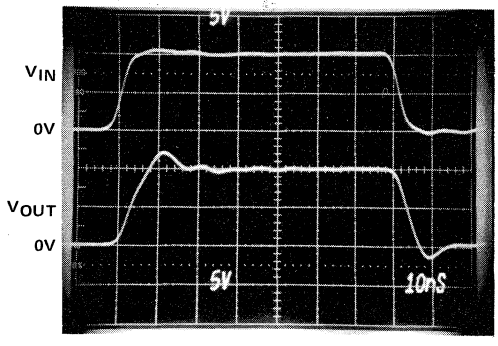




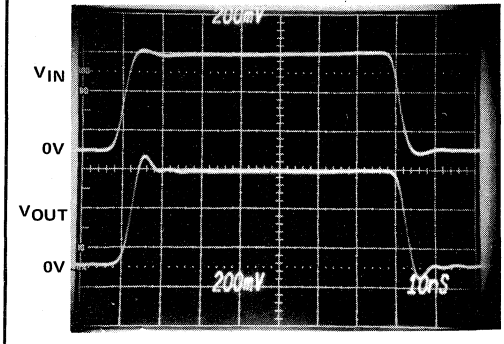
+10V RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$



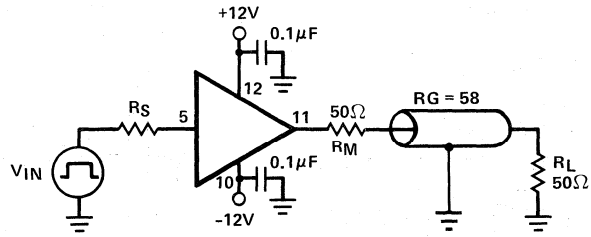
+10V RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 1K\Omega$



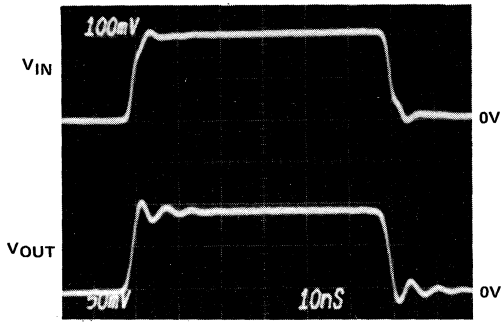
+0.5V PULSE RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$



TYPICAL APPLICATIONS



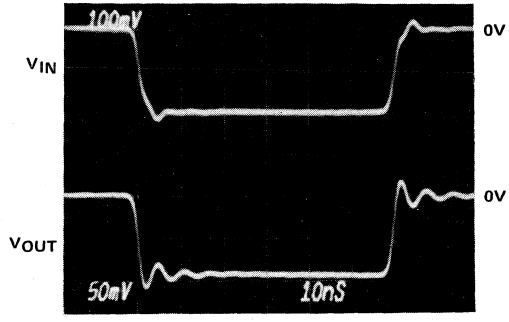
APPLICATION 1. VIDEO COAXIAL LINE DRIVER - 50Ω SYSTEM



POSITIVE PULSE RESPONSE

$T_A = +25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$

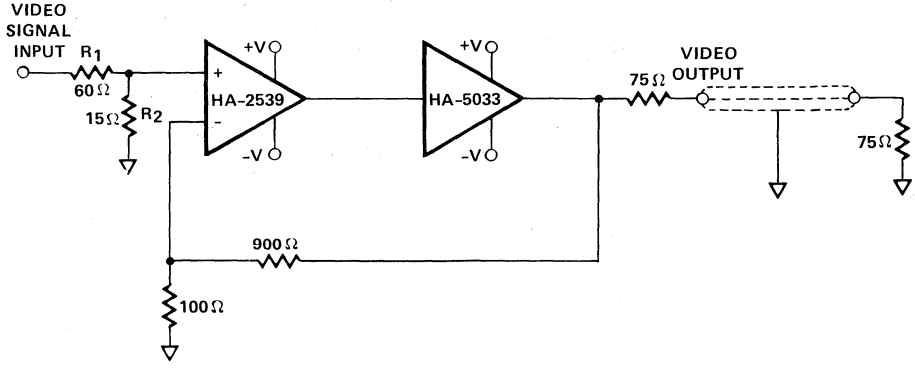
$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2\ V_{IN}$$



NEGATIVE PULSE RESPONSE

$T_A = +25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$

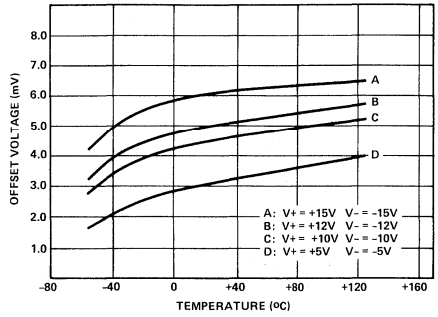
$$V_O = -V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2\ V_{IN}$$



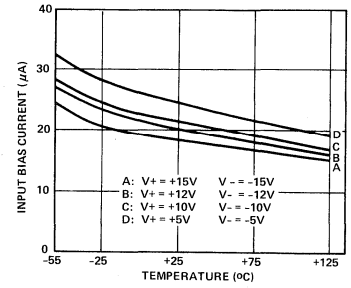
APPLICATION 2. VIDEO GAIN BLOCK

PERFORMANCE CURVES

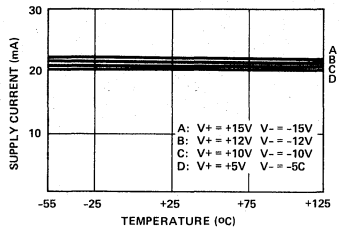
INPUT OFFSET VOLTAGE VS. TEMPERATURE VS. SUPPLY VOLTAGE



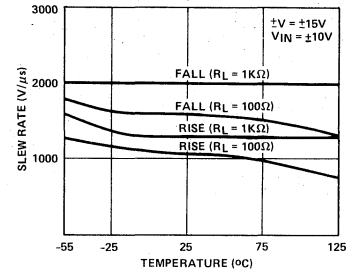
INPUT BIAS CURRENT VS. TEMPERATURE VS. SUPPLY VOLTAGE



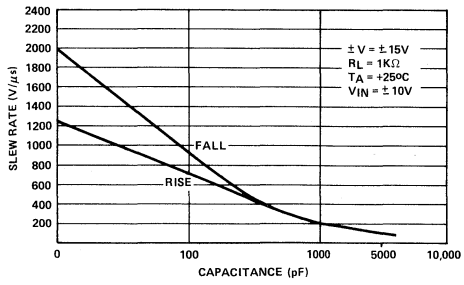
SUPPLY CURRENT VS. TEMPERATURE VS. SUPPLY VOLTAGE



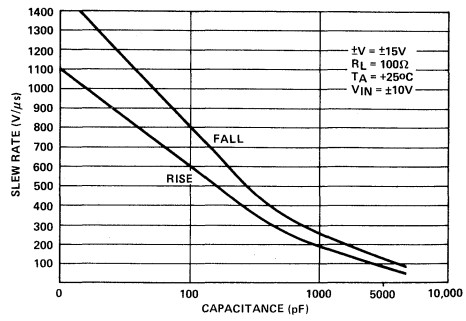
SLEW RATE VS. TEMPERATURE



SLEW RATE VS. LOAD CAPACITANCE (R_L = 1KΩ)

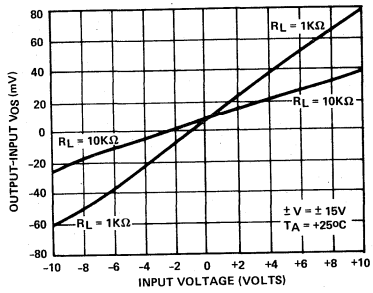


SLEW RATE VS. LOAD CAPACITANCE (R_L = 100Ω)

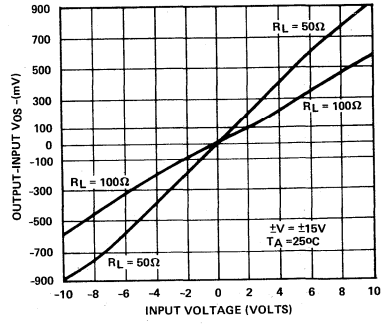


PERFORMANCE CURVES (Continued)

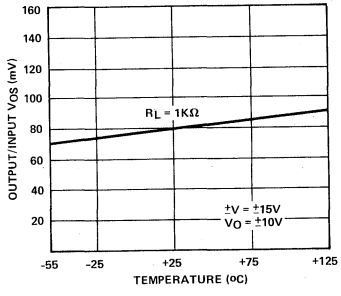
GAIN ERROR VS. INPUT VOLTAGE



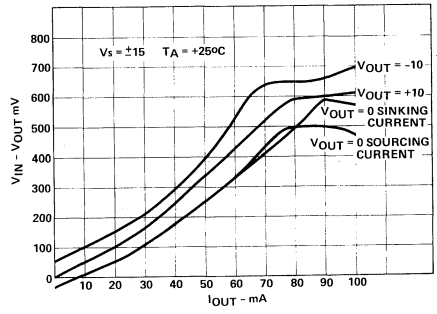
GAIN ERROR VS. INPUT VOLTAGE



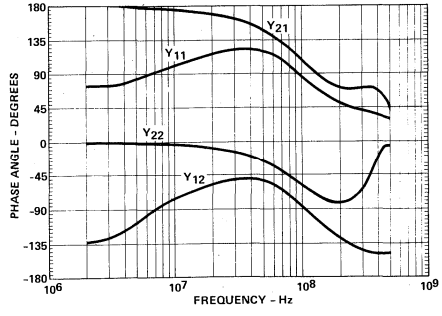
GAIN ERROR VS.TEMPERATURE



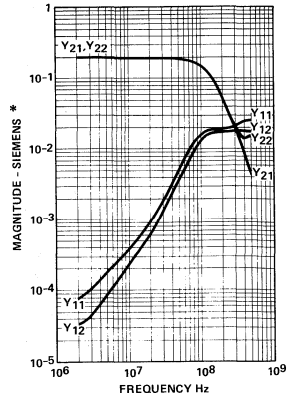
VIN-VOUT VS. IOUT



Y-PARAMETERS PHASE VS. FREQUENCY



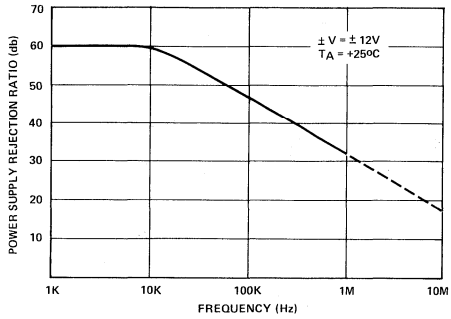
Y-PARAMETER MAGNITUDE VS. FREQUENCY



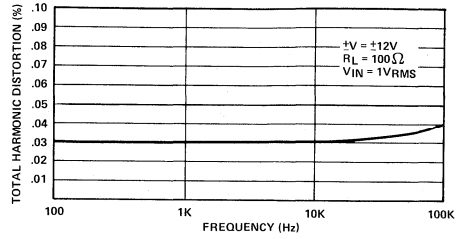
*SIEMENS = Ω^{-1}

PERFORMANCE CURVES (Continued)

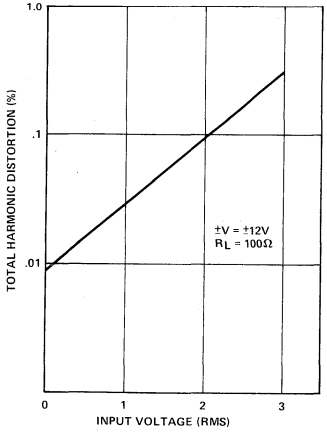
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



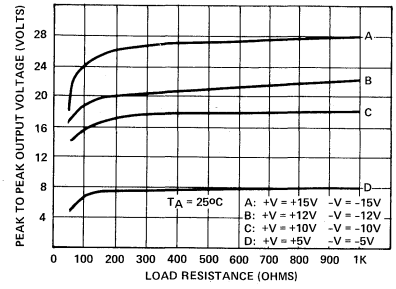
TOTAL HARMONIC DISTORTION VS. FREQUENCY



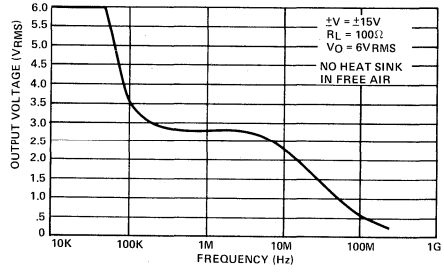
TOTAL HARMONIC DISTORTION VS. RMS INPUT VOLTAGE



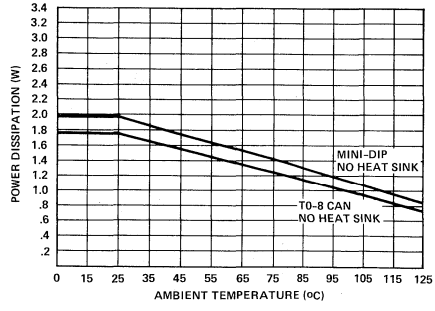
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE VS. SUPPLY VOLTAGE



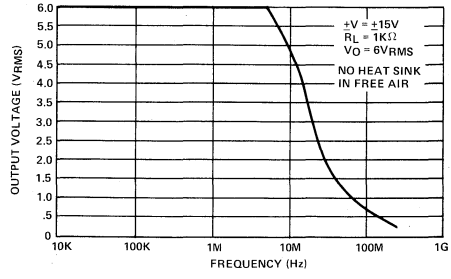
OUTPUT SWING VS. FREQUENCY*



MAXIMUM POWER DISSIPATION VS. AMBIENT TEMPERATURE



OUTPUT SWING VS. FREQUENCY*



*This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.

However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.

This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

HARRIS

HA-5062 Series

Low Power JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- VERY LOW POWER CONSUMPTION TYPICAL SUPPLY CURRENT 200μA
- INTERNAL FREQUENCY COMPENSATION
- HIGH SLEW RATE 4V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL062

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- BATTERY OPERATED EQUIPMENT
- SIGNAL CONDITIONING

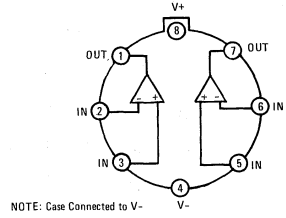
DESCRIPTION

The HARRIS HA-5062 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedence and very low power operation. In addition to being a direct replacement for the TL062 series, the HA-5062 series offers improved performance with a minimum open loop gain 20K V/V and a slew rate of 4v/μs.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5062 series of amplifiers ideally suited for applications in industrial control, communication, and battery powered instrumentation equipment.

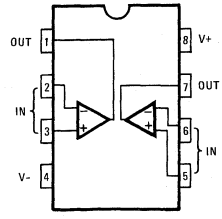
The HA-5062-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5062A-5, HA-5062B-5 and HA-5062-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUTS

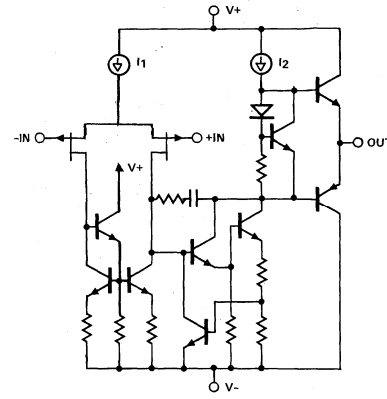


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	±20V
Differential Input Voltage	±40V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation	600mW*
Operating Temperature Range:	
HA-5062-2	$-55^{o}C \leq T_A \leq +125^{o}C$
HA-5062-5	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

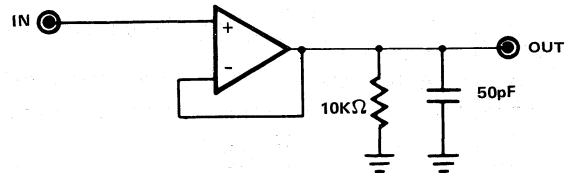
V+ = 15V, V- = -15V. Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5062-2 -55°C to +125°C			HA-5062A-5 0°C to 75°C			HA-5062B-5 0°C to 75°C			HA-5062-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	6		3	6		2	3		3	15	mV
	Full			9			7.5			5			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			3			3			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 5)	Full	80	86		80	86		80	86		70	76		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Unity Gain Bandwidth (Note 6)	+25°C		1			1			1			1		MHz
Full Power Bandwidth (Note 7)	+25°C		63			63			63			63		kHz
TRANSIENT RESPONSE														
Rise Time (Note 8)	+25°C		80			80			80			80		nsec
Overshoot (Note 8)	+25°C		10			10			10			10		%
Slew Rate (Note 9)	+25°C		4			4			4			4		V/µs
Settling Time (Note 10)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 11)	+25°C			0.4			0.4			0.4		200	0.5	mA
Power Supply Rejection Ratio (Note 12)	Full	80	95		80	95		80	95		70	95		dB

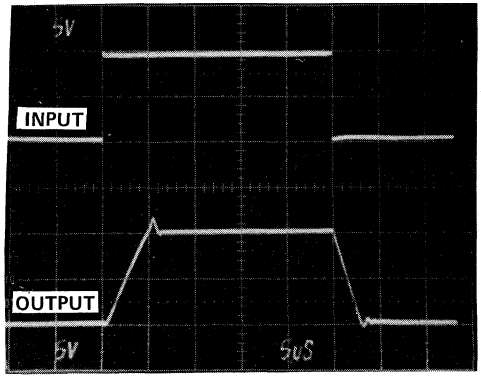
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 100\Omega$.
4. $R_L \geq 10K\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 10K\Omega$.
7. $R_L = 10K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
8. $V_{IN} = 50mV$, $C_L = 50pF$, $R_L = 10K\Omega$.
9. $V_{IN} = 10V$, $C_L = 50pF$, $R_L = 10K\Omega$.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. No load, No signal.
12. $V_{SUPP} = \pm 5V$ D.C. to ±15 V.D.C.

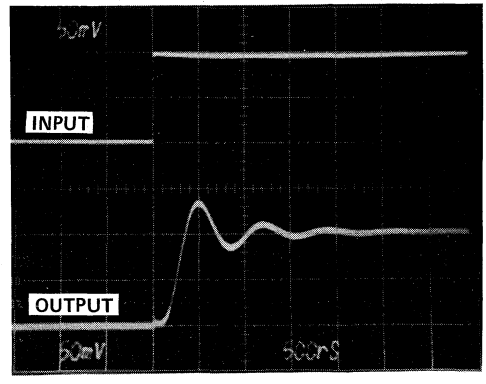
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



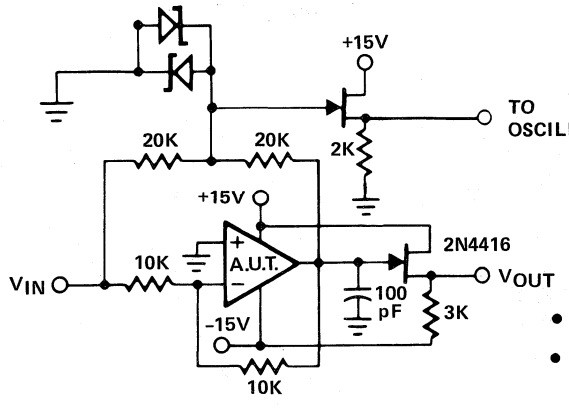
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5 μs/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 50mV/Div.)
Horizontal Scale: (Time: 500ns/Div.)



SETTLING TIME CIRCUIT



- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HARRIS

HA-5064 Series

Low Power, JFET Input Quad Operational Amplifiers

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 100pA
- LOW POWER DISSIPATION 24mW/Pkg.
- FAST SLEWING 4V/μs
- LOW VIO DRIFT 10μV/^{o}C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- GOOD CHANNEL SEPARATION 120dB
- POWER SUPPLY RANGE $\pm$5V TO $\pm$20V

APPLICATIONS

WHERE DENSITY AND POWER REQUIREMENTS ARE DEMANDING:

- ACTIVE FILTERS
- SIGNAL CONDITIONING
- SIGNAL GENERATION
- INSTRUMENTATION AMPLIFIERS

DESCRIPTION

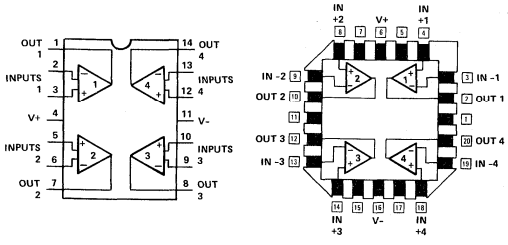
The HARRIS HA-5064 series JFET input monolithic, quad operational amplifiers feature very low power requirements coupled with excellent AC and DC characteristics. Maximum power dissipation of 24 mW/package is achieved by using complementary design, process, and layout techniques.

A 4V/μs slew rate coupled with 1MHz gain-bandwidth makes these devices most suitable for active filter and signal conditioning designs. The HA-5064 series is ideally suited for those applications demanding low power and high density without compromising other performance characteristics. High input impedance and low drift also makes the HA-5064 series useful as instrumentation amplifiers.

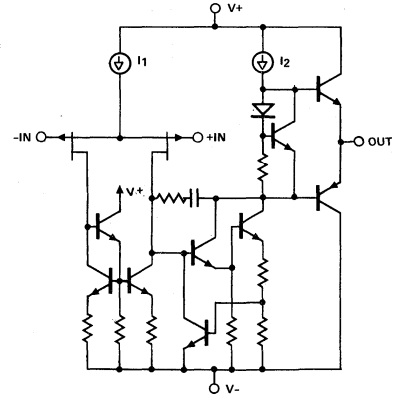
The HA-5064 is packaged in a 14-pin DIP and is pin compatible with most other quad operational amplifiers. The HA-5064-2 is specified for -55^{o}C to +125^{o}C operation while the HA-5064 A-5/HA-5064B-5/HA-5064-5 are specified over the 0^{o}C to +75^{o}C range.

PINOUTS

TOP VIEWS



SIMPLIFIED SCHEMATIC



ONE-FOURTH ONLY

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±30V
Output Current (Note 3)	Continuous
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

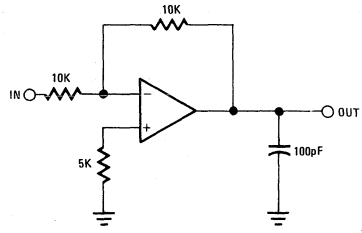
V+ = 15VDC; V- = -15VDC

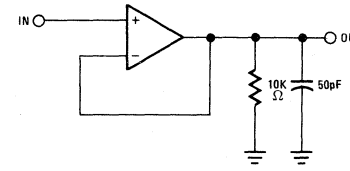
		HA-5064-2 -55°C to +125°C			HA-5064A-5 0°C to +75°C			HA-5064B-5 0°C to +75°C			HA-5064-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2	6		2	6		2	3			15	mV
	Full			9			7.5			5			20	mV
Offset Voltage Average Drift	Full		10			10			10			20		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			3			3			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 6)	Full	80			80			80			70			dB
Gain Bandwidth	+25°C		1			1			1			1		MHz
Channel Separation (Note 7)	+25°C		120			120			120			120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 8)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 9)	Full	±1			±1			±1			±1			mA
Full Power Bandwidth (Note 10)	+25°C		63			63			63			63		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time (10% TO 90%)	+25°C		80			80			80			80		nsec
Slew Rate	+25°C	2	4		2	4		2	4		2	4		V/µsec
Settling Time (Note 13)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C			.8			.8			.8			1	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

NOTES

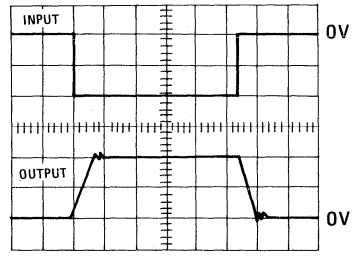
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 10KΩ
6. ΔV_{IN} = ±10V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 10KΩ
8. R_L = 10K ohms.
9. Output current is measured with V_{OUT} = 10 volts.
10. R_L = 10K; Full power bandwidth guaranteed, based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
11. Output resistance measured under open loop conditions.
12. Refer to Test Circuits section of the data sheet.
13. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -1.
14. V_{SUPP} = ±5VDC to ±15VDC.

TEST CIRCUITS

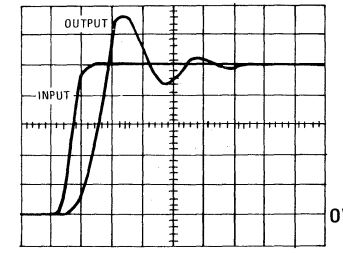




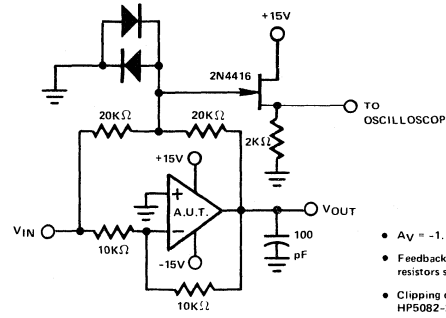
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



SETTLING TIME CIRCUIT



- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HARRIS

HA-5082 Series

JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- LOW POWER CONSUMPTION TYPICAL SUPPLY CURRENT 3.5mA
- HIGH SLEW RATE 15V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL082

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- SIGNAL CONDITIONING

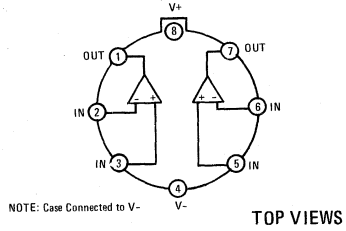
DESCRIPTION

The HARRIS HA-5082 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedance and, high slew rate. In addition to being a direct replacement for the TL082 series, the HA-5082 series offers improved performance with an input offset voltage of 2mV, a slew rate of 15V/μs, and bandwidths of 4MHz.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5082 series of amplifiers ideally suited for applications in industrial control, communication, and computer peripheral equipment.

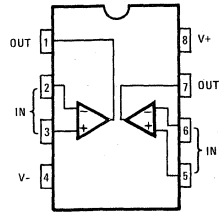
The HA-5082-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5082A-5, HA-5082B-5 and HA-5082-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUTS

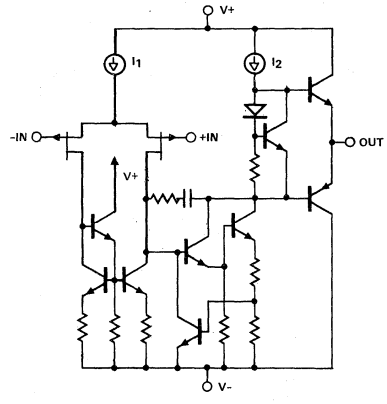


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	±20V	Power Dissipation	600mW*
Differential Input Voltage	± 40V	Operating Temperature Range:	
Input Voltage (Note 2)	±15.0V	HA-5082-2	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Short Circuit Duration	Indefinite	HA-5082-5	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

*To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V. Parameters are guaranteed at indicated ambient temperature after warm-up.

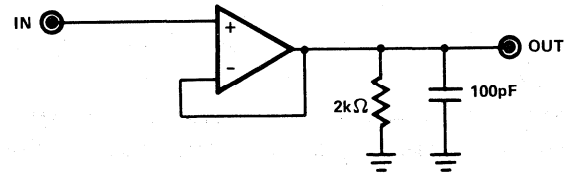
		HA-5082-2 -55°C to +125°C			HA-5082A-5 0°C to 75°C			HA-5082B-5 0°C to 75°C			HA-5082-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	5		3	5			2		5	15	mV
	Full			8			7			4			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			4			2			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	50K	200K		50K	200K		50K	200K		25K	200K		V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ratio (Note 5)	+25°C	80	86		80	86		80	86		70	76		dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 7)	+25°C	± 5			± 5			± 5			± 5			mA
Full Power Bandwidth (Note 8)	+25°C		240			240			240			240		kHz
TRANSIENT RESPONSE														
Rise Time (Note 9)	+25°C		60			60			60			60		nsec
Overshoot (Note 9)	+25°C		10			10			10			10		%
Slew Rate (Note 10)	+25°C		15			15			15			15		V/µs
Settling Time (Note 11)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 12)	+25°C		3.5	5.6		3.5	5.6		3.5	5.6		3.5	5.6	mA
Power Supply Rejection Ratio (Note 13)	+25°C	80	86		80	86		80	86		70	76		dB

NOTES:

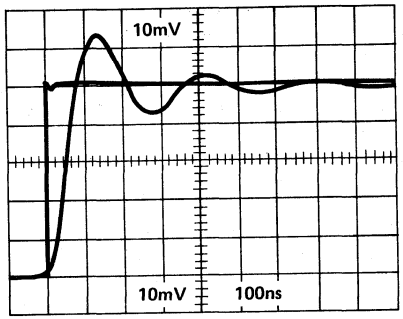
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 100\Omega$.
4. $R_L \geq 2K\ \Omega$, VO = ±10V.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 2K\Omega$.
7. $V_{OUT} = \pm 10V$
8. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
9. $V_{IN} = 50mV$, $C_L = 100pF$, $R_L = 2K\ \Omega$.
10. $V_{IN} = 10V$, $C_L = 100pF$, $R_L = 2K\ \Omega$.
11. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
12. No load, No signal.
13. $V_{SUPP} = \pm 5V$ D.C. to ±15 V.D.C.

TEST CIRCUITS

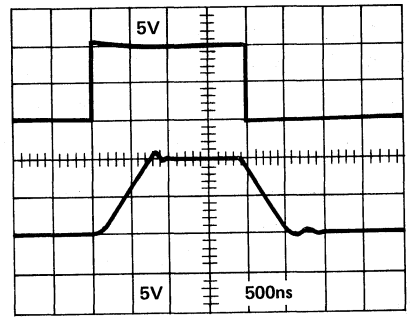
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



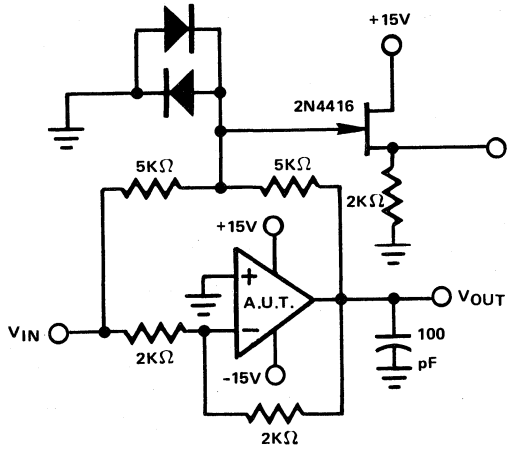
SMALL SIGNAL RESPONSE
Vertical Scale: 10mV/Div.
Horizontal Scale: 100ns/Div.



LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div.
Horizontal Scale: 500ns/Div.



SETTLING TIME CIRCUIT



- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HARRIS

HA-5084 Series

JFET Input Quad Operational Amplifiers

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 200pA
- HIGH SLEW RATE 15V/μs
- WIDE BANDWIDTH 4MHz
- LOW DRIFT 10μV/^{o}C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW SUPPLY CURRENT 7.2mA
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- INTEGRATORS
- TONE DETECTORS
- SAMPLE/HOLD CIRCUITS
- DATA ACQUISITION SYSTEMS
- ABSOLUTE VALUE CIRCUITS

DESCRIPTION

The Harris HA-5084 is a JFET input, monolithic, quad operational amplifier featuring low input bias and offset currents, high input impedance, and high slew rate. Manufactured using FET/Bipolar technology coupled with advanced layout considerations, these devices also feature excellent channel separation and offset voltage drift specifications.

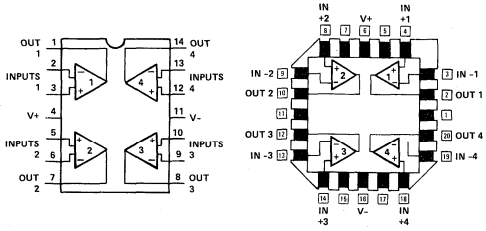
High slew rate (15V/ μs) coupled with excellent input bias (30pA) and offset current (3pA) make the HA-5084 ideally suited for high speed analog designs such as integrators, fast D/A converters, and sample-and-hold circuits.

The HA-5084 is available in ceramic and plastic 14 pin DIP's and is pin compatible with the TL084, LM324, LM348, and MC3403 quad operational amplifier pinout.

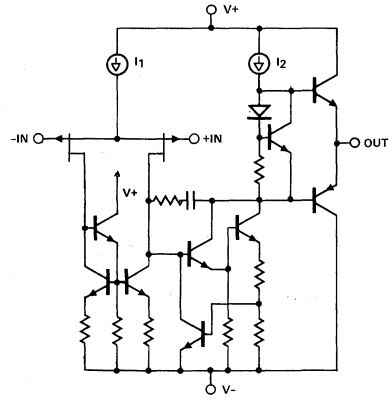
The HA-5084-2 is specified from -55^{o}C to +125^{o}C while the HA-5084-5 operates from 0^{o}C to +75^{o}C.

PINOUTS

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE FOURTH ONLY)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±40V
Output Current (Note 3)	Full Short Circuit Protection
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

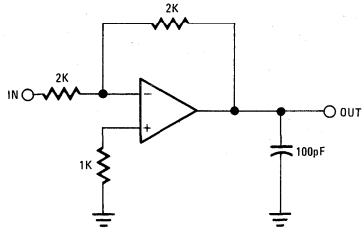
V+ = 15VDC; V- = -15VDC

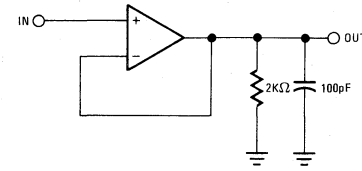
		HA-5084-2 -55°C to +125°C			HA-5084A-5 0°C to +75°C			HA-5084B-5 0°C to +75°C			HA-5084-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C			5			5			2			15	mV
	Full			8			7			4			20	mV
Offset Voltage Average Drift	Full		8.3			8.3			8.3			8.3		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			4			2			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	50K			50K			50K			25K			V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ration (Note 6)	Full	80			80			80			70			dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
Channel Separation (Note 7)	+25°C		-120			-120			-120			-120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note8)	+25°C	±10			±10			±10			±10			V
	Full	±10			±10			±10			±10			V
Output Current (Note 9)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 10)	+25°C		240			240			240			240		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time	+25°C		60			60			60			60		nsec
Slew Rate	+25°C		15			15		10	15			15		V/µsec
Settling Time (Note 13)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		7.2	11		7.2	11		7.2	11		7.2	12	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

NOTES

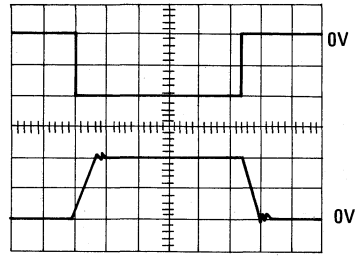
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 10KΩ.
6. ΔV_{IN} = ±10V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms.
8. R_L = 2K ohms.
9. Output current is measured with V_{OUT} = 10 volts.
10. R_L = 2K; Full power bandwidth guaranteed, based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
11. Output resistance specified under open loop conditions.
12. Refer to Test Circuits section of the data sheet.
13. Settling Time is specified to 0.1% of final value for a 10 volt output step and A_V = -1.
14. V_{SUPP} = ±5V.D.C. to ±15V.D.C.

TEST CIRCUITS



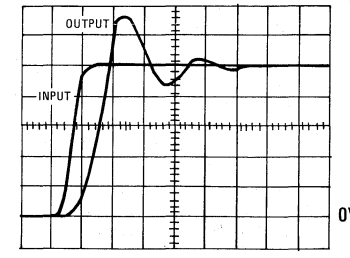


LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



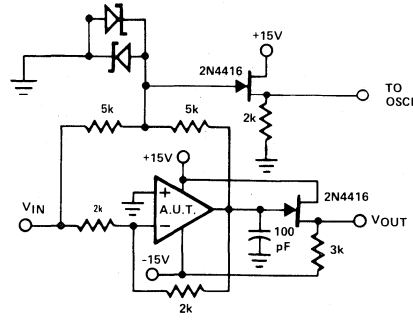
VERT. 5V/DIV.
HORZ. 5 μs/DIV.

SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT



- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HARRIS

HA-5100/5105

Wideband, JFET Input Operational Amplifier

FEATURES

- LOW INPUT OFFSET VOLTAGE 0.5mV
- LOW OFFSET DRIFT . . . . . 5μV/^{o}C
- LOW INPUT BIAS CURRENT 50pA
- LARGE VOLTAGE GAIN . . . . . 150K V/V
- WIDE BANDWIDTH 18MHz
- HIGH SLEW RATE 8V/μsec
- FAST LARGE SIGNAL SETTLING TIME: 1.7μsec

APPLICATIONS

- PRECISION, HIGH SPEED, DATA ACQUISITION SYSTEMS
- PRECISION SIGNAL GENERATION
- PULSE AMPLIFICATION

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

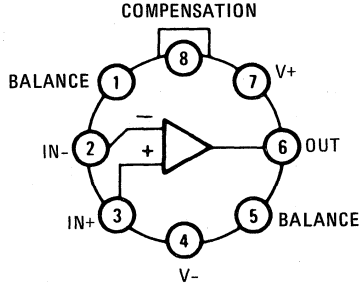
The HA-5100/5105 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics the Harris devices have quite constant slew rate, bandwidth, and settling characteristics over the operating range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing HA-5100/5105's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

* -2 denotes a range of -55^{o}C to +125^{o}C and -5 denotes a 0^{o}C to +75^{o}C range.

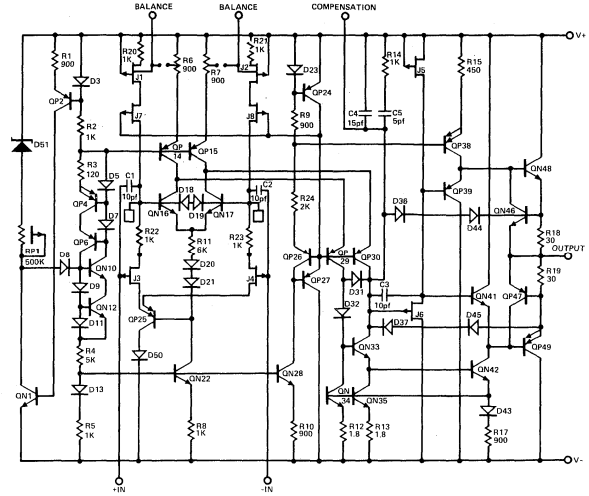
PINOUT

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	510mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

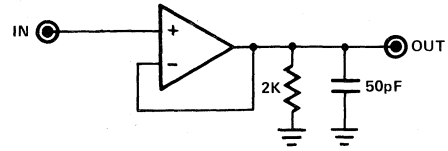
		HA-5100-2 -55°C to +125°C			HA-5100-5 0°C to +75°C			HA-5105-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 6)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	90	150		90	150		75	125		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C		15	35		15	35		20		nsec
Slew Rate	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 10)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
P.S.R.R. (Note 11)	Full	80	86		80	86		80	86		dB

NOTES:

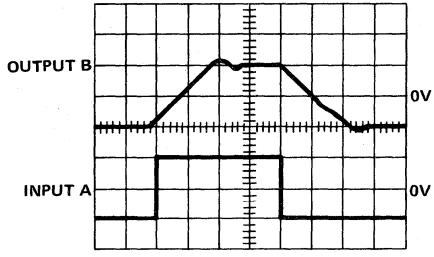
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2K$.
4. $V_{CM} = \pm 10V$ D.C.
5. $R_L = 10K$.
6. $V_{OUT} = 0V$.
7. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
8. Output resistance measured under open loop conditions.
9. Refer to test circuits section of the data sheet.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. $V_{SUPP} = \pm 10V$ D.C. to $\mp 20V$ D.C.

TEST CIRCUITS

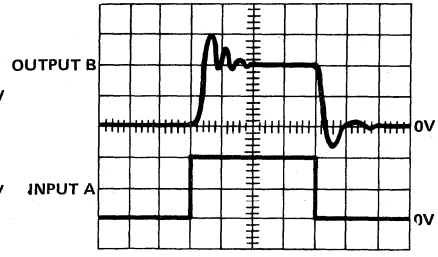
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



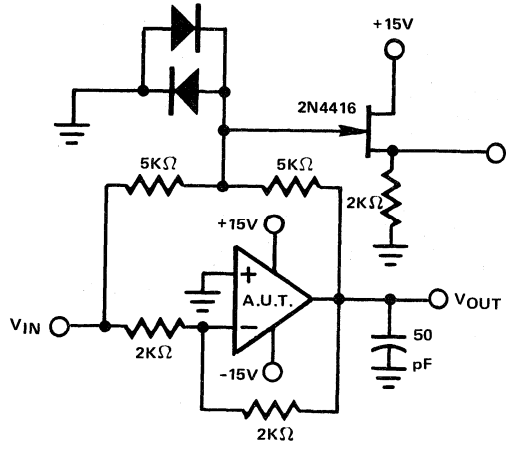
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizonal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizonal Scale: (Time: 100ns/Div.)



SETTLING TIME CIRCUIT

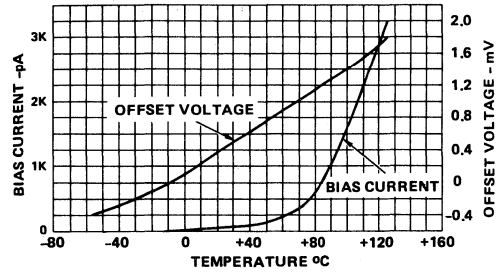


- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

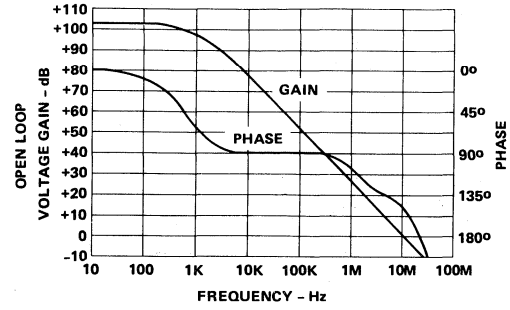
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C UNLESS OTHERWISE STATED.

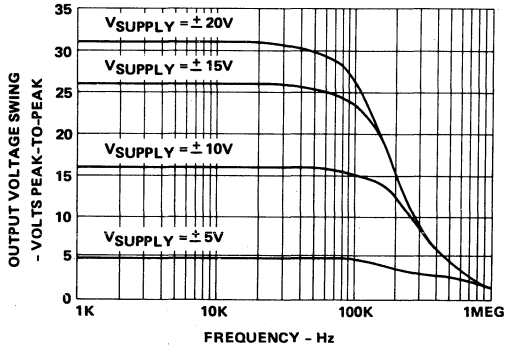
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



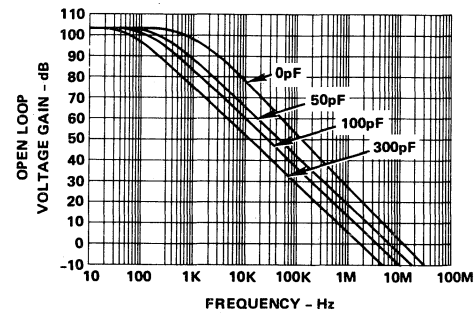
OPEN LOOP FREQUENCY RESPONSE



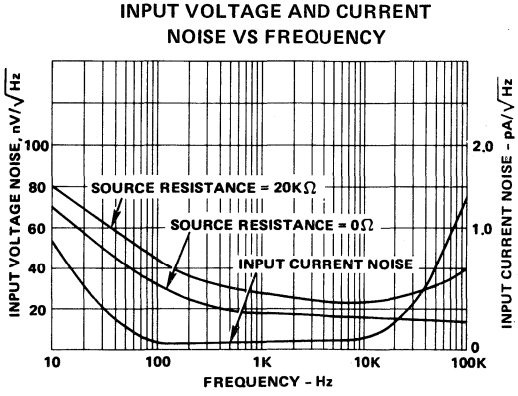
OUTPUT VOLTAGE SWING VS FREQUENCY



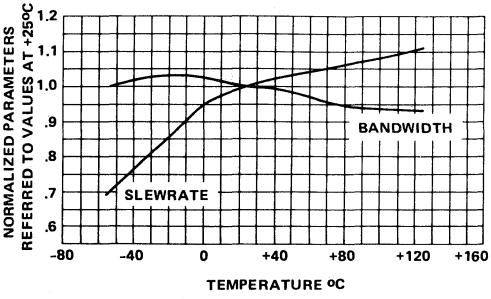
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITORS



INPUT VOLTAGE AND CURRENT NOISE VS FREQUENCY

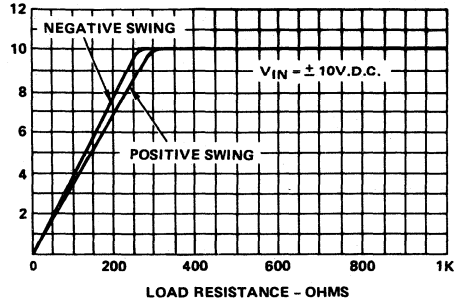


NORMALIZED AC PARAMETERS VS TEMPERATURE

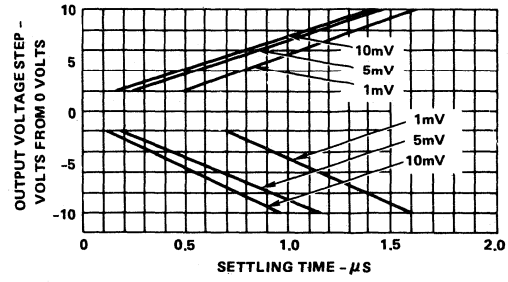


PERFORMANCE CURVES (Continued)

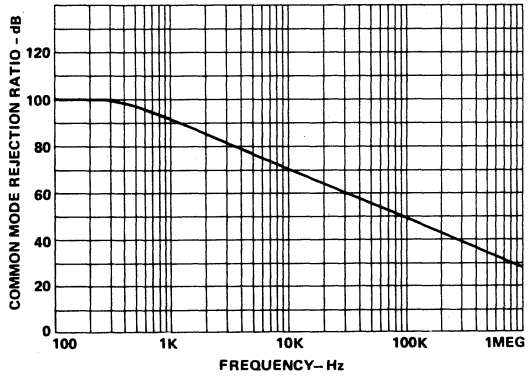
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



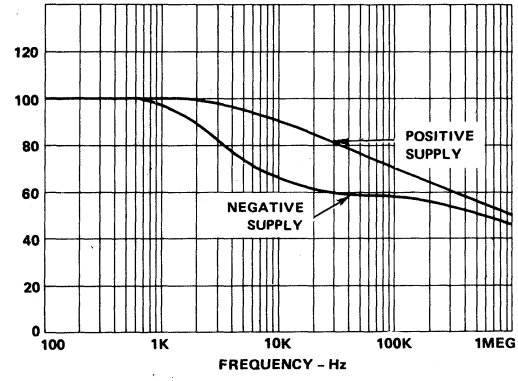
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



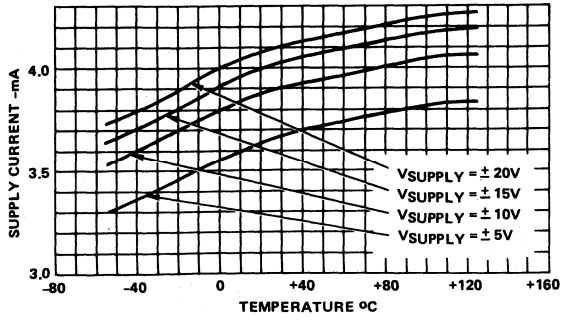
COMMON MODE REJECTION RATIO VS FREQUENCY



POWER SUPPLY REJECTION RATIO VS FREQUENCY



POWER SUPPLY CURRENT VS TEMPERATURE

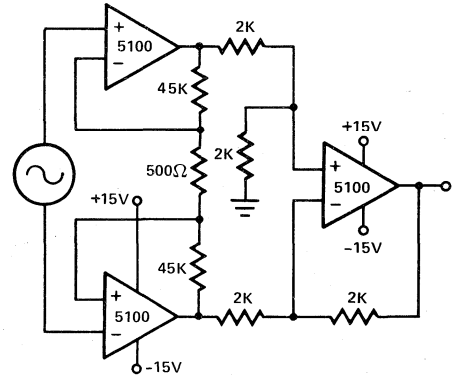


APPLYING THE HA-5100/5105 WIDE BAND OP AMP

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small capacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

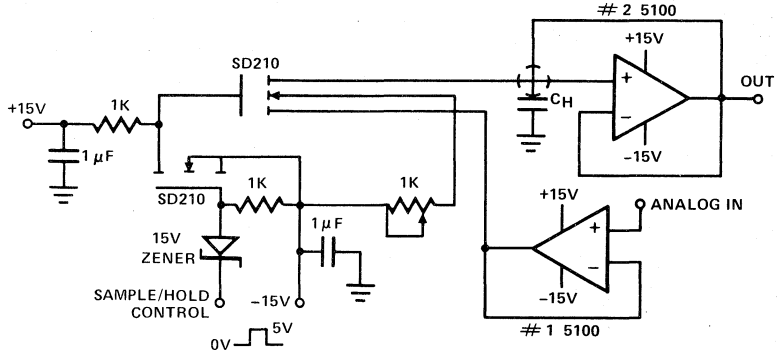
APPLICATIONS

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



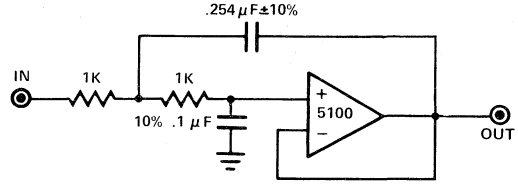
Experimental Results
Yielded 80dB CMRR.
V_{IO} drift < 20μV/°C.

PRECISION/FAST SAMPLE/HOLD CIRCUIT



Experimental Results:
V_{IN} = 10 volt step
C_H = 1000pF
Acquisition Time = 0.4μs (0.1%)
Charge Injection = 30pC
Drift Current = 320pA
Switching Spikes $\approx$ 200mV

1kHz SALLEN AND KEY FILTER



Experimental Results:
F_C = 1KHz
Q = 20
-3dB $\approx$ 1.1KHz
-20dB $\approx$ 3.4KHz

HARRIS

HA-5102/04/12/14

Low Noise High Performance Operational Amplifiers

Preliminary

FEATURES

- LOW NOISE — 4.3 nV/√Hz
- WIDE BANDWIDTH — 8MHz (COMP.) 60MHz (UNCOMP.)
- HIGH SLEW RATE — 3V/μs (COMP.) 20V/μs (UNCOMP.)
- LOW OFFSET VOLTAGE — 2mV
- SINGLE SUPPLY OPERATION
- AVAILABLE IN DUALS OR QUADS

APPLICATIONS

- HIGH Q, ACTIVE FILTERS
- AUDIO AMPLIFIERS
- INSTRUMENTATION AMPLIFIERS
- INTEGRATORS
- SIGNAL GENERATORS

DESCRIPTION

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from 3V/μs slew rate and 8MHz bandwidth (5102/04) to 20V/μs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3 nV/√Hz at kHz.

Fabricated using the Harris standard high frequency process, these operational amplifiers also offer excellent input specifications such as 2.0mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide the flexibility of operating from a single +5V supply.

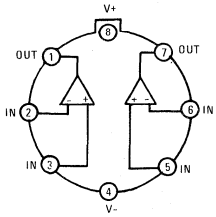
This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate interchangeability with most other dual and quad operational amplifiers.

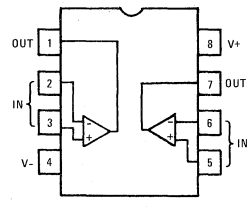
HA-5102	Dual, Compensated
HA-5112	Dual, Uncompensated
HA-5104	Quad, Compensated
HA-5114	Quad, Uncompensated

PINOUTS

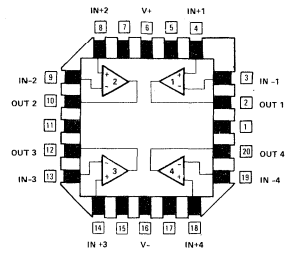
TOP VIEWS



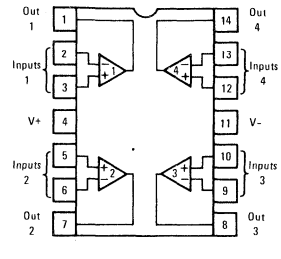
HA-5102/12



HA-5102/12



HA-5104



HA-5104/14

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 4)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-5102/5104/5112/5114-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-5102/5104/5112/5114-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		0.5	2.0		0.5	2.5		0.5	2.0		0.5	2.5	mV
	Full			2.5			3.0			2.5			3.0	mV
Offset Voltage Average Drift	Full		3			3			3			3		µV/°C
Bias Current	+25°C		130	200		130	200		130	200		130	200	nA
	Full			325			325			325			325	nA
Offset Current	+25°C		30	75		30	75		30	75		30	75	nA
	Full			125			125			125			125	nA
Input Resistance	+25°C		500			500			500			500		kΩ
Common Mode Range	Full	±12			±12			±12			±12			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C													
	Full	100K	250K		100K	250K		100K	250K		100K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			86			86			86			dB
Small Signal Bandwidth	+25°C													
HA-5102/5104			8			8			8			8		MHz
Gain Bandwidth Product	+25°C													
HA-5112/5114 A_V = 10			60			60				60		60		MHz
Channel Separation (Note 7)	+25°C		108			108			180			108		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Output Current (Note 8)	Full	±10	±15		±10	±15		±10	±15		±10	±15		mA
Full Power Bandwidth														
(Note 9) HA-5102/5104	+25°C		50			50			50			50		kHz
HA-5112/5114	+25°C		250			250			250			250		kHz
Output Resistance	+25°C		110			110			110			110		Ω

ELECTRICAL CHARACTERISTICS

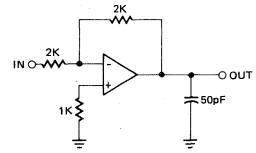
V+ = 15VDC; V- = -15VDC

		HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TRANSIENT RESPONSE (Note 10)														
Rise time														
HA-5102/5104	+25°C		50	100		50	100		50	100		50	100	ns
HA-5112/5114	+25°C		38	60		38	60		38	60		38	60	ns
Overshoot														
HA-5102/5104	+25°C		20	35		20	35		20	35		20	35	%
HA-5112/5114	+25°C		30	40		30	40		30	40		30	40	%
Slew Rate														
HA-5102/5104	+25°C	±1	±3		±1	±3		±1	±3		±1	±3		V/μs
HA-5112/5114	+25°C	±12	±20		±12	±20		±12	±20		±12	±20		V/μs
Settling Time (Note 11)														
HA-5102/5104	+25°C		4.5			4.5			4.5			4.5		μs
HA-5112/5114	+25°C		0.6			0.6			0.6			0.6		μs
NOISE CHARACTERISTICS														
Input Noise Voltage	+25°C													
f = 10Hz			17			17			17			17		$nV/\sqrt{Hz}$
f = 1KHz			4.3			4.3			4.3			4.3		$nV/\sqrt{Hz}$
Input Noise Current	+25°C													
f = 10Hz			5.1			5.1			5.1			5.1		$pA/\sqrt{Hz}$
f = 1KHz			.57			.57			.57			.57		$pA/\sqrt{Hz}$
Broadband Noise Voltage	+25°C													
f = DC to -30KHz			870			870			870			870		nVrms
POWER SUPPLY CHARACTERISTICS														
Supply Current														
HA-5102/5112	+25°C		3.0	5.0		3.0	5.0		3.0	5.0		3.0	5.0	mA
HA-5104/5114	+25°C		5.0	6.5		5.0	6.5		5.0	6.5		5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86			86			86			86			dB

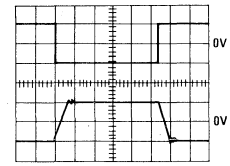
NOTES:

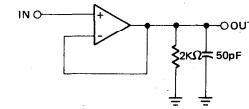
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages $< \pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above $T_A = +25°C$.
5. $V_{OUT} = \pm 10V$, $R_L = 2K$.
6. $V = \pm 5.0V$.
7. Channel separation value is refferred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; $R_S = 1K\Omega$. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. Output current is measured with $V_{OUT} = \pm 5V$.
9. Full power bandwidth is guaranteed by equation:
   Full power bandwidth = $\frac{\text{Slew Rate}}{2\pi V \text{ Peak}}$
10. Refer to Test Circuits section of the data sheet.
11. Setting time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10 for HA-5112/5114 and 0.1% of final value for a 10 volt input step, A_V = -1 for HA-5102/5104.

TEST CIRCUITS

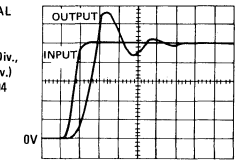


LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.) HA-5102/5104

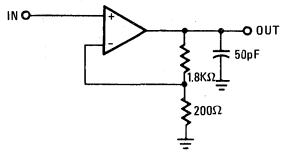


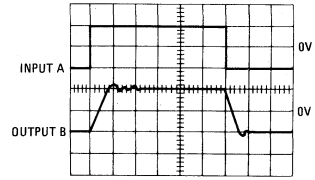


SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.) HA-5102/5104

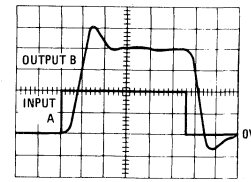


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT HA-5112/5114



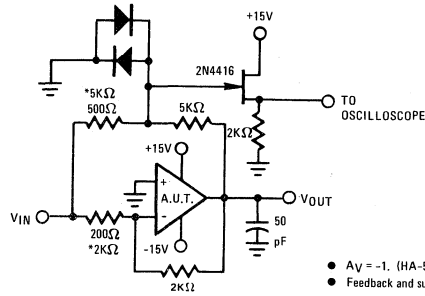


VOLTS: Input A: .5V/Div., Output B: 5V/Div.
TIME: 500ns/Div.



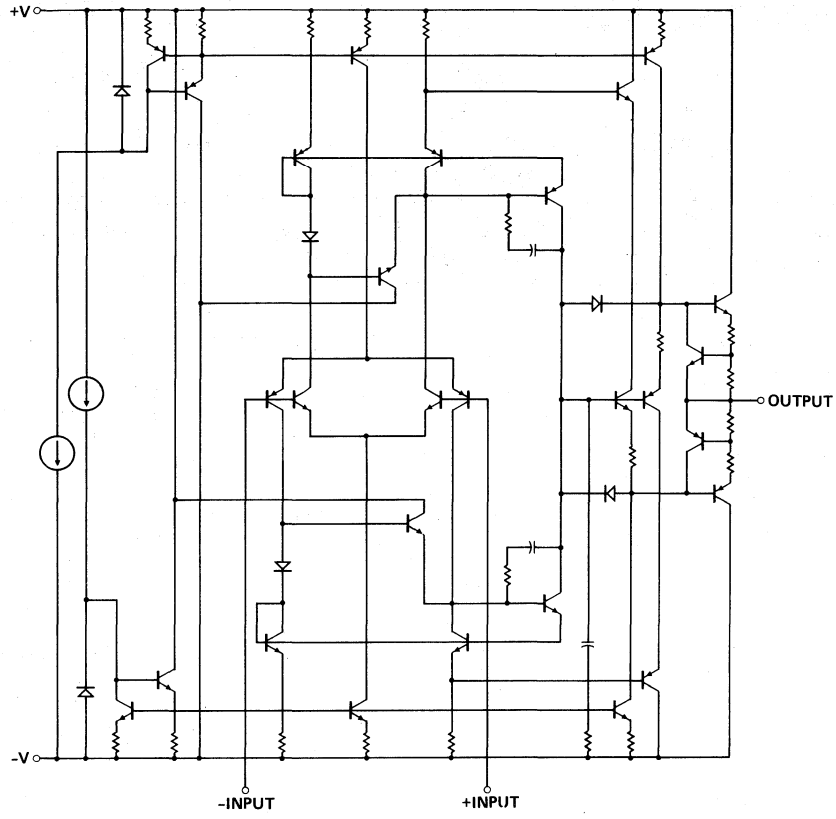
VOLTS: Input A: .01V/Div., Output B: 50mV/Div.
TIME: 50ns/Div.

SETTLING TIME CIRCUIT



- A_V = -1. (HA-5102/5104), *A_V = -10 (HA-5112/5114)
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional HP5082-2810 recommended.

SCHEMATIC



HARRIS

HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

Not Recommended For New Designs See HA-5160

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE 50V/μs
- SETTLING TIME 850ns
- POWER BANDWIDTH 800KHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

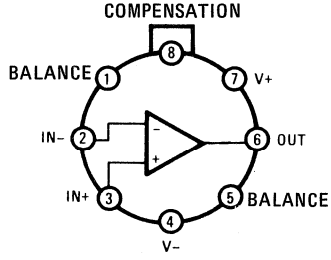
HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are controlled at closed loop gains greater than 10 without compensation.

With excellent dynamic and input characteristics, HA-5110/5115 are well suited for many wideband, pulse, and video applications. These amplifiers are ideal components for video and RF circuitry requiring up to 60MHz gain-bandwidth-product and 800KHz power bandwidth. 50V/μs slew rate and 850ns settling time make these devices useful in pulse amplification and data acquisition designs. HA-5110/5115's 0.5mV offset voltage, 10pA offset current, and extremely high impedance coupled with excellent AC parameters make these amplifiers ideal selections for accurate signal conditioning designs. For applications requiring less critical input characteristics, HA-5115 is available in untrimmed form.

HA-5110/5115 are available in metal can (TO-99) packages. Suffix -2 denotes a range to -55°C to +125°C and -5 denotes a 0°C to +75°C range.

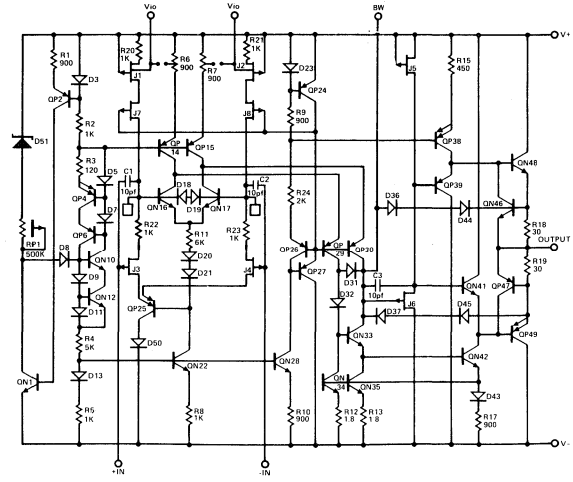
PINOUT

TOP VIEW



Case Connected to V-

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^-	40V	Internal Power Dissipation (Note 2)	510mW
Differential Input Voltage	±40V	Storage Temperature Range	-65°C to +150°C
Peak Output Current	Full Short Circuit Protection		

ELECTRICAL CHARACTERISTICS

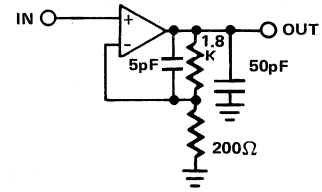
$V+ = 15VDC$; $V- = -15VDC$
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5110-2 -55°C to +125°C			HA-5110-5 0°C to +75°C			HA-5115-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product (A_V = 10)	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Output Current (Note 6)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	550	625		550	625		550	625		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		nsec
Slew Rate (A_V = 10)	+25°C	35	50		35	50		35	40		V/µsec
Settling Time (Note 10)	+25°C		.85			.85			1.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
Power Supply Rejection Ratio (Note 11)	+25°C	80	94		80	94		80	94		dB

NOTES:

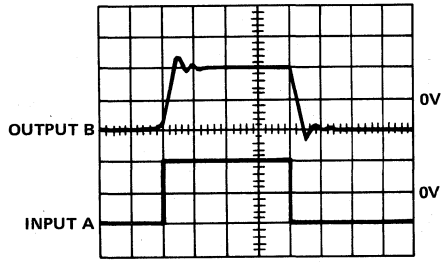
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2K$
4. $V_{CM} = \pm 10$ V.D.C.
5. $R_L = 10K$
6. $V_{OUT} = 0V$
7. $R_L = 2K$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE.}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and $A_V = -10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to ±20 V.D.C.

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



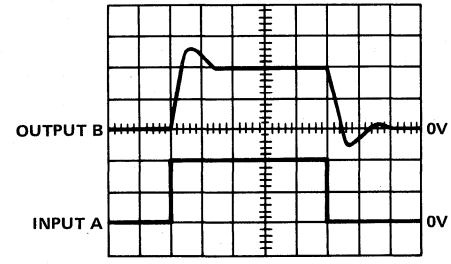
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A=.5V/Div,B=5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

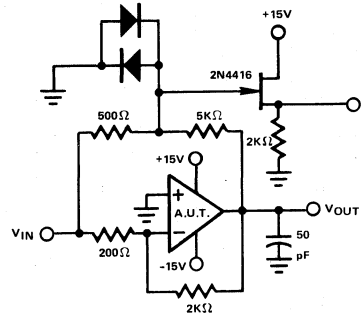


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=10mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME CIRCUIT

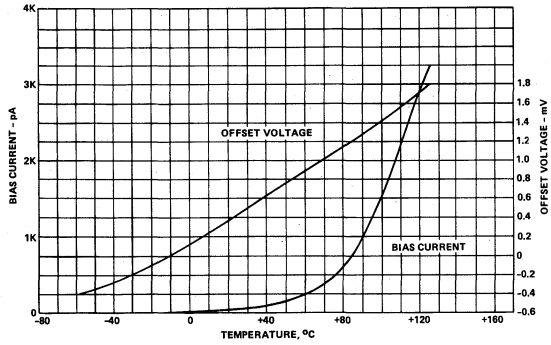


- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

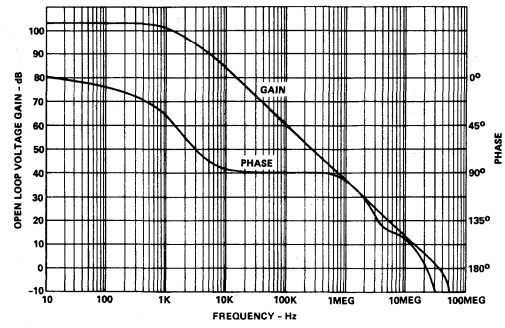
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

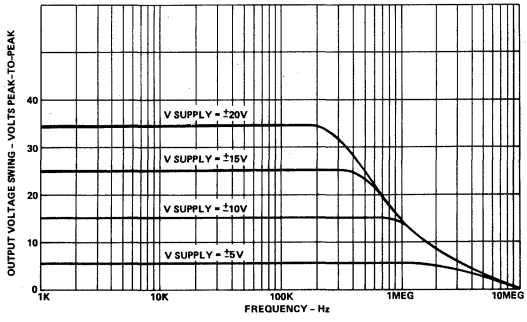
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



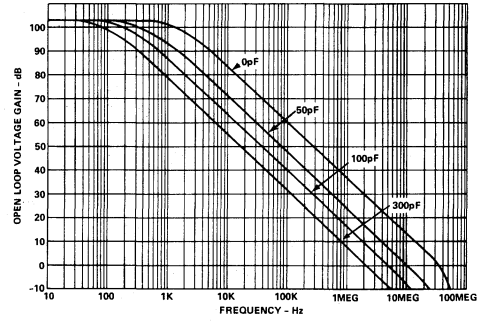
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. FREQUENCY

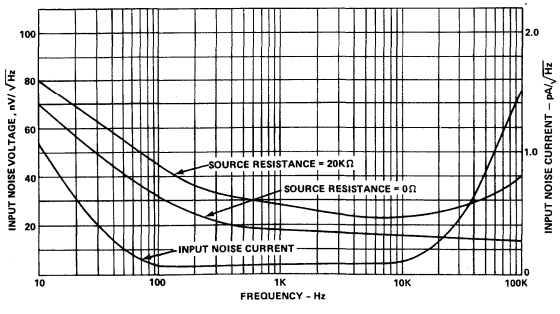


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITORS

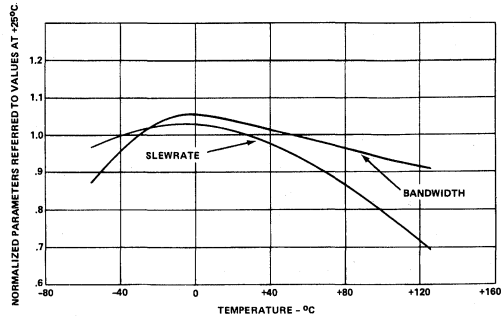


NOTE: External compensation components are not required for closed loop gains > 10, but may be added to reduce bandwidth if desired.

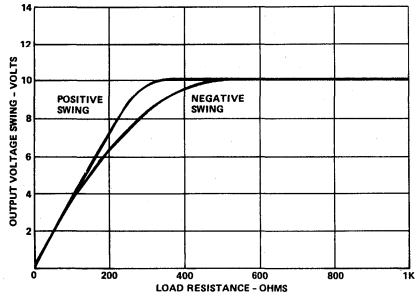
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



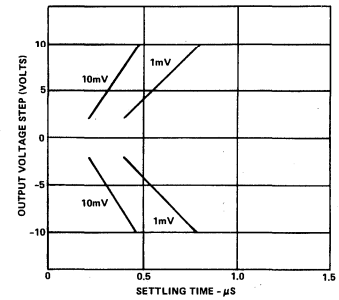
NORMALIZED AC PARAMETERS vs. TEMPERATURE



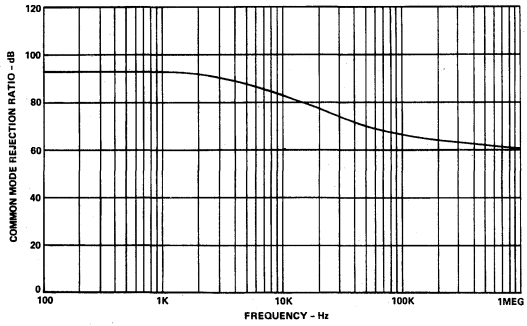
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



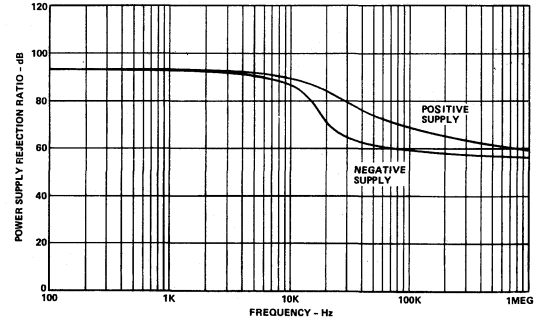
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



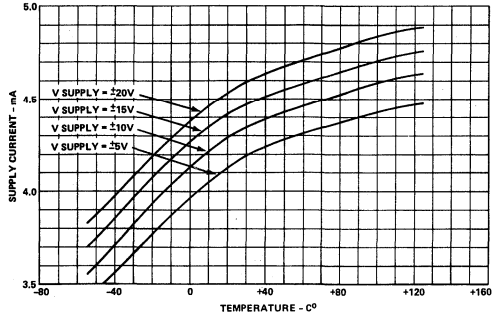
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE



APPLYING THE HA-5110/5115

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small compacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.

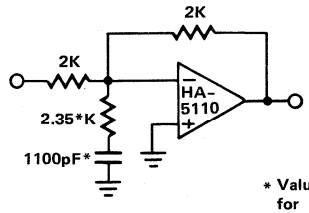
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small capacitor ($\approx$ 10pF) should be connected in parallel with the feedback resistor.

4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

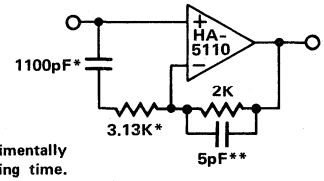
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

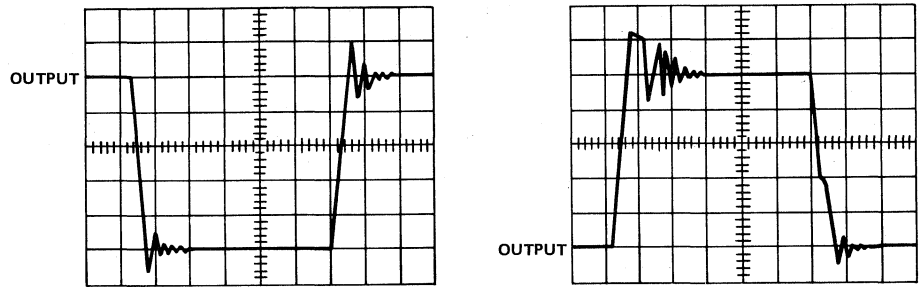
INVERTING



NON-INVERTING

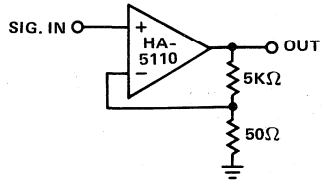


* Values were determined experimentally for optimum speed and settling time.
** Optional

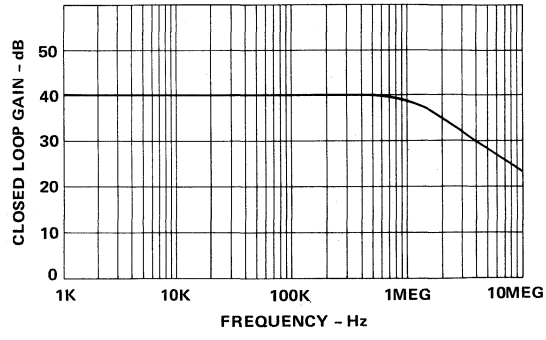


Vertical Scale: (Volts: 2V/Div.)
Horizonal Scale: (Time: 500ns/Div.)

40dB, 1MHz BANDWIDTH AMPLIFIER



CLOSED LOOP FREQUENCY RESPONSE (A_V = 100)



HARRIS

HA-5130/5135

Precision Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE — 25μV
- LOW OFFSET VOLTAGE DRIFT — 0.4μV/^{o}C
- LOW NOISE — 9nV/$\sqrt{Hz}$
- OPEN LOOP GAIN — 10^7
- BANDWIDTH (UNITY GAIN) — 2.5MHz
- ALL BIPOLAR CONSTRUCTION

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25μV (Max.) input offset voltage and 0.4μV/^{o}C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

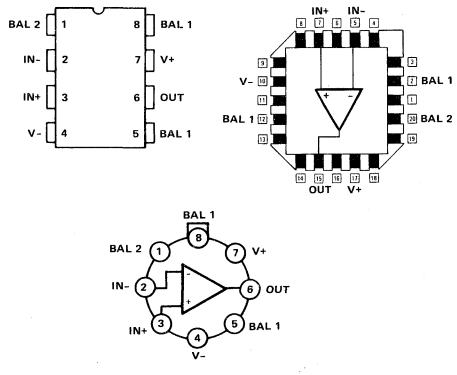
These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

HA-5130/35 is packaged in an 8 pin (TO-99) can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations.

HA-5130/5135-2 is specified for -55^{o}C to +125^{o}C operation while HA-5130/5135-5 operate from 0^{o}C to +75^{o}C.

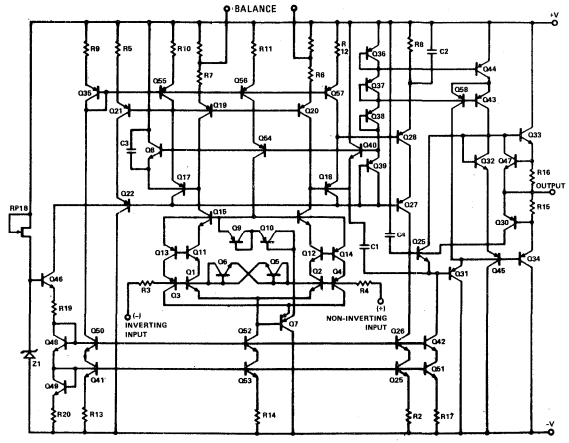
PINOUTS

TOP VIEWS



(PINS 5 AND 8 ARE INTERNALLY CONNECTED)

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated

Voltage Between V+ and V- Terminals 40.0V

Differential Input Voltage ±15.0V

Output Short Circuit Duration Indefinite

Power Dissipation (Note 2) 300mW

Operating Temperature Range

HA-5130/5135-2 $-55°C \leq T_A \leq +125°C$

HA-5130/5135-5 $0°C \leq T_A \leq +75°C$

Storage Temperature Range $-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

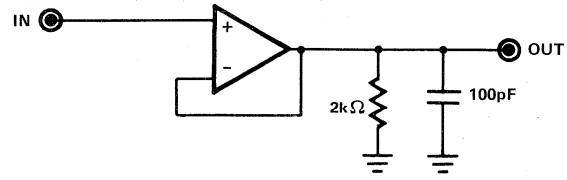
PARAMETER	TEMP.	HA-5130-2/-5 MIN.	HA-5130-2/-5 TYP.	HA-5130-2/-5 MAX.	HA-5135-2/-5 MIN.	HA-5135-2/-5 TYP.	HA-5135-2/-5 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		10	75	µV
	Full		50	60		50	130	µV
Average Offset Voltage Drift	Full		0.4	0.6		0.4	1.3	µV/°C
Bias Current	+25°C		±1	±2		±1	±4	nA
	Full			±4			±6	nA
Bias Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Offset Current	+25°C			2			4	nA
	Full			4			5.5	nA
Offset Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C	20	30		20	30		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C			0.6			0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10Hz			13.0	18.0		13.0	18.0	
f_0 = 100Hz			10.0	13.0		10.0	13.0	
f_0 = 1000Hz			9.0	11.0		9.0	11.0	
Input Noise Current (Note 3) 0.1Hz to 10Hz	+25°C		15	30		15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10Hz			0.4	0.8		0.4	0.8	
f_0 = 100Hz			0.17	0.23		0.17	0.23	
f_0 = 1000Hz			0.14	0.17		0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140		120	140		dB
	Full	120			120			dB
Common Mode Rejection Ratio (Note 5)	Full	110	120		106	120		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5		0.6	2.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C	8	10		8	10		kHz
Output Current (Note 8)	+25°C	±15	±20		±15	±20		mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C		340			340		ns
Slew Rate	+25°C	0.5	0.8		0.5	0.8		V/µs
Settling Time (Note 11)	+25°C		11			11		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.0	1.3		1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130		94	130		dB

NOTES:

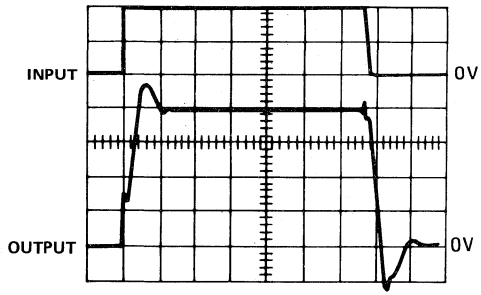
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temp.'s above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2k. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV
5. V_{CM} = ±10V DC
6. R_L = 600Ω
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. V_{SUPP} = ±5V DC to ±20V DC.

TEST CIRCUITS

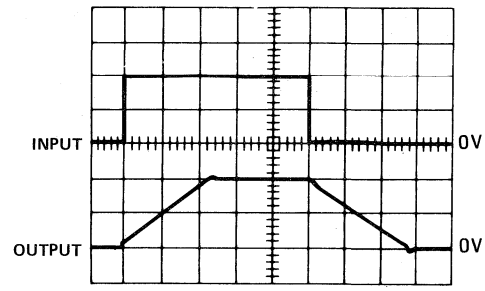
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



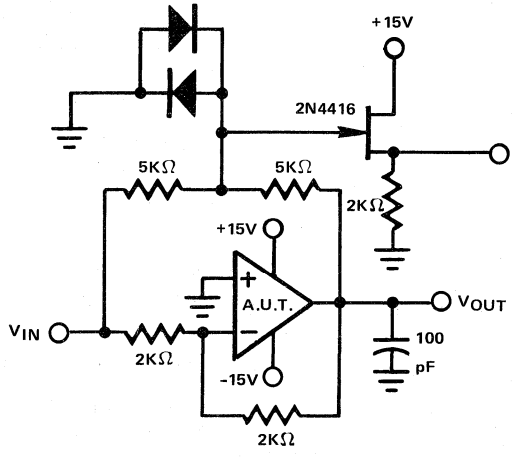
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)

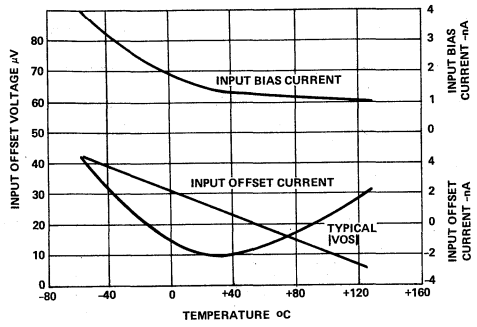


SETTLING TIME CIRCUIT

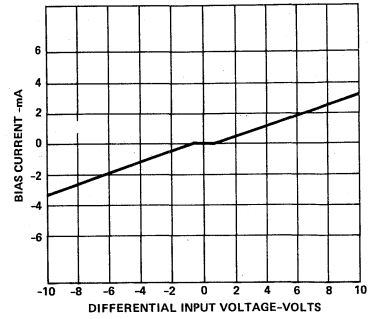


- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

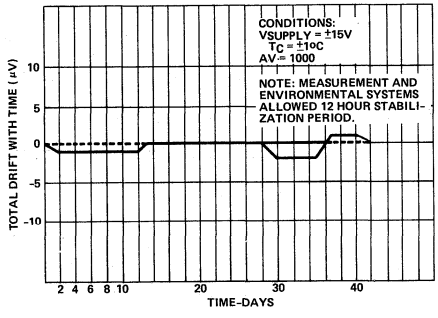
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



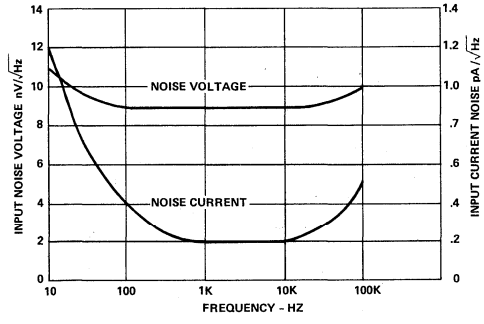
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



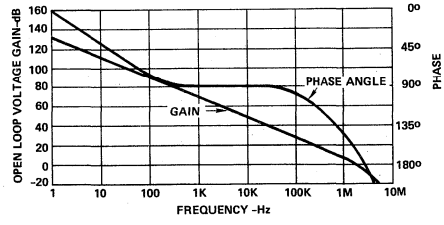
HA-5130 OFFSET VOLTAGE STABILITY vs. TIME



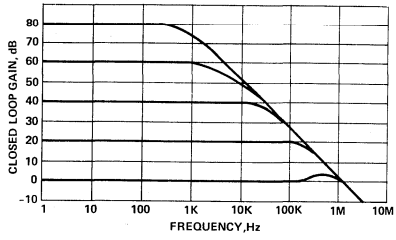
INPUT NOISE vs. FREQUENCY



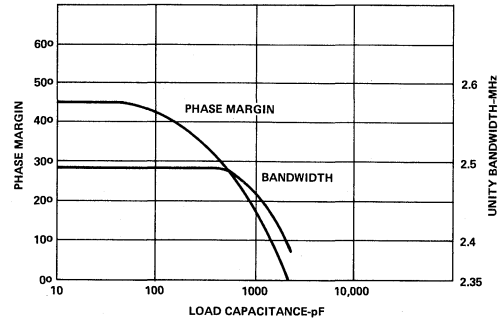
OPEN LOOP FREQUENCY RESPONSE



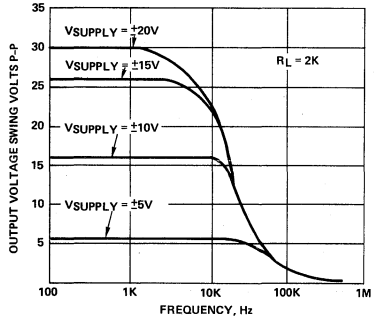
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



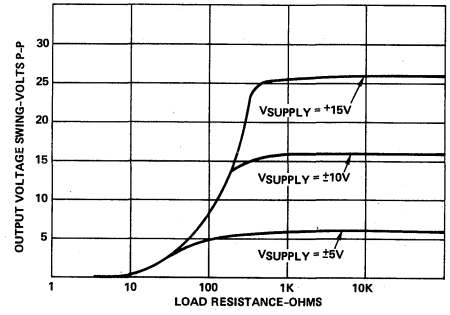
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



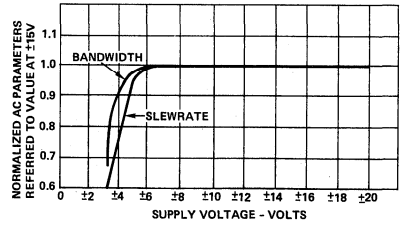
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE

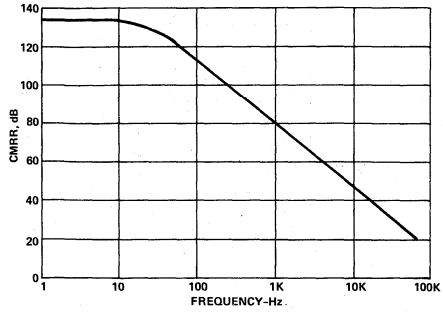


NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

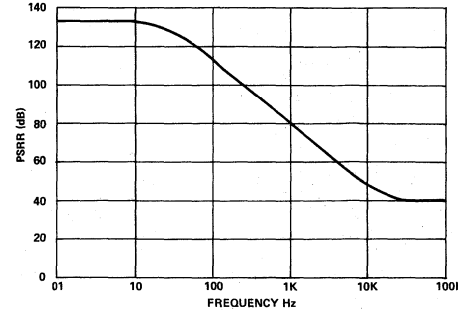


PERFORMANCE CURVES (Continued)

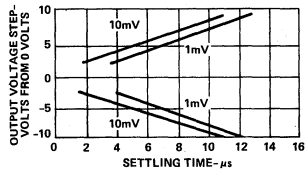
CMRR vs. FREQUENCY



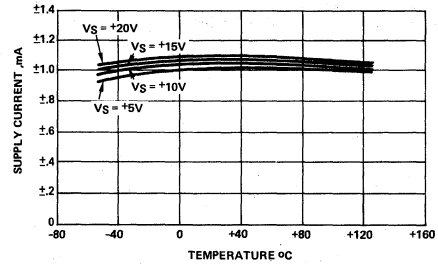
PSRR vs. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



APPLYING THE HA-5130/5135 OPERATIONAL AMPLIFIERS

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces, and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings, and shield drivers are recommended for the most critical applications.

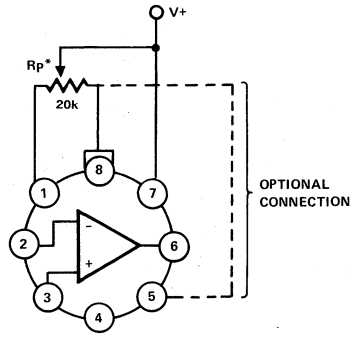
3. When driving large capacitive loads (> 500pF), as small value resistor (≈50Ω) should be connected in series with the output and inside the feedback loop.

4. OFFSET VOLTAGE ADJUSTMENT: A 20 KΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10KΩ, 50KΩ, and 100KΩ may be used. The minimum adjustment range for given values is ±2mV.

5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

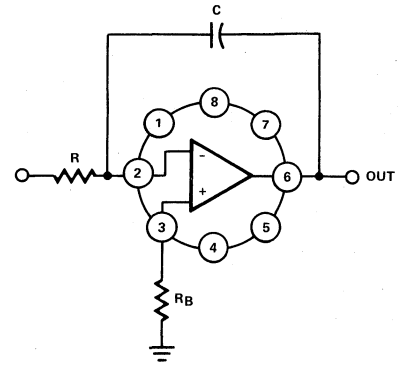
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of IV are applied between the inputs, the use of limiting resistors at the inputs is recommended.

OFFSET NULLING CONNECTIONS



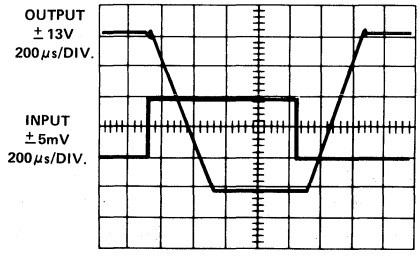
*Although Rp is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

PRECISION INTEGRATOR

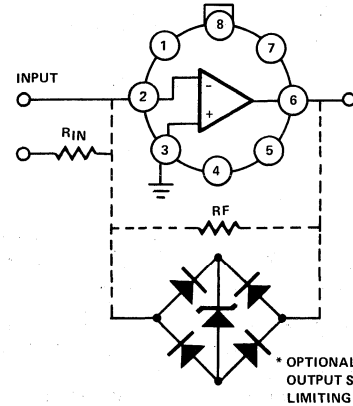


The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

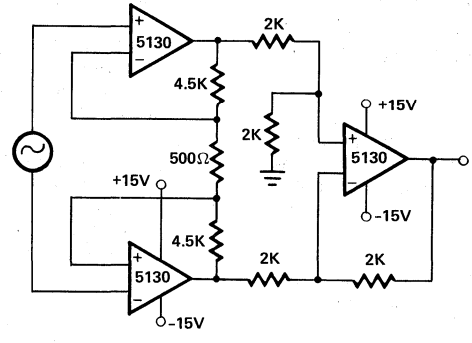
ZERO CROSSING DETECTOR



Low V_{OS} coupled with high open loop Gain, high CMRR, and high PSRR make HA-5130 ideally suited for precision detector applications.



PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



HARRIS

HA-5141/42/44

Ultra-Low Power Operational Amplifiers

FEATURES

- LOW SUPPLY CURRENT — 60μA/AMP
- WIDE OPERATING VOLTAGE RANGE — 2V TO 30V
- SINGLE OR DUAL SUPPLY OPERATION
- HIGH SLEW RATE — 1.5V/μs
- HIGH GAIN — 100kV/V
- UNITY GAIN STABLE
- "A" SUFFIX DEVICES COMBINE THE ABOVE CHARACTERISTICS WITH PRECISION INPUT SPECIFICATIONS
- AVAILABLE IN SINGLES, DUALS AND QUADS

APPLICATIONS

- PORTABLE INSTRUMENTS
- METER AMPLIFIERS
- TELEPHONE HEADSETS
- MICROPHONE AMPLIFIERS
- INSTRUMENTATION

DESCRIPTION

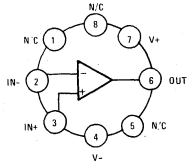
The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

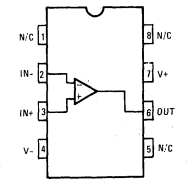
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (50nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers ($20nV/\sqrt{Hz}$). These characteristics coupled with a 1.5V/μs slew rate rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (2V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

These amplifiers are available in singles (HA-5141, can or minidip), duals (HA-5142, can or minidip) or quads (HA-5144, 14 pin dip) with industry standard pinouts which allow the HA-5141/42/44's to be interchangeable with most other operational amplifiers.

PINOUTS

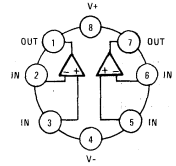
TOP VIEW

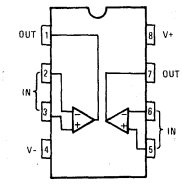




HA-5141

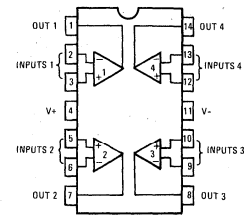
TOP VIEW





HA-5142

TOP VIEW



HA-5144

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	$0^oC \leq T_A \leq +75^oC$
Differential Input Voltage	±7V		$-55^oC \leq T_A \leq +125^oC$
Output Current	S/C Protected	Storage Temperature Range	$-65^o \leq T_A \leq +150^oC$
Internal Power Dissipation	500mW		

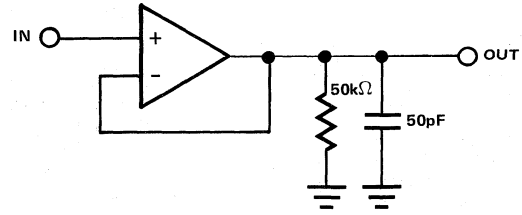
ELECTRICAL CHARACTERISTICS V+ = 5V, V- = 0V

PARAMETER	TEMP.	HA-5141/42/44A -2 or -5 MIN	HA-5141/42/44A -2 or -5 TYP	HA-5141/42/44A -2 or -5 MAX	HA-5141/42/44 -2 or -5 MIN	HA-5141/42/44 -2 or -5 TYP	HA-5141/42/44 -2 or -5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	2		2	6	mV
	Full			5			8	mV
Average Offset Voltage Drift	Full		3			3		µV/°C
Bias Current	+25°C		45	75		45	100	nA
	Full			100			125	nA
Offset Current	+25°C		0.3	10		0.3	10	nA
	Full			15			20	nA
Common Mode Range	+25°C	0 to 4			0 to 3.5			V
	Full	0 to 4			0 to 3			V
Differential Input Resistance	+25°C		0.6			0.6		MΩ
Input Noise Voltage (f = 1kHz)	+25°C		20			20		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.25			0.25		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	50K	100K		20K	100K		V/V
	Full	30K			15K			V/V
Common Mode Rejection Ratio	Full	80	105		77	105		dB
Closed Loop Bandwidth (Note 2, 3)	+25°C		0.4			0.4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	+25°C	0 to 4			0 to 3.5			V
Full Power Bandwidth (Note 4)	+25°C		60			45		kHz
Output Current (Note 5) Source	+25°C		+3			+3		mA
Sink			-0.8			-0.8		mA
TRANSIENT RESPONSE								
Rise Time	+25°C		600			600		ns
Slew Rate	+25°C	1	1.5		0.5	1		V/µs
Settling Time (Note 6)	+25°C		10			10		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		45	65		50	80	µA
	Full			75			100	µA
Power Supply Rejection Ratio	Full	80	105		77	105		dB

NOTES:

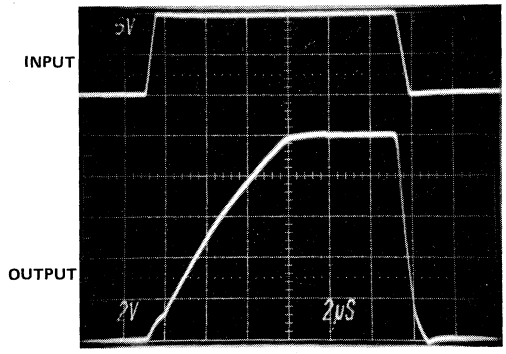
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 50k\Omega$
3. $C_L = 50pf$
4. $R_L = 50k\Omega$; Full Power Bandwidth guaranteed based on Slew Rate measurement using:
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$$
5. $V_O = +3.5V$ (Source), +1.5V (Sink)
6. Settling Time is measured to 0.1% of final value for a 3V output step and $A_V = -1$.

SLEW RATE AND TRANSIENT RESPONSE
TEST CIRCUIT



LARGE SIGNAL RESPONSE

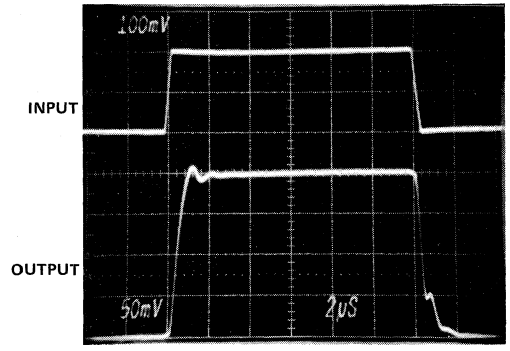
Vertical Scale: (Volts: Input = 5V/Div.)
(Volts: Output = 2V/Div.)
Horizontal Scale: (Time: 2μs/Div.)



+VSUPPLY = +15V, -VSUPPLY = -15V

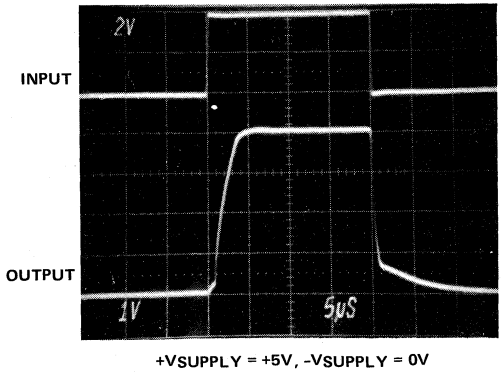
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)



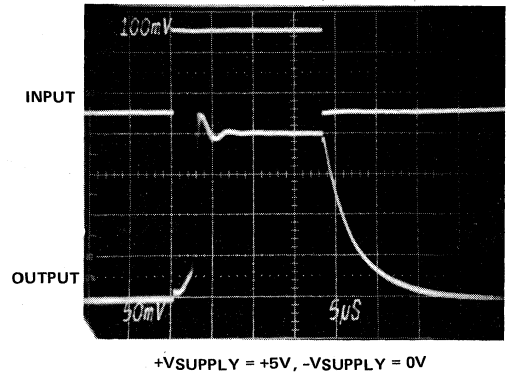
+VSUPPLY = +15V, -VSUPPLY = -15V

Vertical Scale: (Volts: Input = 2V/Div.)
(Volts: Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



+VSUPPLY = +5V, -VSUPPLY = 0V

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)

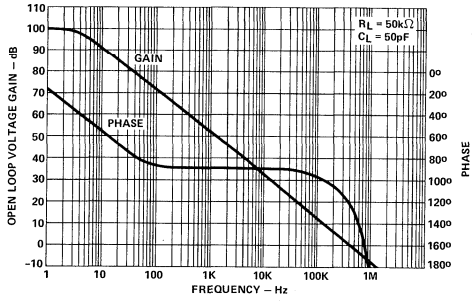


+VSUPPLY = +5V, -VSUPPLY = 0V

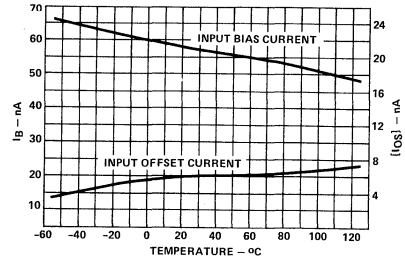
PERFORMANCE CURVES

$V_S = \pm 2.5V$, $T_A = +25^oC$ Unless Otherwise Stated

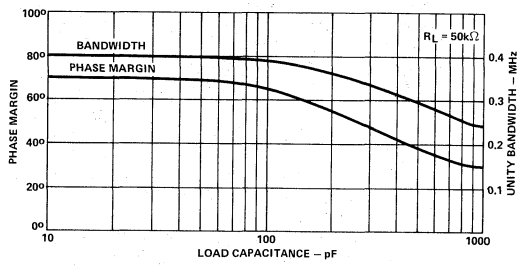
OPEN LOOP FREQUENCY RESPONSE



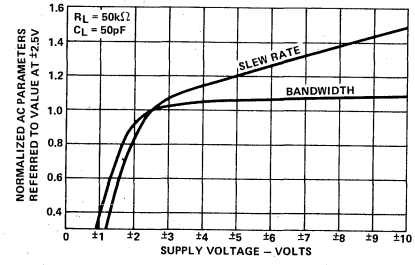
INPUT OFFSET CURRENT AND BIAS CURRENT VS. TEMPERATURE



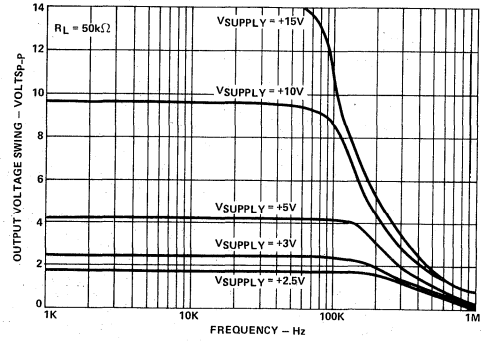
BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



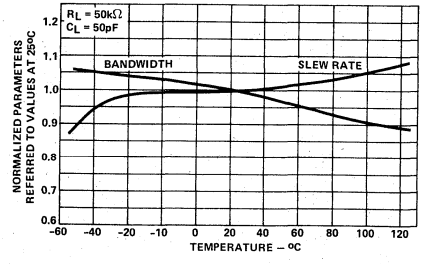
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



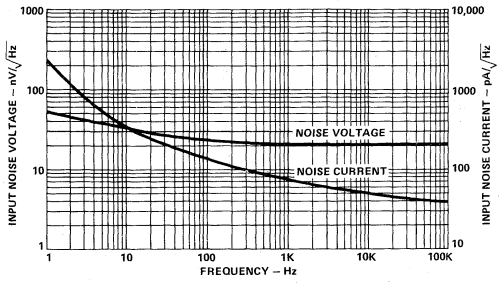
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SINGLE SUPPLY VOLTAGE



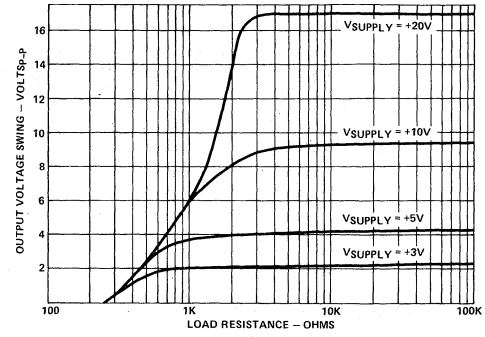
NORMALIZED AC PARAMETERS VS. TEMPERATURE



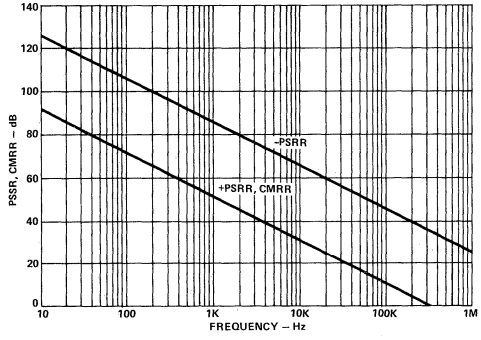
INPUT NOISE VS. FREQUENCY



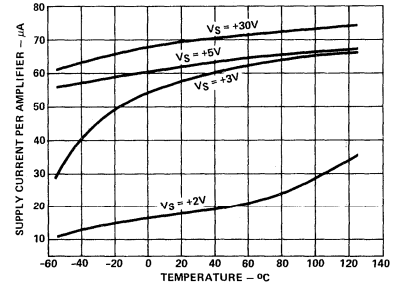
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



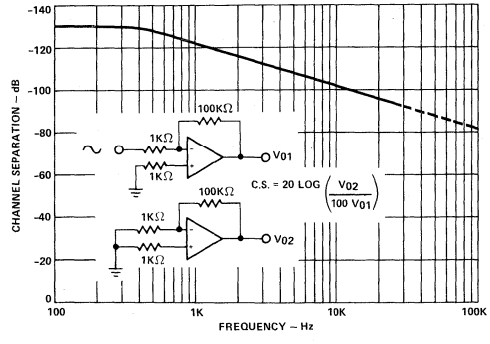
PSRR AND CMRR VS. FREQUENCY



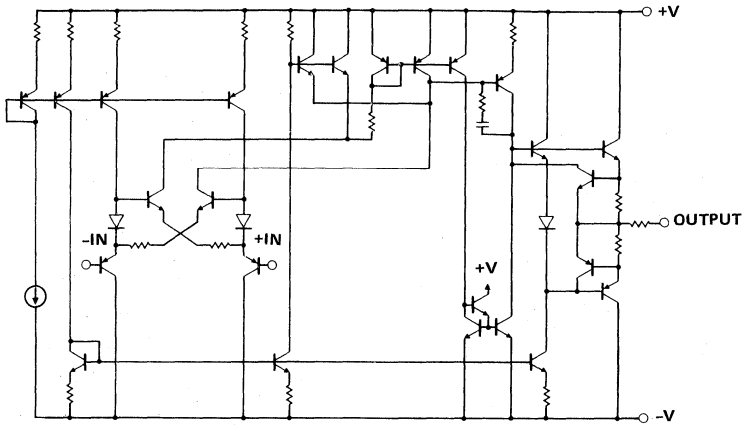
POWER SUPPLY CURRENT VS. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION VS. FREQUENCY



SCHEMATIC



HARRIS

ADVANCE

HA-5147

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifiers

FEATURES

- HIGH SPEED — 35V/μs
- WIDE GAIN BANDWIDTH — 120MHz
- LOW NOISE — 3.5nV/$\sqrt{Hz}$ at 1KHz
- LOW V_{OS} — 10μV
- HIGH CMRR/PSRR — 120dB
- HIGH GAIN — 1800V/mV

APPLICATIONS

- LOW LEVEL MULTIPLEXED TRANSDUCER SIGNAL AMPLIFIERS
- HIGH FIDELITY AUDIO PREAMPLIFIERS
- PULSE/RF AMPLIFIERS
- INSTRUMENTATION AMPLIFIERS
- SIGNAL CONDITIONERS/GENERATORS

DESCRIPTION

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3.5nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of feature include, low V_{OS} (10μV), wide gain-bandwidth (120MHz), high open loop gain (1800V/mV), and high CMRR/PSRR (120dB). Additionally, this flexible device operates over a wide supply range ($\pm$5V to $\pm$20V) while consuming only 140mW of power.

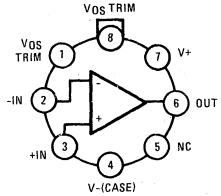
Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

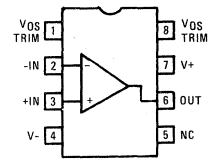
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include, instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

This device can easily be used as a design enhancement by directly replacing the 725, OP-05, OP-06, and OP-07 where gains are greater than ten.

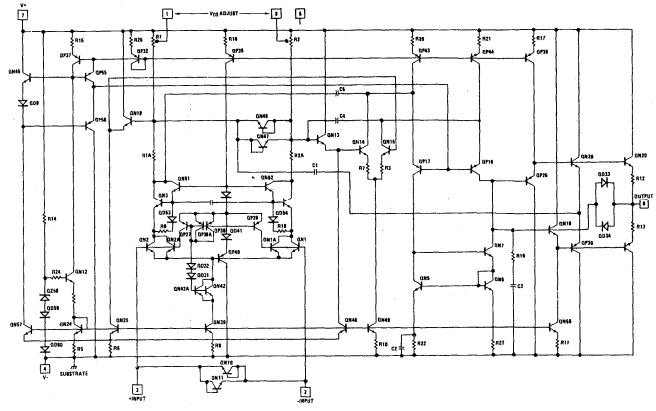
PINOUTS

TOP VIEWS





SCHEMATIC



HA-5160/5162

Wideband, JFET Input, High Slew Rate, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 100MHz
- HIGH SLEW RATE 120V/μs
- SETTLING TIME (0.2%) 280ns
- POWER BANDWIDTH 1000kHz
- OFFSET VOLTAGE 1.0mV
- BIAS CURRENT 20pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

The HA-5160/5162 is a wideband, uncompensated, operational amplifier manufactured with FET/Bipolar technologies and dielectric isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

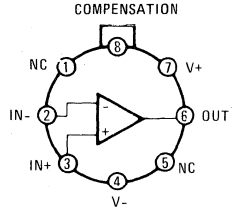
The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.* The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

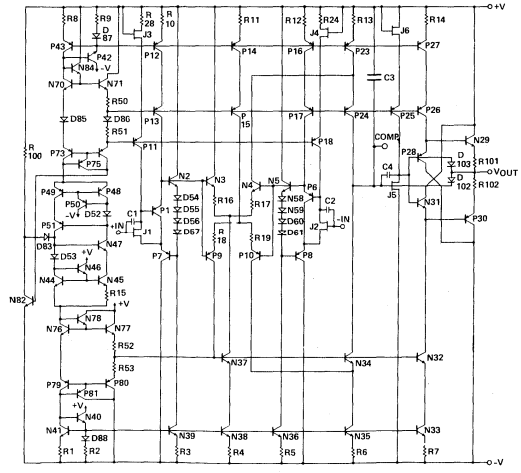
PINOUT

TOP VIEW



Case connected to V-

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	675mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

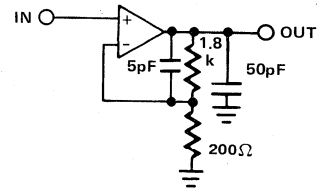
		HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to 75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	TYP	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		1.0	3.0		1.0	3.0		3	15	mV
	Full		3.0	5.0		3.0	5.0		5	20	mV
Offset Voltage Average Drift	Full		10			20			20	35	μV/°C
Bias Current	+25°C		20	50		20	50		20	65	pA
	Full		5	10			10			10	nA
Offset Current	+25°C		2	10		2	10		2	10	pA
	Full		2	5		2	5		2	5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±11		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		25K	100K		V/V
	Full	60K	100K		60K	100K		25K	75K		V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80		74	80		70	80		dB
Gain Bandwidth Product (A_V = 10)	Full		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±10	±11		±10	±11		±10	±11		V
	Full	±10	±11		±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	±5	±10		±5	±10		±5	±10		mA
Full Power Bandwidth (Note 7)	+25°C		1000			1000			1000		kHz
Output Resistance (Note 8)	+25°C		50			50			50		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		ns
Slew Rate (A_V = 10)	+25°C	100	120		100	120		50	70		V/μs
Settling Time (Note 10)	+25°C		280			280			400		ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		8.0	10		8.0	10		8.0	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86		74	86		70	86		dB

NOTES:

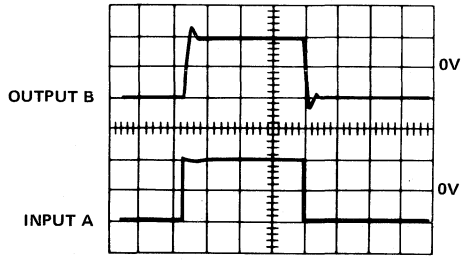
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2k$
4. $V_{CM} = \pm 10V$ DC.
5. $R_L = 2k$
6. $V_{OUT} = 0V$
7. $R_L = 2k$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE.}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and $A_V = 10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to $\pm 20V$ DC.

TEST CIRCUITS

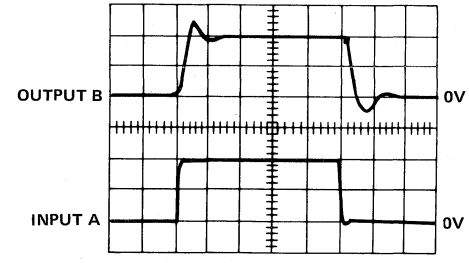
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



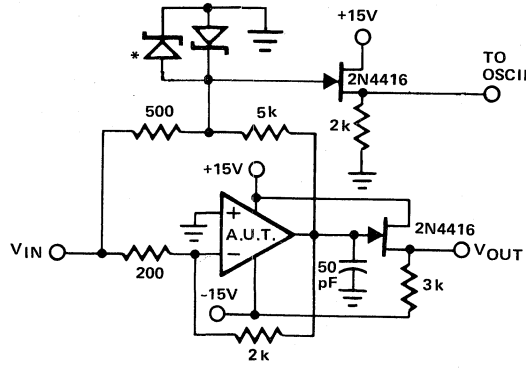
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 0.5V/Div., B = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: A = 10mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



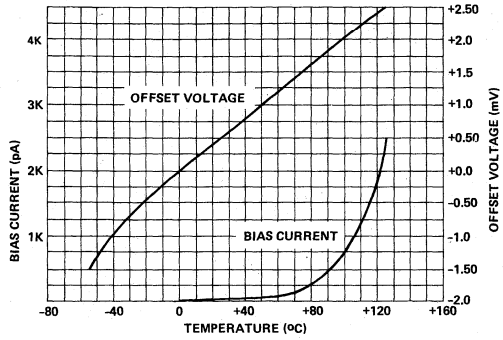
SETTLING TIME CIRCUIT



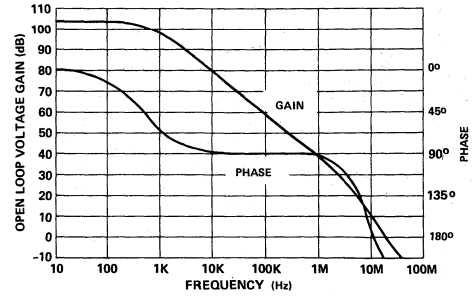
- $A_V = -10$
- Feedback and summing resistors should be 0.1%.

* Clipping Diodes are optional. HP5082-2810 recommended.

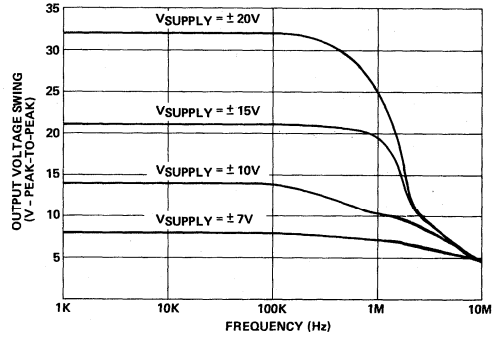
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



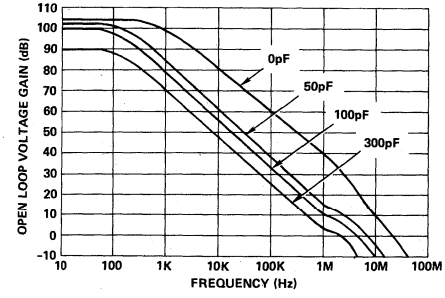
OPEN LOOP FREQUENCY RESPONSE



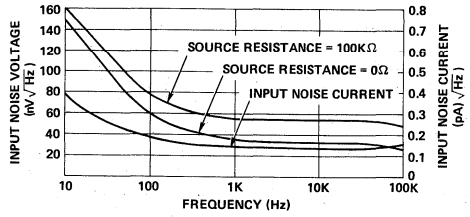
OUTPUT VOLTAGE SWING VS. FREQUENCY



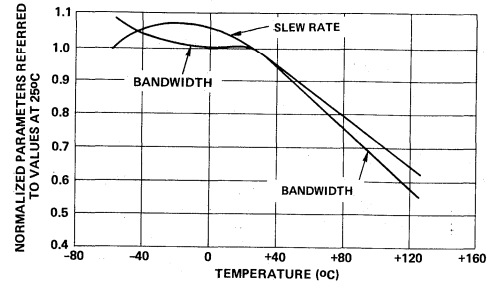
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES



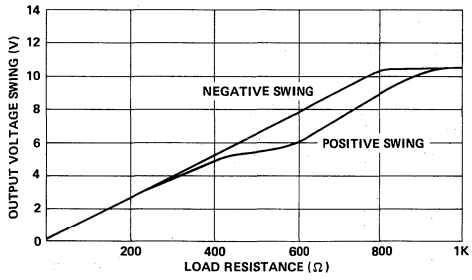
INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY



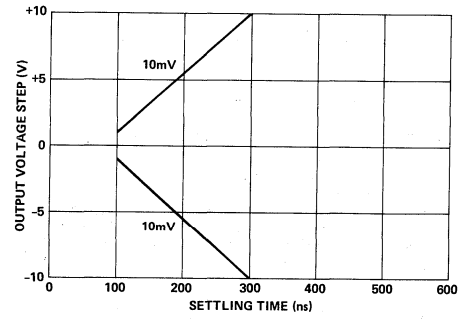
NORMALIZED AC PARAMETERS VS. TEMPERATURE



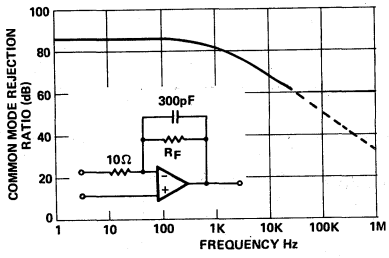
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



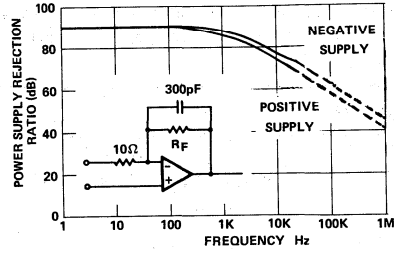
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



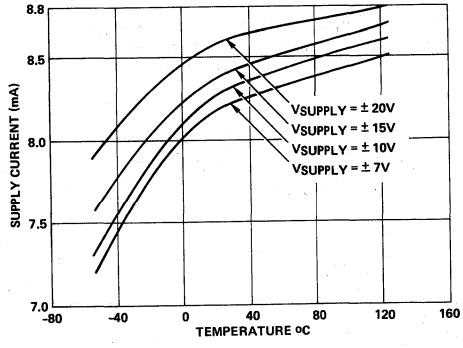
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE



APPLYING THE HA-5160/5162

1. POWER SUPPLY DECOUPLING: Although not absolutely necessasry, it is recommended that all power supply lines be decoupled with 0.01 μF ceramic capacitors to ground decoupling capacitors should be located as near to the amplifier terminals as possible.

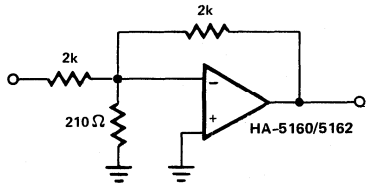
2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device. This small capacitor compensates for the input capacitance of the FET.

3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor ($\approx$100Ω) be connected in series with the output of the device and inside the feedback loop.

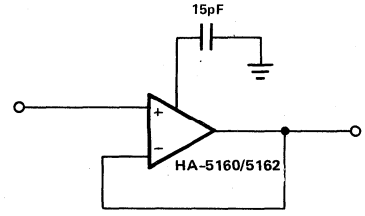
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY *

INVERTING

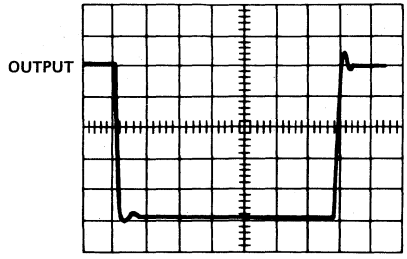


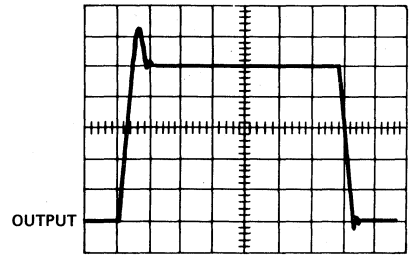
NONINVERTING



*VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME

VERTICAL SCALE: (VOLTS: 2V/DIV.)
HORIZONTAL SCALE: (TIME: 500ns/DIV.)





HARRIS

HA-5170

Precision JFET Input Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE — 100μV
- LOW OFFSET VOLTAGE DRIFT — 2μV/°C
- LOW NOISE — 10nV/$\sqrt{Hz}$
- HIGH OPEN LOOP GAIN — 600K V/V
- WIDE BANDWIDTH — 5MHz

APPLICATIONS

- HIGH GAIN INSTRUMENTATION AMPLIFIERS
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

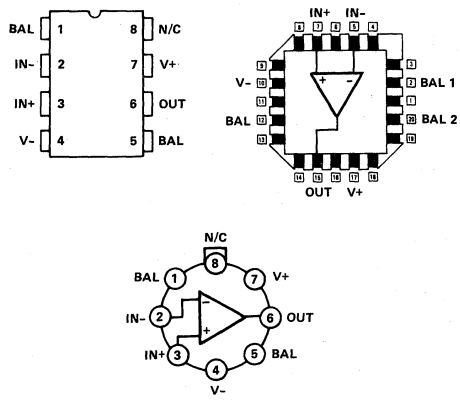
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems.

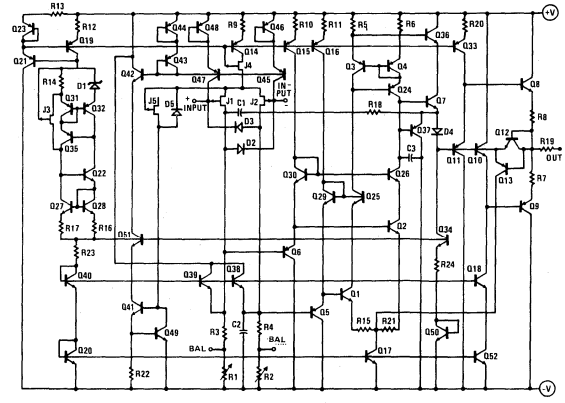
Packaged in an 8-pin (TO-99) can or an 8 lead Minidip, the HA-5170 is pin compatible with most existing op amp configurations.

PINOUT

TOP VIEWS



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated

Voltage Between V+ and V-Terminals	44.0V	Power Dissipation (Note 2)	675mW
Differential Input Voltage	± 30.0V	Operating Temperature Range	
		HA-5170-2	$-55^oC \leq T_A \leq +125^oC$
		HA-5170-5	$0^oC \leq T_A \leq +75^oC$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

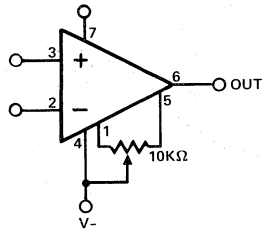
ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5170-2 MIN	HA-5170-2 TYP	HA-5170-2 MAX	HA-5170-5 MIN	HA-5170-5 TYP	HA-5170-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.3		0.1	0.3	mV
	Full			0.5			0.5	mV
Average Offset Voltage Drift (Note 3)	Full		2	5		2	5	µV/°C
Bias Current	+25°C		20	100		20	100	pA
	Full		3	30		0.1	2	nA
Bias Current Average Drift	Full		3			3		pA/°C
Offset Current	+25°C		3	30		3	60	pA
	Full			5			0.1	nA
Offset Current Average Drift	Full		0.3			0.3		pA/°C
Common Mode Range	Full	±10	+15.1 -12		±10	+15.1 -12		V
Differential Input Resistance	+25°C		6×10^{10}			6×10^{10}		Ω
Input Capacitance	+25°C		12			12		pF
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C		0.5	5		0.5	5	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							
f_O = 10Hz			20	150		20	150	$nV/\sqrt{Hz}$
f_O = 100Hz			12	50		12	50	$nV/\sqrt{Hz}$
f_O = 1000Hz			10	25		10	25	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 3)	+25°C							
f_O = 10Hz			.05			.05		$pA/\sqrt{Hz}$
f_O = 100Hz			.01			.01		$pA/\sqrt{Hz}$
f_O = 1000Hz			.01			.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	300K	600K		300K	600K		V/V
	Full	200K			250K			V/V
Common Mode Rejection Ratio (Note 5)	Full	85	100		90	100		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
Full Power Bandwidth (Note 7)	+25°C	80	120		80	120		kHz
Output Current (Note 8)	+25°C	±10			±10			mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		45	100		45	100	ns
Slew Rate	+25°C	5	8		5	8		V/µs
Settling Time (Note 10)	+25°C		1			1		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.9	2.5		1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		90	105		dB

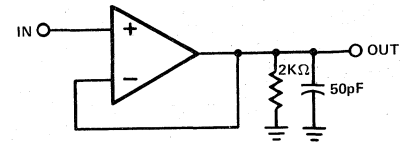
NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2k.
5. V_{CM} = ±10V D. C.
6. R_L = 2kΩ.
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V.
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. V_{SUPP} = ±5V D. C. to ±20V D. C.

V_{OS} ADJUSTMENT

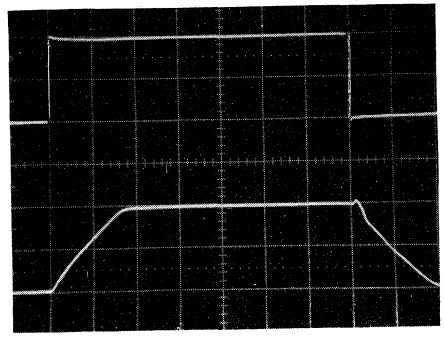


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



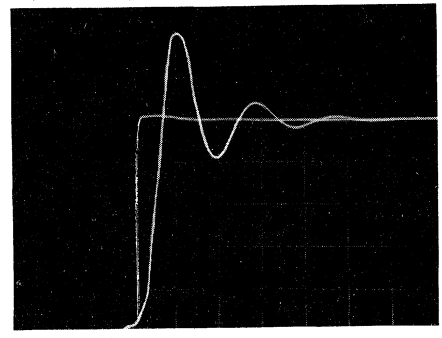
LARGE SIGNAL RESPONSE

VERTICAL SCALE: 5V/Div.
HORIZONTAL SCALE: 500ns/Div.

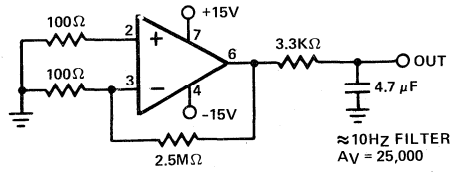


SMALL SIGNAL RESPONSE

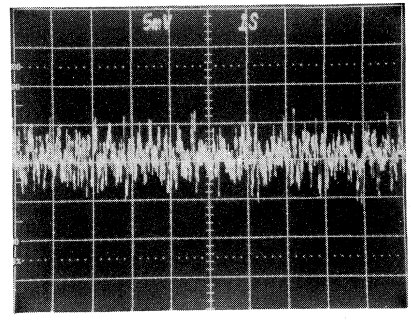
VERTICAL SCALE: 10mV/Div.
HORIZONTAL SCALE: 100ns/Div.



LOW FREQUENCY NOISE TEST CIRCUIT

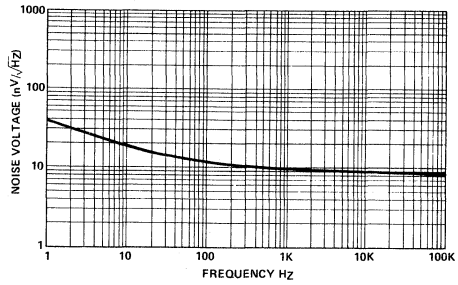


HA-5170 LOW FREQUENCY NOISE (0.1HZ To 10HZ)

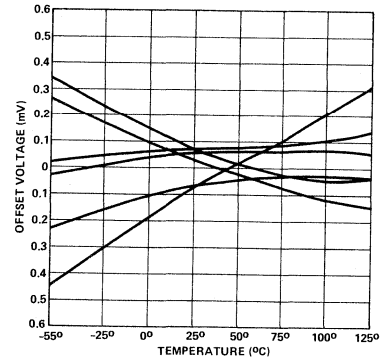


VERTICAL SCALE: 200nV/Div. (Noise Referred to Input)
5mVDiv. At Output, A_{VCL} = 25,000
HORIZONTAL SCALE: 1 Sec./Div.

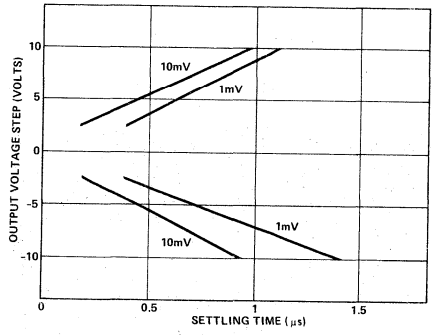
INPUT VOLTAGE NOISE VS. FREQUENCY



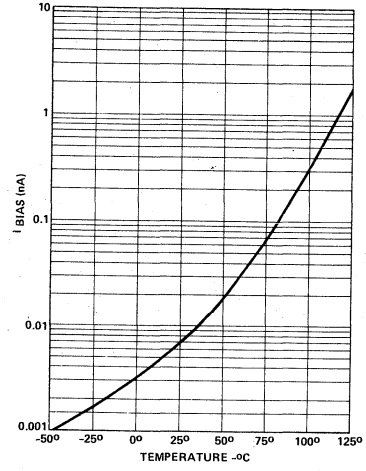
OFFSET VOLTAGE VS. TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



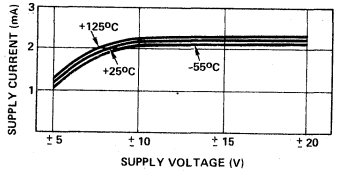
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



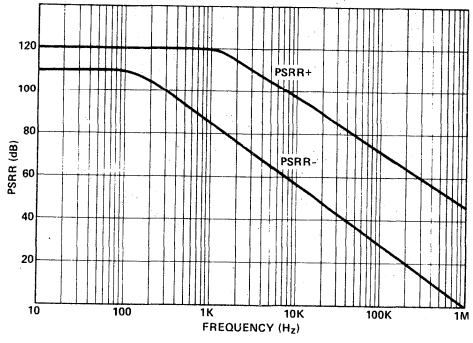
BIAS CURRENT VS. TEMPERATURE



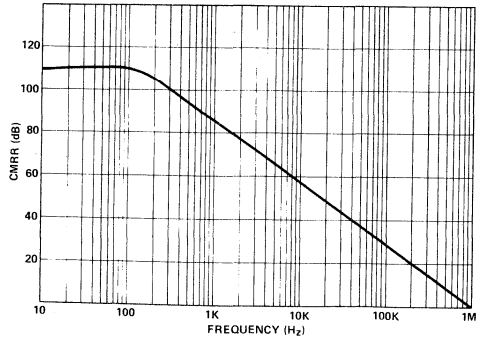
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE & TEMPERATURE



POWER SUPPLY REJECTION RATIO VS. FREQUENCY

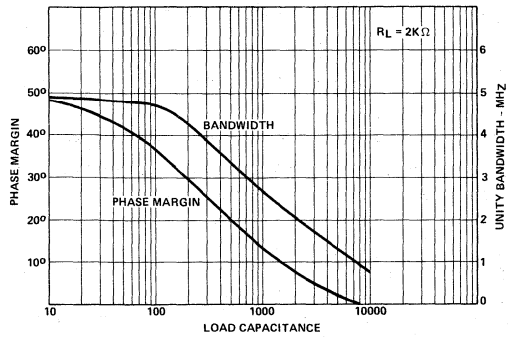


COMMON MODE REJECTION RATIO VS. FREQUENCY

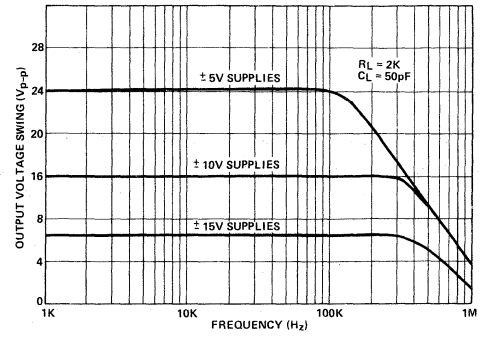


PERFORMANCE CURVES (Continued)

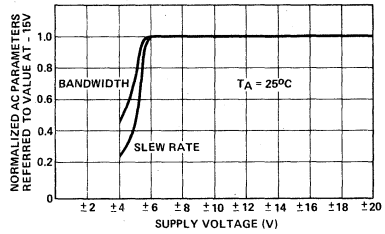
SMALL SIGNAL BANDWIDTH & PHASE MARGIN VS. LOAD CAPACITANCE



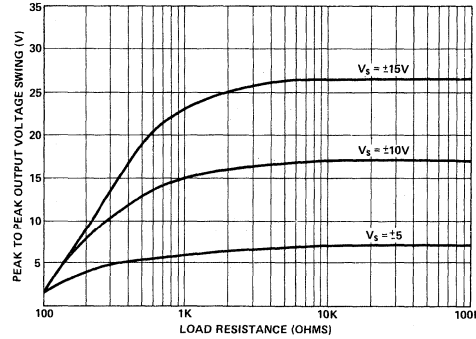
OUTPUT VOLTAGE SWING VS. FREQUENCY & SUPPLY VOLTAGE



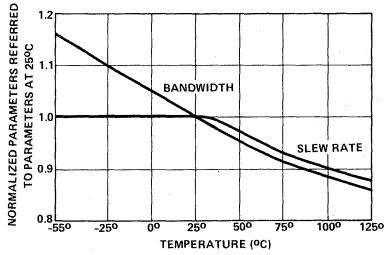
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



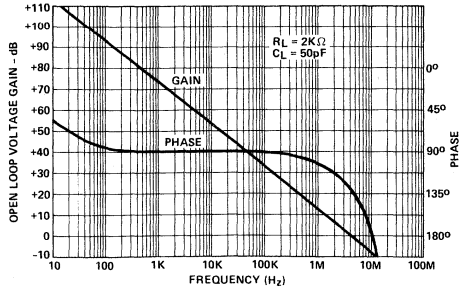
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



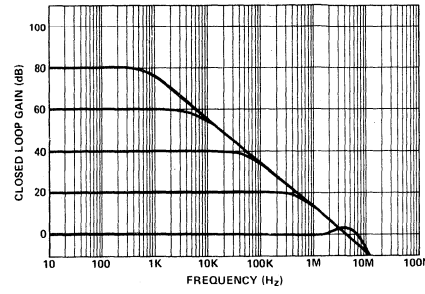
NORMALIZED AC PARAMETERS VS. TEMPERATURE



OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



HA-5180/5180A

Low Bias Current, Low Power JFET Input Operational Amplifier

FEATURES

- ULTRA LOW BIAS CURRENT 250fA
- LOW POWER SUPPLY CURRENT 0.8mA
- LOW OFFSET VOLTAGE 0.5mV (max.)
- BANDWIDTH 2MHz
- SLEW RATE 7V/μs

APPLICATIONS

- ELECTROMETER AMPLIFIER DESIGNS
- PHOTO CURRENT DETECTORS
- PRECISION, LONG-TERM INTEGRATORS
- LOW DRIFT SAMPLE & HOLD CIRCUITS
- VERY HIGH IMPEDANCE BUFFERS
- HIGH IMPEDANCE BIOLOGICAL MICRO PROBES

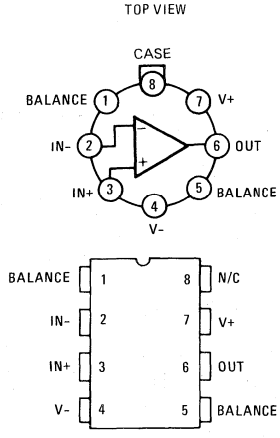
DESCRIPTION

The HARRIS HA-5180/5180A is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typ.) available in any monolithic operational amplifier. The HA-5180/5180A has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage. For applications which require precision performance the HA-5180A offers an input offset voltage of 0.5mV (max.) while the HA-5180 offers 3mV (max.)

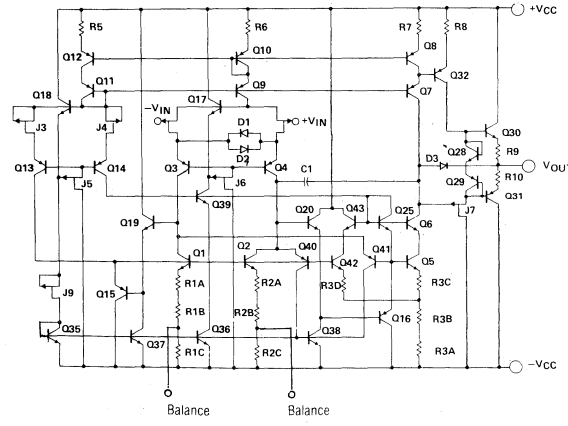
The HA-5180/5180A also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2MHz bandwidth and 7V/μs slew rate of the HA-5180/5180A extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

The HA-5180/5180A is packaged in a 8-pin (TO-99) can and an 8-lead cerdip and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance.

PINOUT



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated

Voltage Between V+ and V- Terminals 40V

Differential Input Voltage ±40V

Output Short Circuit Duration Indefinite

Power Dissipation (Note 2) 300mW

Operating Temperature Range

HA-5180/5180A-2 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

HA-5180/5180A-5 $0^{\circ}C \leq T_A \leq +75^{\circ}C$

Storage Temperature Range $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL RATINGS V+ = 15V, V- = -15V

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.5		0.1	0.5	mV
	Full			1			1	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage, 0.1Hz to 10Hz	+25°C		5			5		µVp-p
Input Noise Voltage Density	+25°C							
fo = 10Hz			200			200		$nV/\sqrt{Hz}$
fo = 100Hz			120			120		$nV/\sqrt{Hz}$
fo = 1000Hz			70			70		$nV/\sqrt{Hz}$
Input Noise Current (f=1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Overshoot	+25°C		30	50		30	50	%
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

ELECTRICAL RATINGS V+ = 15V, V- = -15V

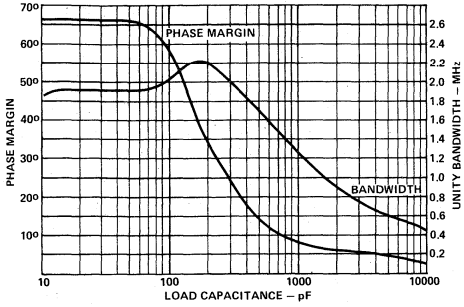
PARAMETER	TEMP.	5180-2 MIN	5180-2 TYP	5180-2 MAX	5180-5 MIN	5180-5 TYP	5180-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1	3		1	3	mV
	Full			4			4	mV
Average Offset Voltage Drift	Full		5			5		μV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage, 0.1Hz to 10Hz	+25°C		5			5		Vp-p
Input Noise Voltage Density	+25°C							
fo = 10Hz			200			200		$nV/\sqrt{Hz}$
fo = 100Hz			120			120		$nV/\sqrt{Hz}$
fo = 1000Hz			70			70		$nV/\sqrt{Hz}$
Input Noise Current (f=1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Overshoot	+25°C		30	50		30	50	%
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/μs
Settling Time (Note 10)	+25°C		2			2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

NOTES:

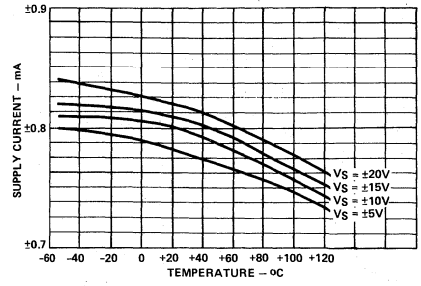
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. V_{OUT} = ±10V; R_L = 2k. Gain dB = 20 log $_{10}$Av.
5. V_{CM} = ±10V D.C.
6. R_L = 2k
7. R_L = 2k, V_{peak} = 10V; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = ±10V.
9. Output resistance specified under open loop conditions (f = 100Hz)
10. Settling time is specified to 0.1% of final value for a 10V output step and A_V = -1.
11. V_{SUPP} = ±5V D.C. to ±20V D.C.

PERFORMANCE CURVES

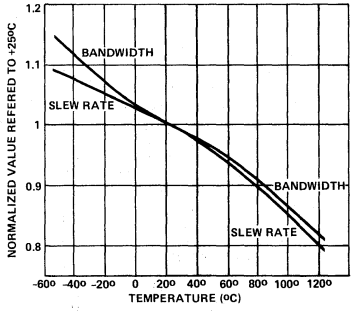
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



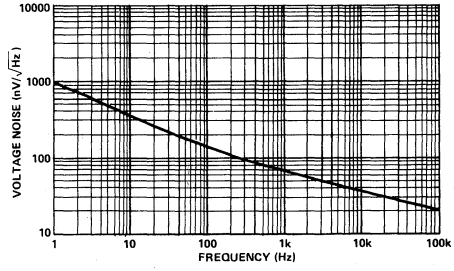
SUPPLY CURRENT VS. TEMPERATURE



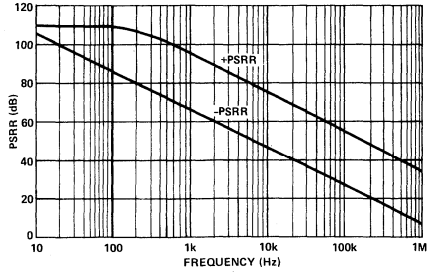
NORMALIZED AC PARAMETERS VS. TEMPERATURE



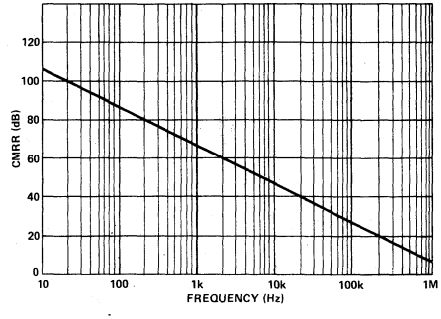
INPUT VOLTAGE NOISE VS. FREQUENCY



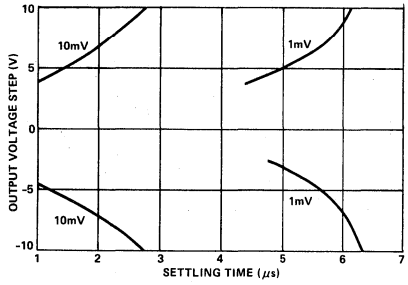
PSRR VS. FREQUENCY



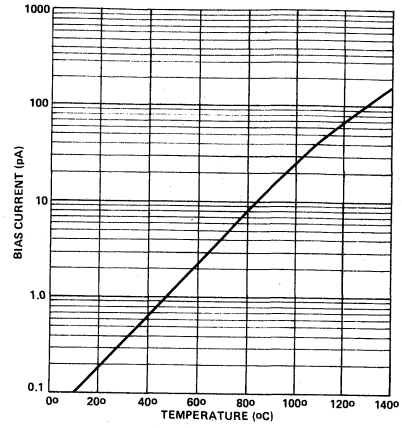
CMRR VS. FREQUENCY



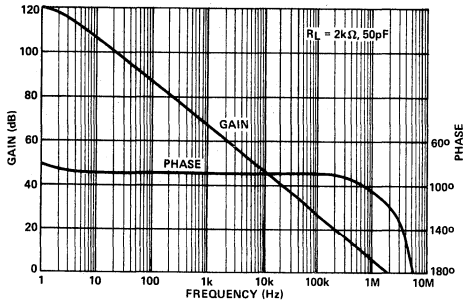
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



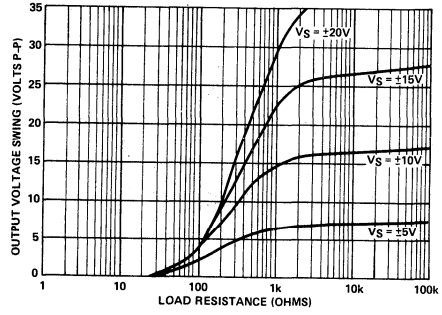
BIAS CURRENT VS. TEMPERATURE



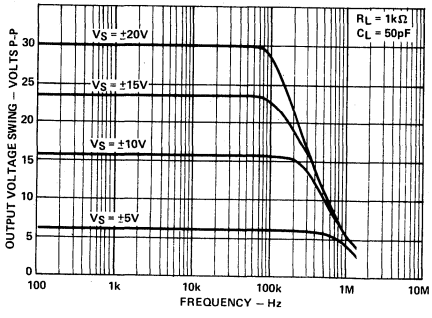
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



OUTPUT VOLTAGE SWING VS. FREQUENCY



APPLICATION HINTS

The HA-5180/5180A offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180/5180A care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180/5180A allows easy installation at the signal source or inside a probe. The HA-5180/5180A is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

If it is not possible to place the HA-5180 very close to the signal source then the use of shielded coaxial cable will offer the best isolation of the high impedance signal line from external noise sources. However, the effects of leakage, capacitance and vibrational noise should be taken into account when using coaxial cables. Leakage can be minimized by using cables with very high insulation resistance (such as polyethylene or Virgin Teflon). For example, the current to voltage converter circuit (as shown in Fig. 1) will eliminate leakage across the insulation of the cable by forcing the signal line to the same potential as the shield. This circuit also provides fast response to input signals because the cable capacitance is never forced to be charged or discharged. However, the cable capacitance directly increases the input capacitance of the circuit and could cause the circuit to become unstable; if so, adding capacitance across Rf will stablilize the circuit again. Leakage can also be reduced in the high-impedance non-inverting configuration (see Fig. 2) by bootstrapping the shield to the same potential as the signal source instead of ground. If low closed-loop gains are used, the non-inverting configuration could also become unstable due to the positive feedback to the input through the cable capacitance. One method of compensating this circuit is to place a small (low leakage) capacitor from the input to ground. This technique will also reduce the effective capacitance presented to the signal source. When large closed-loop gains and/or long cable lengths are used, a buffer should be added to the circuit to drive the shield.

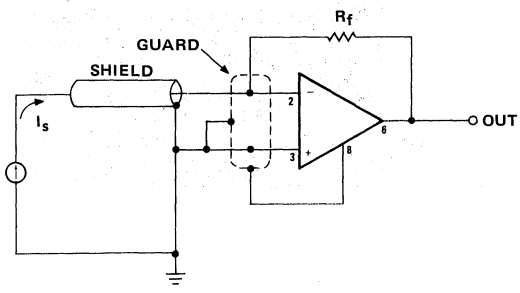


Figure 1. CURRENT TO VOLTAGE CONVERTER

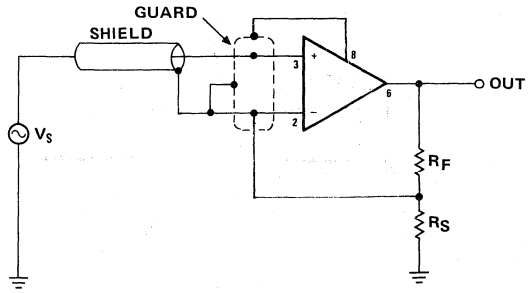


Figure 2. VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

When using coaxial cable with the HA-5180 the cable should be kept as rigid and vibration free as possible. Frictional movement of the shield over the insulation can generate electrical charge which is picked up by the high impedance signal line as noise. Movement and bending of the cable can also cause charge. movement due to small changes in cable capacitance and capacitance to surrounding objects. Another source of noise currents is that which is generated by the movement of a conductor in a magnetic feild.

For lowest leakage at the device inputs either use a teflon IC socket or connect the signal line to the HA-5180/5180A inputs using teflon standoffs. A guard ring, as shown in Fig. 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents across the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon, rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments. A good quality conformal coating with low dielectric absorption provides the best protection from humidity and contamination.

Input protection is generally not necessary when designing with the HA-5180/5180A. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180/5180A to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degradation of performance.

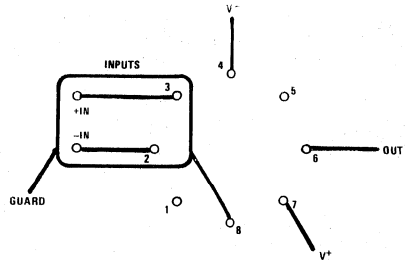


Figure 3. GUARD RING EXAMPLE

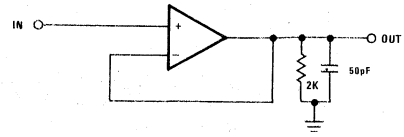


Figure 4. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

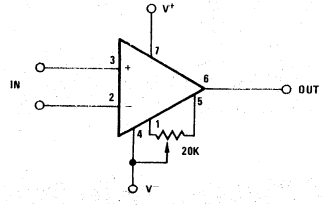
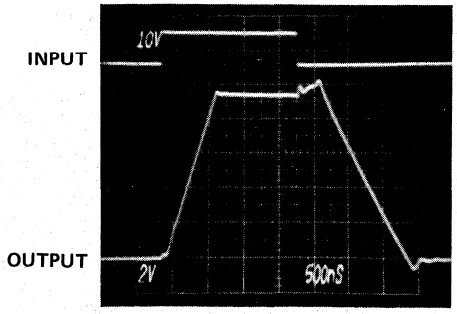


Figure 5. SUGGESTED OFFSET ADJUSTMENT CIRCUIT

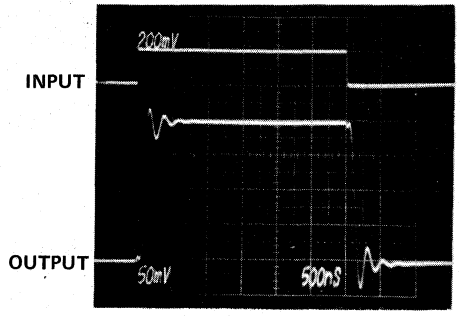
LARGE SIGNAL RESPONSE

VERTICAL SCALE (Volts: 5V/DIV INPUT)
(Volts: 2V/DIV OUTPUT)
HORIZONTAL SCALE (TIME: 500ns/DIV)



SMALL SIGNAL RESPONSE

VERTICAL SCALE (Volts: 100mV/DIV INPUT)
(Volts: 50mV/DIV OUTPUT)
HORIZONTAL SCALE (TIME: 500ns/DIV)



HARRIS

HA-5190/5195

Wideband, Fast Settling Operational Amplifier

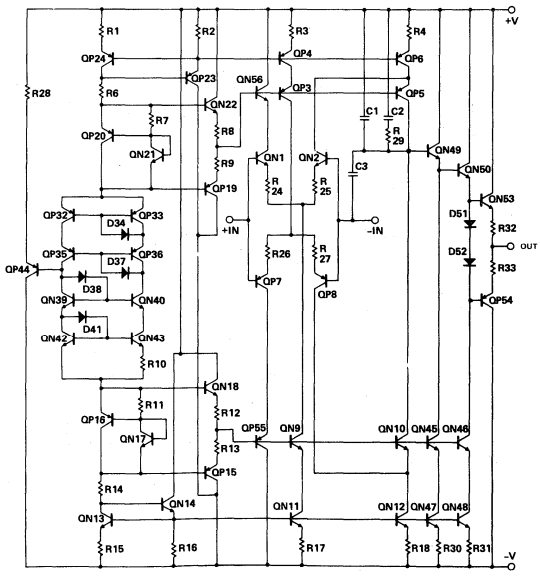
FEATURES

- FAST SETTLING TIME — 70ns
- VERY HIGH SLEW RATE — 200V/μs
- WIDE GAIN-BANDWIDTH — 150MHz
- POWER BANDWIDTH — 6.5MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- REPLACE COSTLY HYBRIDS

SCHEMATIC



GENERAL DESCRIPTION

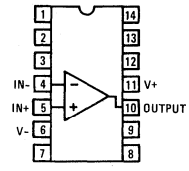
HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

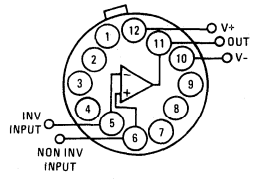
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2). HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

PINOUTS

TOP VIEWS





CASE TIED TO V-

LH0032 PINOUT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; $R_L = 200$ ohms, unless otherwise specified.

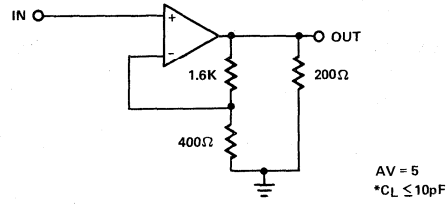
		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		1	4		1	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/µs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 200\Omega, C_L < 10pF$, $V_O = \pm 5V$
4. $V_{CM} = \pm 5V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 5$ VDC to ± 15 VDC

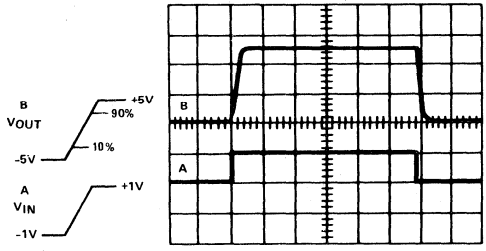
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*



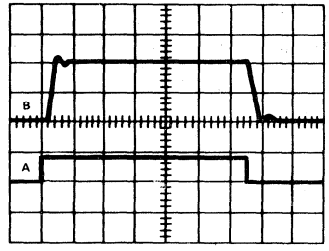
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 4.0V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

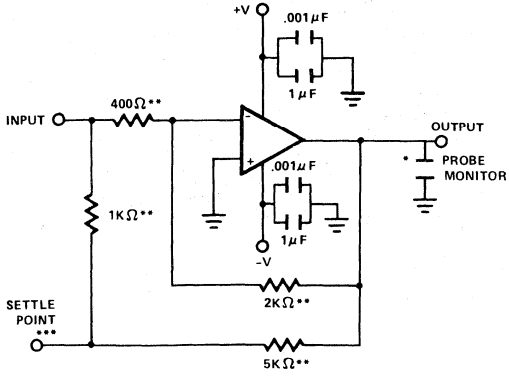


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=50mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT



* Load Capacitance should be less than 10pF.

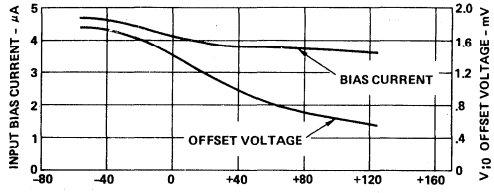
** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

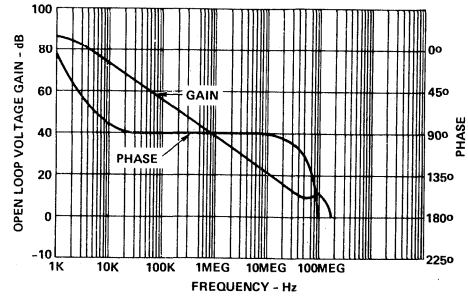
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

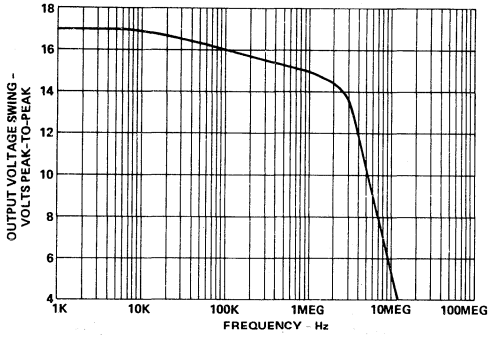
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



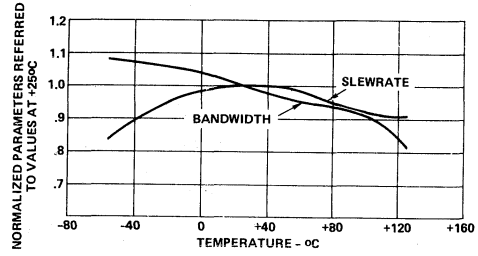
OPEN LOOP FREQUENCY RESPONSE



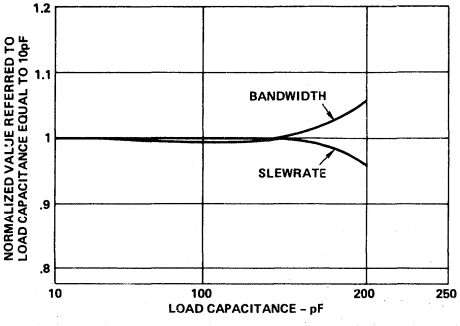
OUTPUT VOLTAGE SWING VS. FREQUENCY



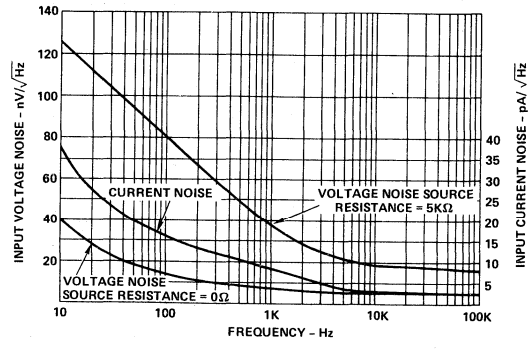
NORMALIZED AC PARAMETERS VS. TEMPERATURE



NORMALIZED AC PARAMETERS VS. LOAD CAPACITANCE

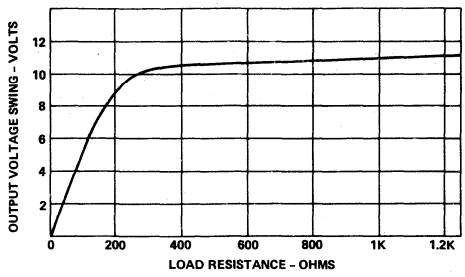


INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY

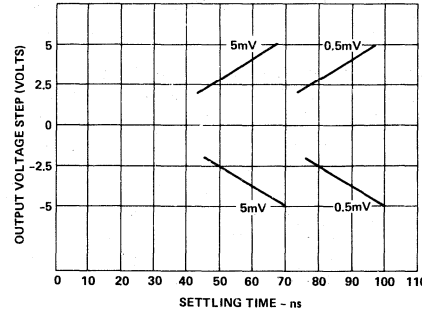


PERFORMANCE CURVES (Continued)

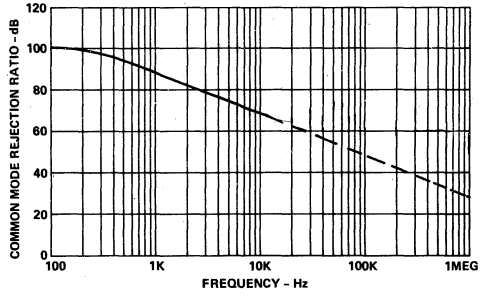
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



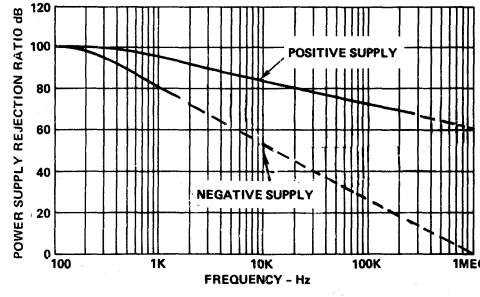
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



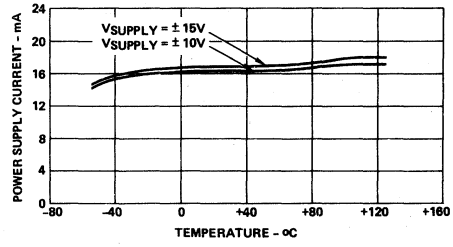
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE



APPLYING THE HA-5190/5195

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains ≥ 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

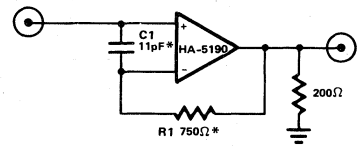
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.

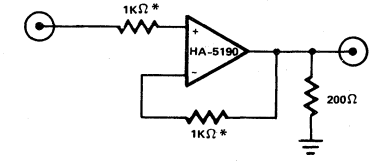
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.

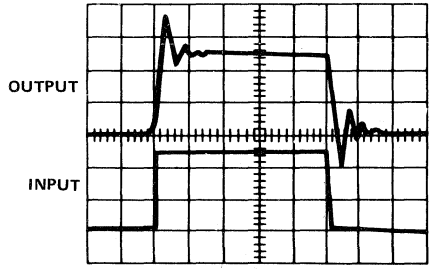
APPLICATIONS

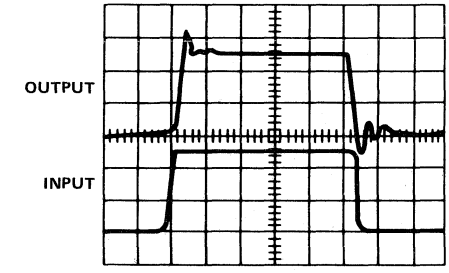
SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

NONINVERTING







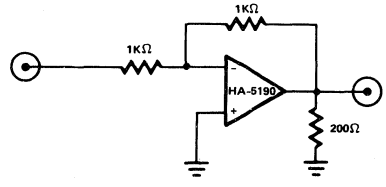


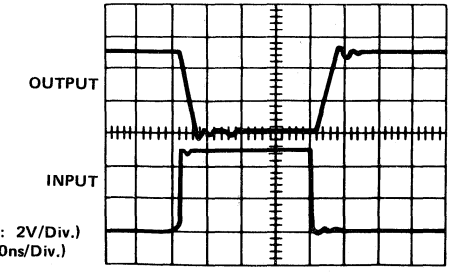
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

* Values were determined experimentally for optimum speed and settling time.

R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

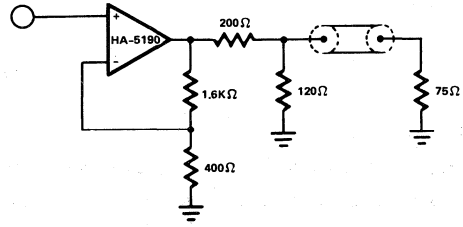
INVERTING



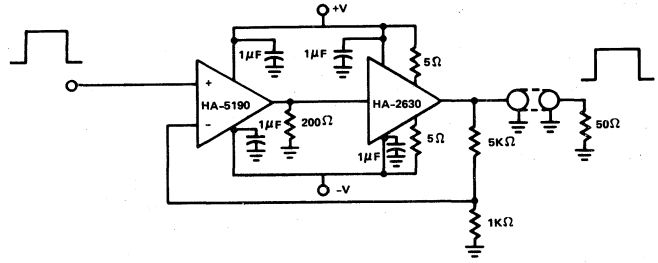


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

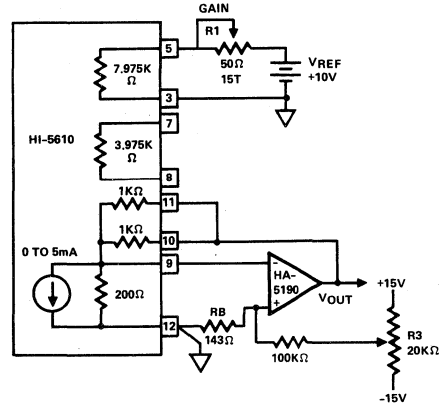
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

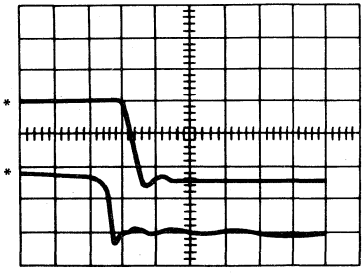


VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER



FAST DAC OUTPUT BUFFER





Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

B = V_{OUT} C = DIGITAL INPUT

* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

HARRIS

HA-23080

Operational Transconductance Amplifier

Preliminary

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE 50V/μs
- ADJUSTABLE/GATEABLE GAIN
- LOW OFFSET CURRENT 120nA
- ADJUSTABLE POWER CONSUMPTION

APPLICATIONS

- USE AS BUILDING BLOCKS FOR:
- MULTIPLEXERS
- SAMPLE AND HOLD CIRCUITS
- COMPARATORS
- VOLTAGE FOLLOWERS

DESCRIPTION

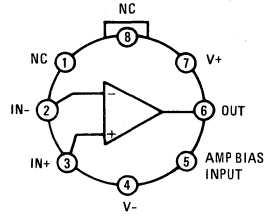
HA-23080 is an operational transconductance amplifier offering an unique blend of DC and AC electrical characteristics coupled with a bias input control for additional versatility. Fabricated using Harris Semiconductor's standard dielectric isolation process, these gateable-gain blocks provide input characteristics such as 0.3mV offset voltage, 120nA offset current and 150μV/V offset voltage sensitivity. Combined with these input characteristics are outstanding dynamic specifications including 50V/μs slew rate and 2MHz bandwidth.

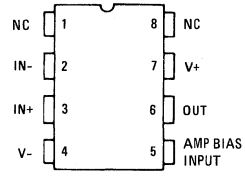
Using these features plus the flexibility afforded by the amplifier bias input, HA-23080 may be easily employed as the main component in multiplexer, comparator, multiplier, and sample/hold designs. This OTA is also useful as a fast voltage follower.

Using the popular operational amplifier pinout, HA-23080 comes available in 8 pin (TO-99) cans and 8 pin cerdips. Its specified temperature range is 0°C to +75°C for -5 and -55°C to +125°C for -2.

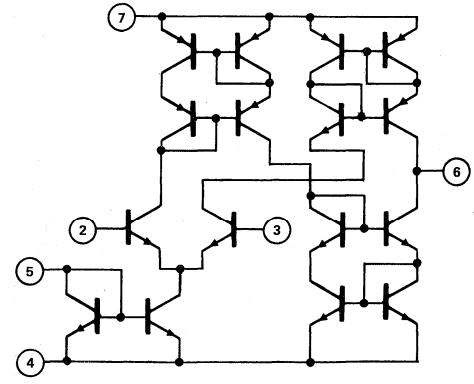
PINOUTS

TOP VIEWS





SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	36V	Power Dissipation	125mW
Differential Input Voltage	±5V	Operating Temperature Range	
Common Mode Input Voltage	V+ to V-	HA-23080-2	$-55^oC \leq T_A \leq +125^oC$
Input Signal Current	1mA	HA-23080-5	$0^oC \leq T_A \leq +75^oC$
Amplifier Bias Current	2mA	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Output Short Circuit Duration	Indefinite		

ELECTRICAL CHARACTERISTICS $V+ = 15V, V- = -15V$, $I_{ABC} = 500\mu A$ (unless Indicated Otherwise) (Note 2)

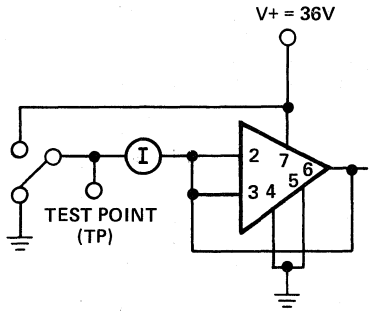
PARAMETER	TEMP.	HA-23080-2/-5 MINIMUM	HA-23080-2/-5 TYPICAL	HA-23080-2/-5 MAXIMUM	UNITS
INPUT CHARACTERISTICS					
Offset Voltage – $I_{ABC} = 5\mu A$	+25°C		0.3	2	mV
			0.4	2	mV
	Full			5	mV
Offset Voltage Change $I_{ABC} = 5\mu A$ to $I_{ABC} = 500\mu A$	+25°C		0.1	3	mV
Average Offset Voltage Drift – $I_{ABC} = 100\mu A$	Full		3	18	μV/°C
Bias Current	+25°C		2	5	μA
	Full			8	μA
$I_{ABC} = 500nA$	+25°C		2	5	nA
Offset Current	+25°C		0.12	0.6	nA
Common Mode Range	+25°C	±12	±13.6		V
Differential Input Current $I_{ABC} = 0, V_{DIFF} = 4V$	+25°C		0.008	5	nA
Leakage Current (See Test Circuit)					
$I_{ABC} = 0, V_{TP} = 0V$	+25°C		0.08	5	nA
$I_{ABC} = 0, V_{TP} = 36V$	+25°C		0.3	5	nA
Input Capacitance (Note 3)	+25°C		3.6		pF
Input Resistance	+25°C	10	26		kΩ
TRANSFER CHARACTERISTICS					
Forward Transconductance (Large Signal)	+25°C	7700	9900	15000	μmho
	Full	4000			μmho
Common Mode Rejection Ratio	+25°C	80	110		dB
Open Loop Bandwidth	+25°C		20		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 4) – $I_{ABC} = 5\mu A$	+25°C	±12	±13.8		V
	+25°C	±12	±13.5		V
Output Current (Note 5) – $I_{ABC} = 5\mu A$	+25°C	3	5	7	μA
	+25°C	350	500	750	μA
	Full	300			μA
Output Capacitance (Note 3)	+25°C		5.6		pF
Output Resistance	+25°C		15		MΩ
Input-to-Output Capacitance (Note 3)	+25°C		0.024		pF
TRANSIENT RESPONSE (See Test Circuit)					
Slew Rate – Compensated	+25°C		50		V/μs
Uncompensated	+25°C		75		V/μs
NOISE CHARACTERISTICS					
Total Input Noise Voltage (Note 6)	+25°C			12	μV_{PEAK}
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C	0.8	1	1.5	mA
Input Offset Voltage Sensitivity	+25°C			150	μV/V
Amplifier Bias Voltage	+25°C		0.71		V

NOTES:

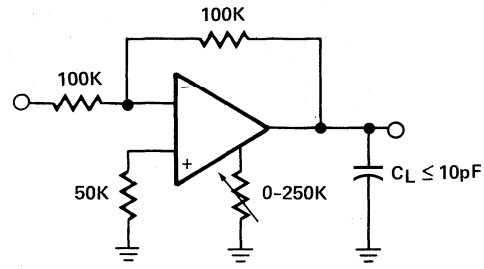
1. Absolute maximum ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. I_{ABC} (Amplifier Bias Current) The current supplied to the amplifier bias terminal (Pin 5) to establish its operating point.
3. f = 1MHz
4. $R_L = \infty$
5. $R_L = 0$
6. $V_S = \pm 8.5V$, $I_{ABC} = 500nA$, Bandwidth = 1kHz, $R_{SOURCE} = 100k\Omega$, Test Time = 30 sec.

TEST CIRCUITS

LEAKAGE CURRENT TEST CIRCUIT

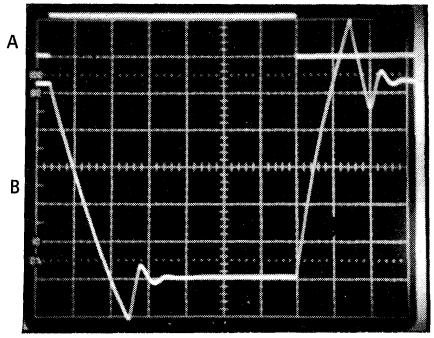


TYPICAL SLEW RATE TEST CIRCUIT



TYPICAL SLEW RATE WAVEFORMS

LARGE SIGNAL RESPONSE

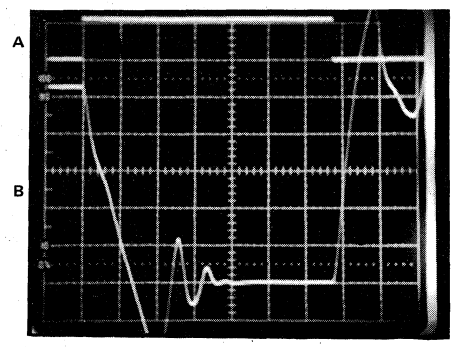


A = Input Signal
B = Output Signal
$I_{ABC} = 200\mu A$

Vertical Scale: A = 10V/Div.
B = 2V/Div.

Horizontal Scale: 0.5μs/Div.

LARGE SIGNAL RESPONSE



A = Input Signal
B = Output Signal
$I_{ABC} = 650\mu A$

Vertical Scale: A = 10V/Div.
B = 2V/Div.

Horizontal Scale: 0.2μs/Div.

HARRIS

HA-23551

Triple Current Sense Latch

Preliminary

FEATURES

- CURRENT SENSING WITH PRECISION THRESHOLD VOLTAGE
- LARGE COMMON MODE RANGE 3.5 TO 40V
- LOW SWITCHING DELAY 190ns
- OPEN COLLECTOR OUTPUT
- TTL COMPATIBLE RESET

APPLICATIONS

- CURRENT SENSING/CONTROL FOR SOLENOID DRIVERS
- PULSE BY PULSE CURRENT CONTROL FOR SWITCHING POWER SUPPLIES
- CURRENT SENSING/CONTROL FOR STEPPER MOTOR DRIVERS
- TEMPERATURE CONTROL CIRCUITS
- LASER DIODE CURRENT MONITORING AND CONTROL CIRCUITS

DESCRIPTION

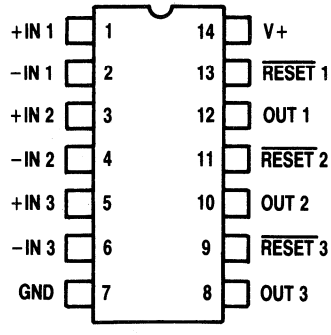
The HA-23551 triple current-sense latch is a monolithic device which employs the Harris Dielectric Isolation process and digital current-limiting techniques to overcome the speed and stability problems of linear approaches. Each current-sense latch consists of a comparator, latch circuit, open-collector output and TTL-compatible digital reset. Primarily designed for precise current monitoring and control in applications such as solenoid drivers, power supply circuits, stepper motor drivers, etc. The HA-23551 can also be used in conjunction with transducers to provide control of physical parameters such as temperature and pressure.

The input stage consists of a comparator which has a common-mode voltage range of 3.5 to 40V and whose threshold voltage is internally set by $I_{ref} \cdot R_T$ (360mV typ., see simplified schematic below). Whenever the differential input exceeds the input threshold voltage the comparator forces the open-collector output low. The output transistor switches within 190ns, is capable of sinking up to 1A and can directly drive VMOS or Bipolar power transistors. If the RESET input is at a logic "1" when the input threshold voltage is exceeded, a positive feedback signal equal to $2 \cdot I_{ref} \cdot R_T$ (720mV typ.) will be fed back to the comparator causing the output to latch in the "low" state. A logic "0" applied to $\overline{\text{RESET}}$ will release the positive feedback signal and cause the output transistor to turn "off" if the differential input voltage is below the threshold voltage.

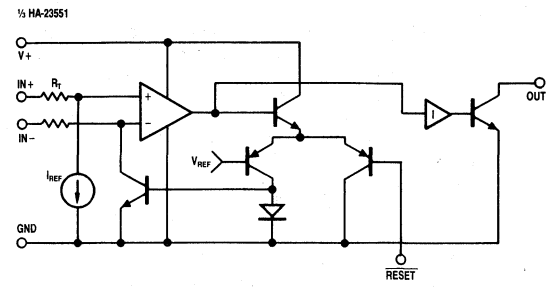
The HA-23551 is offered in a 14-pin cerdip or plastic package and is available in three different operating temperature ranges. The HA-23551-2 may be operated over the −55°C to +125°C military temperature range, the HA-23551-4 over the −25°C to +85°C industrial temperature range, and the HA-23551-5 over the 0°C to +75°C commercial temperature range.

PINOUT

TOP VIEW



SIMPLIFIED SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between +V and GND	25V	$\overline{\text{RESET}}$ Input Voltage	7V
Voltage Between ± IN and GND	40V	Power Dissipation	600mW
Differential Input Voltage	±12V	Operating Temperature Range	
		HA1-23551-2	$-55°C \leq T_A \leq +125°C$
Output Off Voltage	40V	HA1-23551-4	$-25°C \leq T_A \leq +85°C$
		HA1-23551-5	$0°C \leq T_A \leq +75°C$
Peak Output ON Current	1A	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS +V = +5V, GND = 0V

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Threshold Voltage (Note 2)	Full	345	360	375	mV
Input Threshold Voltage Drift	Full		±20		µV/°C
+IN Bias Current (Note 3)	Full		675	1000	µA
+IN Bias Current Drift	Full		30		nA/°C
−IN Bias Current (Unlatched, Note 3)	Full		120	250	µA
(Latched, Note 4)	Full		370	500	µA
−IN Bias Current Drift	Full		10		nA/°C
Common Mode Voltage Range	Full	3.5		40	V
Common Mode Input Impedance	Full		350		KΩ
DIGITAL INPUT CHARACTERISTICS					
High Level $\overline{\text{RESET}}$ Voltage	Full	2			V
High Level $\overline{\text{RESET}}$ Current (Note 5)	Full		1	20	µA
Low Level $\overline{\text{RESET}}$ Voltage	Full			0.8	V
Low Level $\overline{\text{RESET}}$ Current (Note 6)	Full			−10	µA
OUTPUT CHARACTERISTICS					
Output On Voltage (Note 7)	Full		0.2	0.5	V
Output Off Leakage (Note 8)	Full		0.01	1	µA
Output On Impedance	Full		0.15		Ω
SWITCHING CHARACTERISTICS					
$\overline{\text{RESET}}$ Minimum Pulse Width (Note 9)	25°C	300			ns
$\overline{\text{RESET}}$ To Output Delay, t_{off} (Note 10)	25°C		150	1000	ns
Input Threshold to Output Delay, t_{on} (Note 11)	25°C		190	1000	ns
Input Minimum Pulse Width	25°C	300			ns
SUPPLY CHARACTERISTICS					
Supply Current (Note 12)	Full		1.6	2.5	mA

Notes:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $3.5V \leq \pm IN \leq 40V$
3. $+IN = -IN = 40V$, $\overline{\text{RESET}} = 0.8V$
4. $+IN = -IN = 40V$, $\overline{\text{RESET}} = 2.4V$
5. $+V = 5.5V$, $\overline{\text{RESET}} = 2.4V$
6. $+V = 5.5V$, $\overline{\text{RESET}} = 0.4V$
7. $I_{sink} = -10mA$, $+IN = -IN$, $\overline{\text{RESET}} \geq 2V$
8. $V_{out} = 40V$
9. See Test Circuit and Switching Waveforms
10. $V_{ID} = 0$, See Test Circuit and Switching Waveforms
11. $V_{IR} = 0$, See Test Circuit and Switching Waveforms
12. $+V = 5.5V$, All Latches in non-latched State

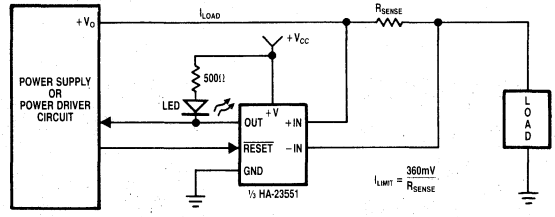
APPLICATIONS

The HA-23551 is ideally suited for applications which require accurate sensing of power supply or power driver circuit currents. Figure 1 shows a typical application where the HA-23551 senses the current delivered to a load. A unique design feature of the comparator input stage allows proper operation with common mode voltages well above the supply voltage of the HA-23551. For example, in Figure 1 $+Vo$ may vary from 3.5 to 40V while $+V_{cc}$ remains at $+5V$. The desired current limit is determined by the value of R_{sense} and the stable 360mV (typ.) threshold voltage of the HA-23551. When the voltage drop across R_{sense} exceeds the threshold voltage, the output goes low and internal positive feedback causes the output to latch in the low state (see simplified schematic). The output will remain in the low state until the voltage drop across R_{sense} drops below the threshold voltage and a RESET signal at least 300ns wide is received. The open collector outputs of the HA-23551 are capable of sinking 25mA continuously and may be used to directly drive indicator lamps, LEDs or SCR crowbar circuits.

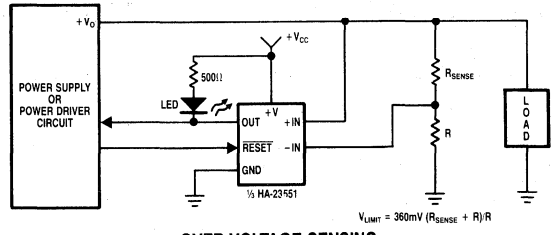
The HA-23551 may also be used to detect over-voltage conditions as shown in Figure 2. In this case the output will latch low when $+V_o \cdot R_{sense} / (R_{sense} + R)$ 360 mV.

The input bias currents of the HA-23551 are quite constant over temperature and common mode voltage variations and can be used to bias a thermistor for temperature sensing circuits as shown in Figure 3. When the voltage across the resistor, thermistor combination exceeds the threshold voltage an over-temperature signal is returned to the power supply.

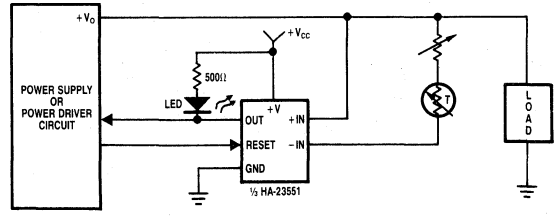
Since the HA-23551 contains three current sense latches, all three functions below could be incorporated using only one 14-pin dip. Other applications for the HA-23551 include current sensing and control of stepper motor drivers, laser diode drivers, solenoid actuators, switching power supplies or any circuit which requires fast, accurate sensing and control of supply currents.



OVER-CURRENT SENSING
FIGURE 1

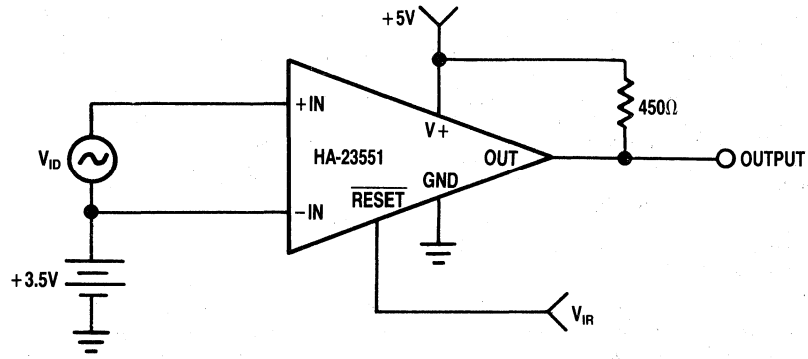


OVER-VOLTAGE SENSING
FIGURE 2



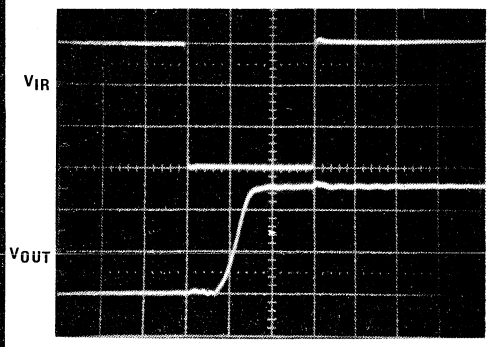
OVER-TEMPERATURE SENSING
FIGURE 3

RESPONSE TIME TEST CIRCUIT



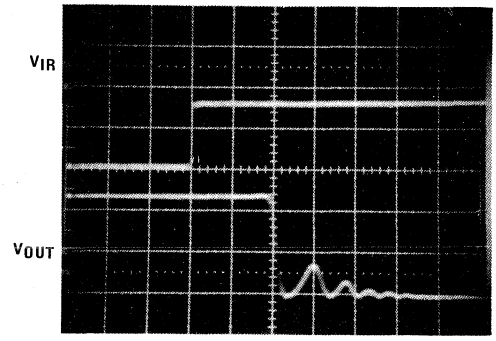
SWITCHING WAVEFORMS

V_{IR} = 1V/DIV
V_{OUT} = 2V/DIV
Time = 100 ns/DIV



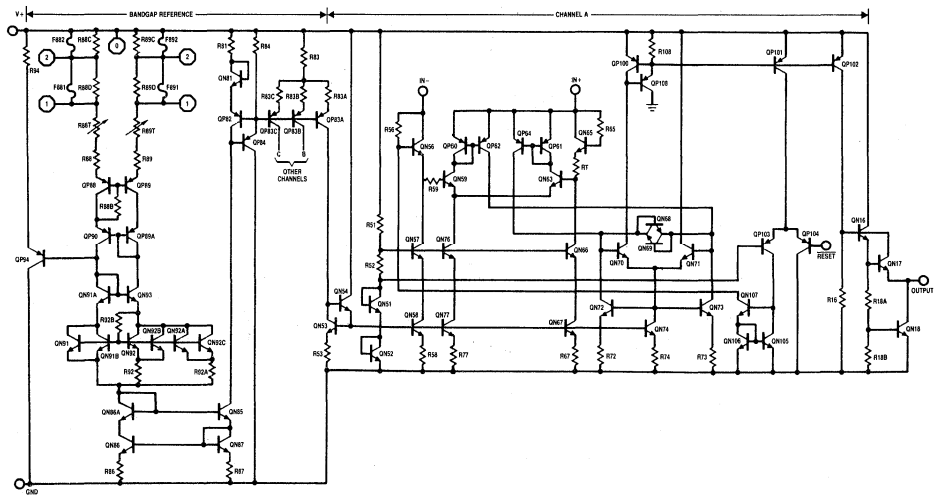
V_{ID} = OV, +IN = −IN = 3.5V

V_{ID} = 200 mV/DIV
V_{OUT} = 2V/DIV
Time = 50 ns/DIV



V_{IR} = 0

FULL SCHEMATIC



HARRIS

HV-1000/1000A

Induction Motor Energy Saver

FEATURES

- OPERATES DIRECTLY OFF 120V/240V AC LINE – NO POWER SUPPLY REQUIRED
- 50Hz OR 60Hz OPERATION
- PRODUCES POWER SAVINGS FROM 10% TO 50% FOR MOTORS WITH LIGHT OR VARIABLE LOADS
- SCR OUTPUT STAGE TRIGGERS TRIAC DIRECTLY
- LOAD ANTICIPATOR SENSES SHOCK LOADS AND RESPONDS INSTANTLY WITH FULL POWER
- WITHSTANDS LINE SURGES TO 3500V
- CAUSES MOTOR TO RUN QUIETER, COOLER
- CAN BE MOUNTED INSIDE MOTOR
- NEEDS ONLY 3 RESISTORS, 3 CAPACITORS AND A TRIAC TO ASSEMBLE COMPLETE CONTROLLER

DESCRIPTION

The HV-1000 and HV-1000A are energy saving, induction motor, control circuits designed to reduce the power consumed by single phase induction motors. HV-1000 is for 120V AC use and HV-1000A for 240V AC use.

The controller circuit senses the load on the motor and then controls a TRIAC to apply reduced voltage to lightly loaded motors, full voltage to heavily loaded motors.

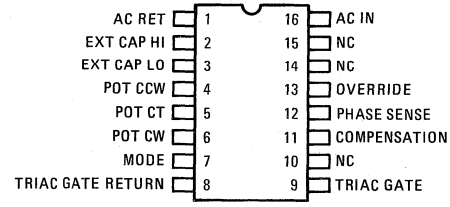
The HV-1000/1000A are available in a 16 lead plastic DIP. Ideal for mounting inside induction motors, they can also be mounted in a heat sunk circuit box for external, after market application.

APPLICATIONS

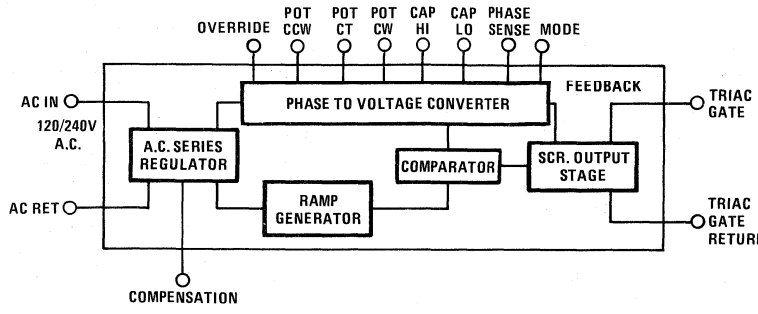
- MACHINE TOOLS
- INDUSTRIAL SEWING MACHINES
- HEAT PUMPS
- PRESSES
- CONVEYORS
- DISC PACK DRIVES
  - ► ANY APPLICATION WHERE FOR SOME OF THE TIME THE MOTOR IS DRIVING LESS THAN ITS RATED LOAD

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Input Voltage (With 5k Input Resistor)	$350V_{PEAK}$	Storage Temperature	-40°C to +100°C
Input Voltage (Without Input Resistor)	$\pm 400V_{PEAK}$	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	500mW	Output Current (10 microsecond Pulse)	500mA
Operating Temperature Range	0°C to +75°C		

ELECTRICAL CHARACTERISTICS See Note (a)

HV-1000/1000A using its internal power factor settings (pins 4, 5, 6, 7 shorted together). See Figure 1 for definition of θc, the current zero crossing, and θt, the TRIAC trigger point. Frequency = both 50Hz and 60Hz unless otherwise stated.

PARAMETER	DEFINITION	MIN	TYP	MAX	UNITS
Skew (b)	Difference Between Positive and Negative θt for $\theta c = 32^o$	0	± 6.5		Degrees
Load Anticipator Trip Point (60Hz Operation)	Value of θc at which Load Anticipator Trips at 60Hz	16	23		Degrees
Load Anticipator (c) Trip Point (50Hz Operation)	Value of θc at which Load Anticipator Trips at 50Hz	13	19		Degrees
Full Load Power Factor Setting	Value of θc at which $\theta c = \theta t$	39	43	47	Degrees
Full Load Power Factor (d)	Power Factor when $\theta c = \theta t$	.68	.73	.77	Power Factor
No Load Power Factor Setting	Value of θc when $\theta t = 146^o$		32		Degrees
Maximum Input Voltage	Breakover Voltage of Input Protection SCRs	400	500		V_{PEAK}
Current Drain	RMS Input Current to chip (Pin 16)			2.0	mA RMS
Maximum Output Voltage	Breakover Voltage of Output Stage with Input to Chip Biased Normally with AC Power	600	800		V_{PEAK}

NOTES:

(a) No guarantee of power savings can be given since the savings achieved depend entirely on the motor and its application. However, for a completely unloaded motor driving only a flywheel or a pulley, power savings of 50% are typical. It is not uncommon to observe savings of as much as 80%. In all applications the percentage of power saved will depend on how much of the time the motor runs lightly loaded. Harris Application Note 542 covers the subject of selecting suitable applications.

(b) The presence of skew results in partial rectification of the AC power through the motor and reduced power savings. The skew numbers shown here may decrease the power savings of an unloaded motor as indicated on a rotating wheel type, electric, utility power meter by approximately 10% maximum.

The skew is greatest at no load ($\theta c = 32^o$) and decreases linearly to zero as the motor approaches full load.

(c) The effect of a shock load is to shift θc (the current zero crossing) temporarily closer to the voltage zero crossing. If the shock is severe enough to perturb θc all the way back to the load anticipator trip point, the HV-1000 will discontinuously switch (trip) to full power. The anticipator trip point is increased by the absolute value of an external potentiometer, 10k ohms increasing it about 6 degrees. A circuit utilizing an external potentiometer is shown in Figure 6.

(d) This full load power factor is typical of a wide variety of U.S., single phase, 60Hz, capacitor start induction motors of power levels between ¼ HP and 1 HP. Many other motors, both larger and smaller and operating at 50Hz, can also be driven satisfactorily by this power factor setting. However, there are some motors for which this full load power factor setting is not satisfactory, being either too high or too low. To suit these motors, a potentiometer must be added as shown in Figure 6. The potentiometer should then be adjusted so that full voltage is applied to the motor ($\theta c = \theta t$) when the motor is fully loaded. An oscilloscope and a dynamometer are required to do this set-up precisely, although other loading means can be substituted for a dynamometer, if none is available. The absolute value of the potentiometer determines the range of adjustment, a 5k potentiometer giving a much larger range of adjustment than a 1k potentiometer.

Induction motors run at a speed which depends primarily on the supply frequency, little on voltage. They draw almost a constant current regardless of the load – the motor responds to load with a change in power factor. Thus, a lightly loaded motor wastes energy by heating its windings with inductive current. The HV-1000/1000A measures the load using the current phase angle and then saves power by applying to the motor only sufficient voltage to drive the load.(1) The voltage is adjusted by TRIAC phase control.

The controller chip triggers a TRIAC which is in series with the motor. This varies the RMS voltage across the motor. The resulting voltage waveform across the motor is shown at the top of Figure 1. A motor can be characterized by the relation between the two parameters θc and θt, shown in Figure 1 for a typical motor. At point A, the motor is running fully loaded with full voltage applied, as it was designed. At point B, the motor is running lightly loaded with voltage reduced to the point of stalling. The function of the controller is to force the motor to operate along the load line AB, rather than AC which it does naturally. Figure 2 shows an example of the typical power savings which results when the controller chip is incorporated in a motor.

The key features of the circuit are firstly that all analog processing is carried out with the circuitry running entirely on 50Hz – 60Hz alternating current. Direct current is not used at all. Secondly it is integrated using dielectric isolation, with junction breakdowns of 400V. Junctions are stacked in both the input regulator and the SCR output stage so that the composite breakdown voltage of these stages is ±800V.

The analog processing which achieves the control function is explained conceptually in Figure 3. At any given load condition, the controller tries to force the motor current phase θc to a pre-programmed set phase. The phase to voltage converter measures the difference between the set phase and θc, and increments a pedestal voltage at a rate proportional to the difference, delaying the trigger point θt, where a reference ramp intersects the pedestal. The delayed triggering reduces the voltage applied to the motor, decreasing the motor winding current so that θc is forced to the set phase by the modulation of θt. The set phase is itself a slow function of θt, which produces the sloping controller characteristic fo Figure 1. This is achieved via the feedback path from the output stage to the phase to voltage converter.

An additional feature of the phase to voltage converter is the load anticipator. If θc is typically more than 0.42ms less than the set phase for 60Hz operation, which means the motor has received a sudden heavy load, the full line voltage is immediately applied to the motor. This allows the motor to respond at once to a step function load. If the load is abruptly removed, the controller cuts back the voltage applied to the motor over a time period set by the external time constant capacitor. This mechanism is described in more detail in Harris Application Note 542.

(1) This circuit principle was first described by F. J. Nola in U.S. Pat. 4052648.

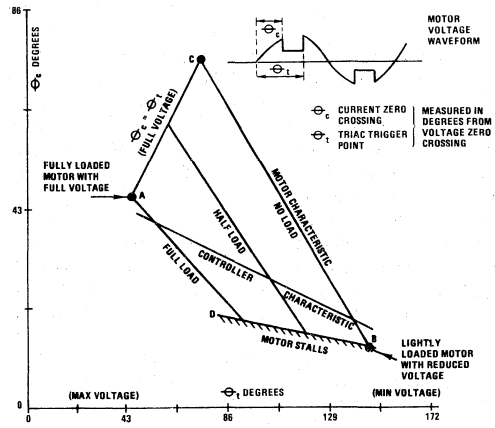


FIGURE 1
Voltage Waveform Characteristics of a TRIAC Controlled Induction Motor

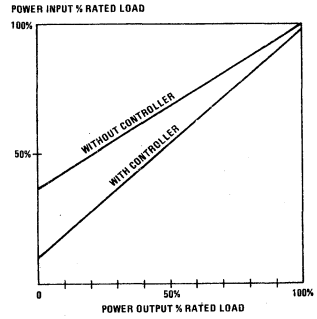


FIGURE 2
Power Savings as a Function of Load for a 1/3 HP Motor

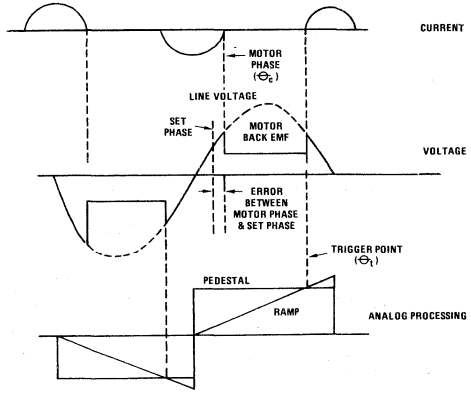


FIGURE 3
Relation of the Voltage and Current Waveforms to the Analog Processing Function

APPLICATIONS INFORMATION

Improvement of the efficiency of single phase induction motors may be achieved in two ways. For motors which drive a steady load equal to their rated capacity, the best method is to use a run capacitor with an auxiliary winding. This causes the internal field structure of the motor to resemble that of a three phase motor, an inherently more efficient arrangement. However, if a capacitor run motor is used to drive less than its rated load, its power consumption will usually be greater than a motor without a run capacitor. If this is the case for a significant fraction of the time, a run capacitor is not effective for improving efficiency. By contrast an electronic energy saving motor controller produces significant improvements in efficiency for lightly loaded motors, and is therefore, the best choice for motors which spend a significant part of their time lightly loaded. Electronic energy saving controllers are useful for machine tools, industrial sewing machines, heat pumps, presses, conveyors, disc pack drives, and commercial washing machines; in other words for any application where the load on the motor is either variable or ill defined. Run capacitors are useful for refrigerators, air conditioners, and ventilation fans – all applications where the load on the motor is steady and well defined. An electronic energy saving controller should not be applied in a circumstance where a motor is driving a constant, steady load equal to its rated load. In this circumstance the power dissipated in the TRIACs may actually increase the total power usage. However, it sometimes happens that induction motors are relatively conservatively designed, and the real power capability of the motor is greater than that stated. This may come about, for instance, because the motor may have been designed to operate with worst case low line voltage, say, 100V for a nominal 115V motor. In such a circumstance, an electronic energy saving controller can produce useful savings, because in reality, the conservative design of the motor is causing it to be operating at less than its full capability. This circumstance can be tested experimentally by connecting a power meter to the motor and then adjusting the set power factor with a potentiometer on the controller circuit to test whether reduced power consumption can be obtained. Once set up in this way, the controller will continue to give the motor just sufficient voltage to drive the load in hand, even if the line voltage drifts high. In other words, the energy saving controller also acts as a line voltage regulator. This is especially beneficial in areas where the line voltage fluctuates, since high line voltage can cause an induction motor to consume excessive amounts of power. For more information see Harris Application Note 542 "Using the HV-1000 Induction Motor Energy Saver".

APPLICATION CIRCUITS

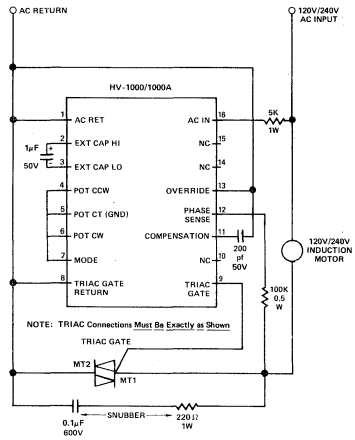


FIGURE 4
Basic Application Circuit for the HV-1000

Basic Circuit

Figure 4 shows the basic application circuit for HV-1000. This circuit would be suitable for a 1/2 HP motor. For smaller or larger motors, the time constant capacitor (between pins 2 and 3) and snubber capacitor should be scaled in proportion to the size of the motor.

Operation with a Motor Switch

We recommend that the HV-1000 circuit should be permanently wired to the motor so that HV-1000 and motor are switched together. However, if this is not possible and a switch has to be placed in series with the motor between the motor and HV-1000, the circuit of Figure 5 should be used. The 0.01 μF (600V) capacitor keeps the phase sense property of HV-1000 alive while the switch is open, ensuring a smooth start-up when the switch is closed.

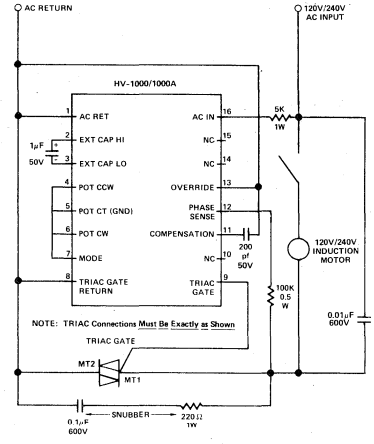


FIGURE 5
Application Circuit with Switch on Motor

To Adjust the Phase Setting

When it is required to adjust the full load, power factor setting, a potentiometer should be added as shown in Figure 6. The larger the absolute value of the potentiometer, the greater the range of adjustment. 1k ohms is recommended as a starting

point if potentiometer adjustment is required. Adding the potentiometer also increases sensitivity of the load anticipator, a 10k potentiometer advances the anticipator trip point by 6 degrees. In general the smallest absolute value of potentiometer that covers the desired range of adjustment should be used. 10k ohms is the maximum potentiometer value normally needed.

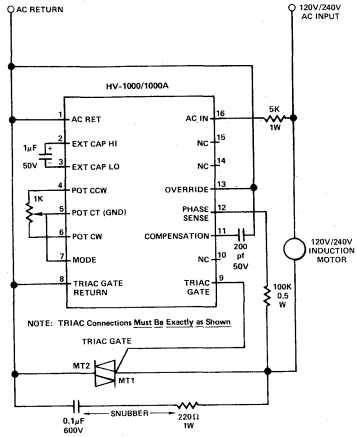


FIGURE 6
Application Circuit for HV-1000/1000A with Potentiometer to get Increased Anticipator Sensitivity and Adjustable Phase Setting

Electronic Override

Pin 13 is a TTL logic input which commands full output power. It can be activated with a switch as shown in Figure 7. The diode between pins 13 and 1 needs 5V capability, it is to prevent negative potentials being applied to pin 13.

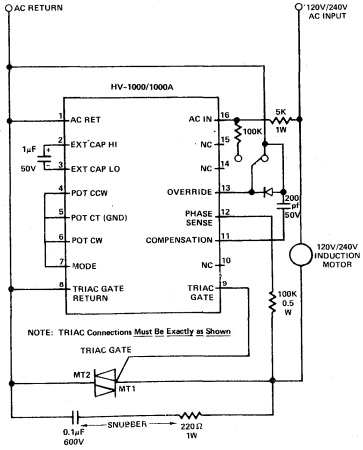


FIGURE 7
Application Circuit for HV-1000/1000A Illustrating Electronic Override

NOTES:

(a) Stability: A small number of motors, primarily amongst the larger (above 1 HP) single phase motors may not necessarily run in a stable fashion with the application circuit of Figure 4. The symptoms are irregular vibration and repeated jerky application of full power to the motor. An oscilloscope placed in differential mode across pins 2 and 3 will show rapid fluctuations in voltage instead of the steady voltage levels characteristic of control equilibrium. This and similar effects are described in Harris Application Note 542. The problem is helped by increasing the inertia on the shaft (e.g., adding a flywheel), by increasing the time constant capacitor and sometimes by adding a potentiometer and adjusting it for smaller power savings. If all these measures fail it may be that a special application circuit will be needed as described in Application Note 542. The effect is dependent on which company manufactured the motor.

(b) Selection of components: The TRIAC used should have a current rating which allows the locked motor current of the motor (often three or more times the run current) to be conducted for as long as this may persist. Normally heat sinking will be required to conduct away the heat of the TRIAC. The 5k input resistor only performs a useful purpose during voltage surges in excess of 600V. When this happens, internal crowbar clamps on chip between pins 1 and 16 break over and momentarily conduct about an ampere, causing thousands of volts to be dropped across the 5k resistor. For this reason the physically large size of a 1W resistor is needed, otherwise the terminals of the resistor would arc over. The time constant capacitor between pins 2 and 3 is normally chosen to be the smallest value that will allow the motor to run in a stable fashion. If it is chosen too large, the HV-1000 will not throttle back the voltage as quickly, if the load suddenly decreases. This effect reduces the power savings.

LF 147/347 Wide Bandwidth Quad JFET Input Operational Amplifier

General Description

The Harris LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage. The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LM348 and LM324 designs.

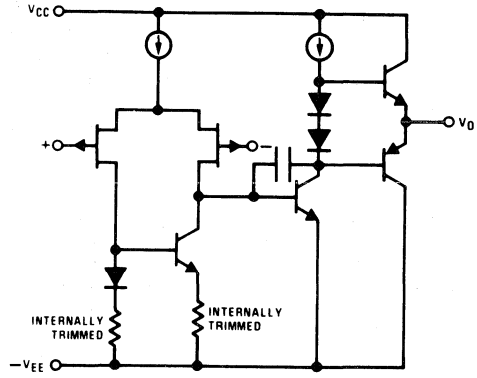
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

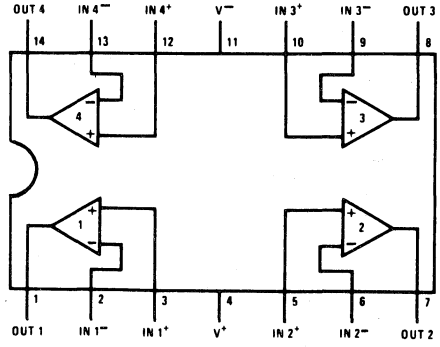
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



Order Number LF347N, or LF347BN

Order Number LF147J, LF347J

TOP VIEW

Absolute Maximum Ratings

	LF147	LF347B/ LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	LF147	LF347B/ LF347
Power Dissipation (Note 3)	900mW	500mW
Tj max	150°C	115°C
θjA	100°C/W	150°C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF147			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 5,6)		25	100		25	100		25	100	pA
		Over Temp.			25			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 5,6)		50	200		50	200		50	200	pA
		Over Temp.			50			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF147			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 125°C/W junction to ambient or 95°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: P_D max rating cannot be exceeded.

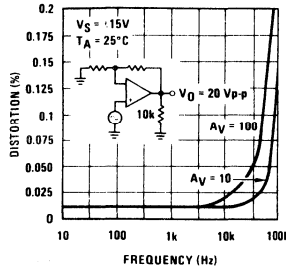
Note 4: These specifications apply for V_S = ±15V and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

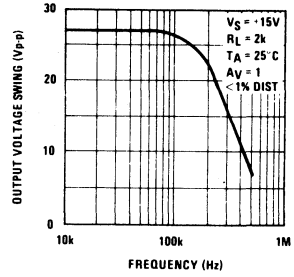
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics (Continued)

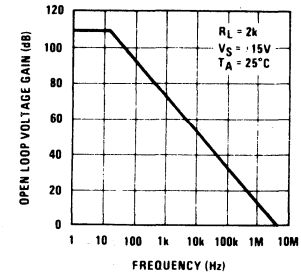
Distortion vs Frequency



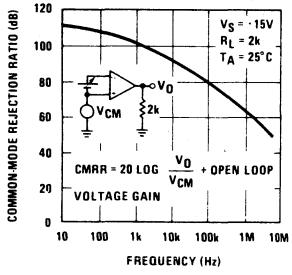
Undistorted Output Voltage Swing



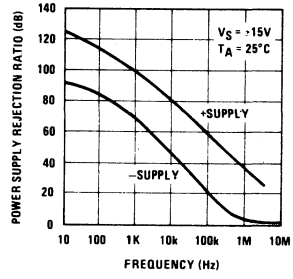
Open Loop Frequency Response



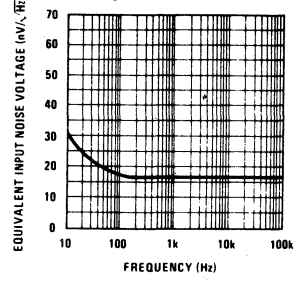
Common-Mode Rejection Ratio



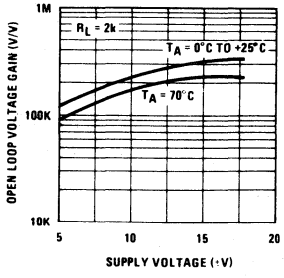
Power Supply Rejection Ratio



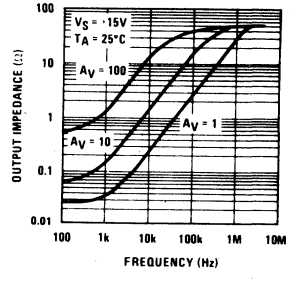
Equivalent Input Noise Voltage



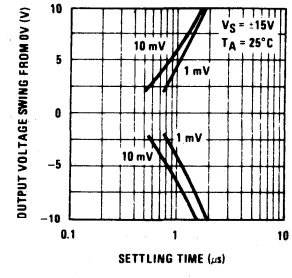
Open Loop Voltage Gain (V/V)



Output Impedance

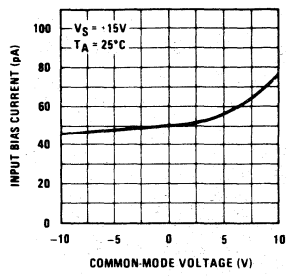


Inverter Settling Time

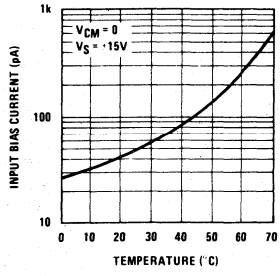


Typical Performance Characteristics

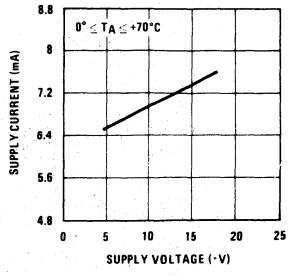
Input Bias Current



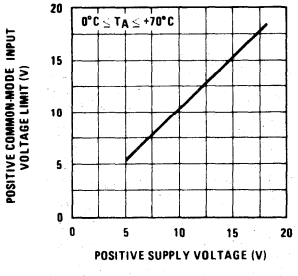
Input Bias Current



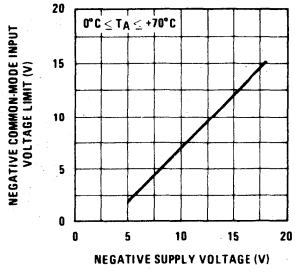
Supply Current



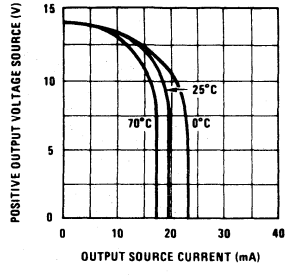
Positive Common-Mode Input Voltage Limit



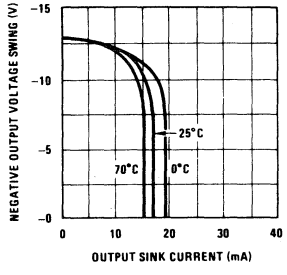
Negative Common-Mode Input Voltage Limit



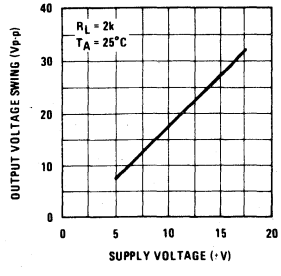
Positive Current Limit



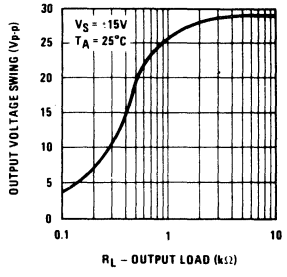
Negative Current Limit



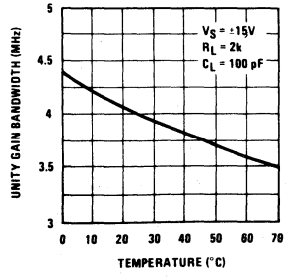
Voltage Swing



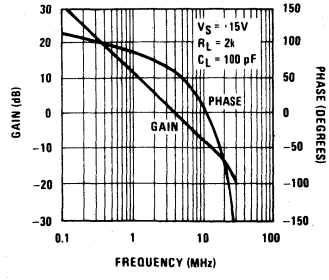
Output Voltage Swing



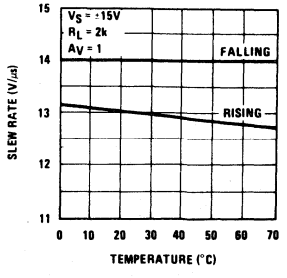
Gain Bandwidth



Bode Plot

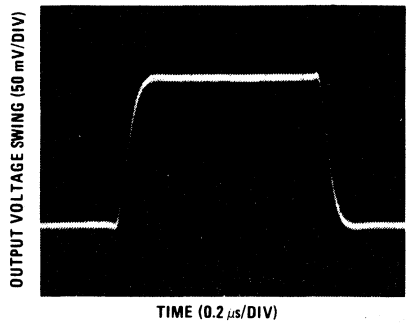


Slew Rate

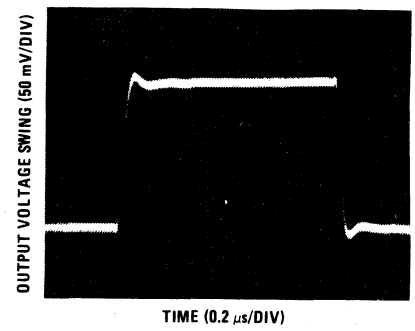


Pulse Response

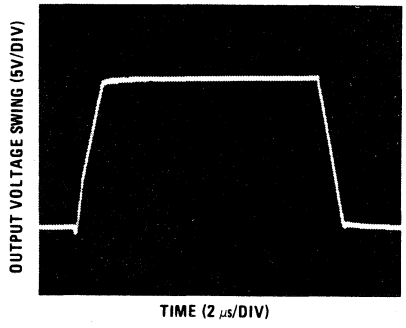
Small Signal Inverting



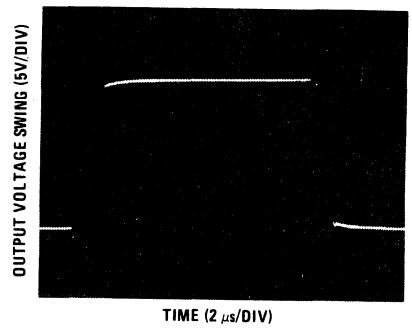
Small Signal Non-Inverting



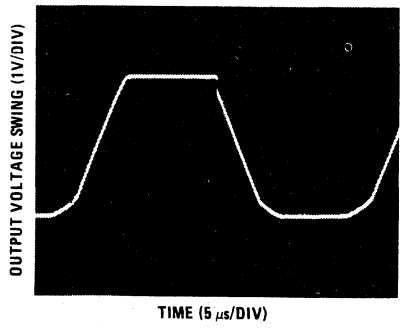
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2k Ω load resistance to ±10V over the full temperature range if the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

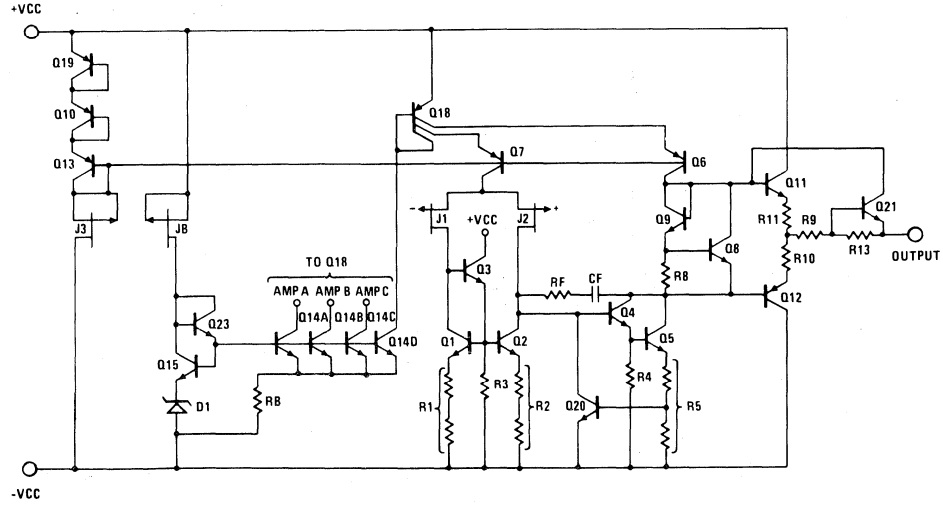
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

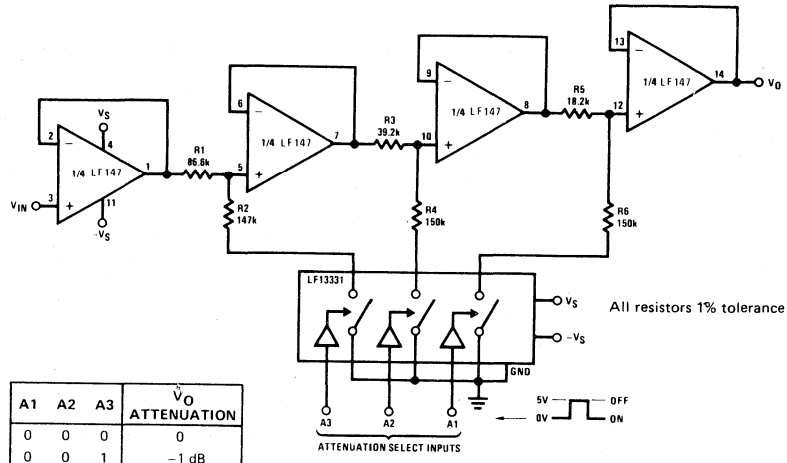
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

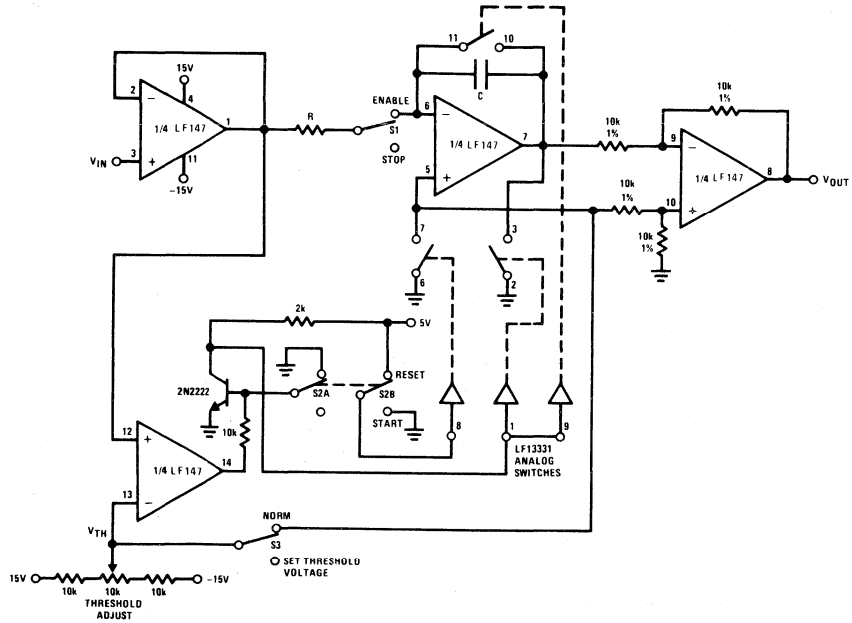
Digitally Selectable Precision Attenuator



A1	A2	A3	$\frac{V_O}{}$ ATTENUATION
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



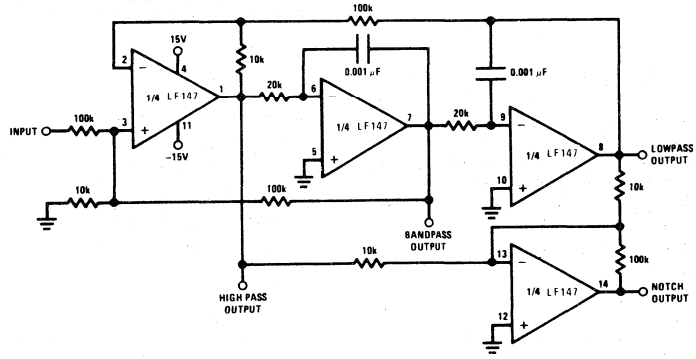
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



For circuit shown:
f_o = 3 kHz, f_{NOTCH} = 9.5 kHz
Q = 3.4
Passband gain:
Highpass — 0.1
Bandpass — 1
Lowpass — 1
Notch — 10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM348 data sheet for design equations

HARRIS

Operational Amplifiers/Buffers
LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

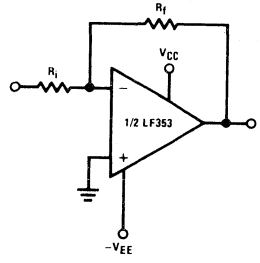
These devices are low cost, high speed, dual JFET input operational amplifiers. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

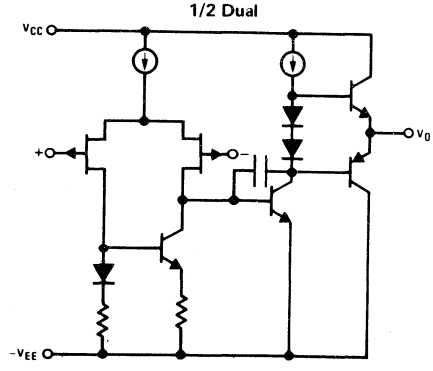
Features

- Typical offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 3.6 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to .1% — 2 μs

Typical Connection



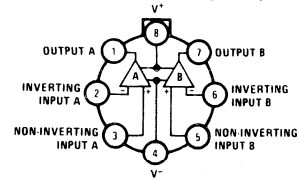
Simplified Schematic



Connection Diagrams

Section 11 for Packaging

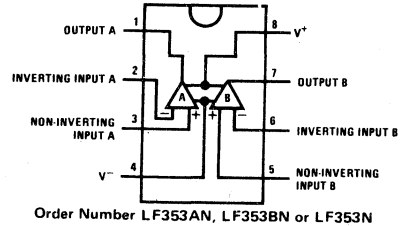
LF353H Metal Can Package (Top View)



Order Number LF353AH or LF353BH

Section 11 for Packaging

LF353N Dual-In-Line Package (Top View)



Order Number LF353AN, LF353BN or LF353N

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10	20		10	30		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	100		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50			50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 10kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			3.6	5.6		3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	10	13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C	3	4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 160°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

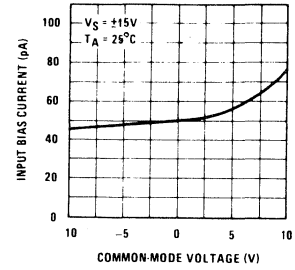
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

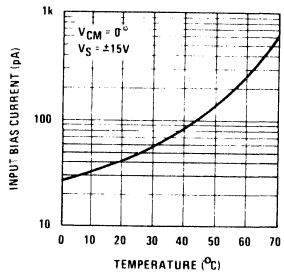
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

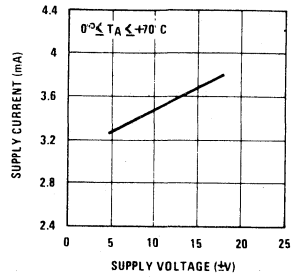
Input Bias Current



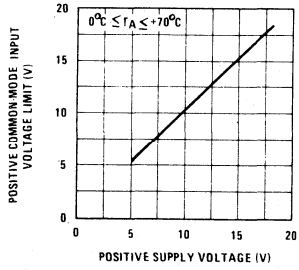
Input Bias Current



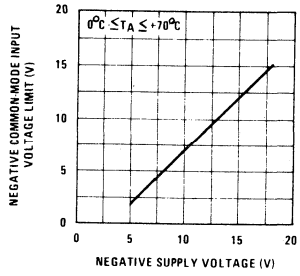
Supply Current



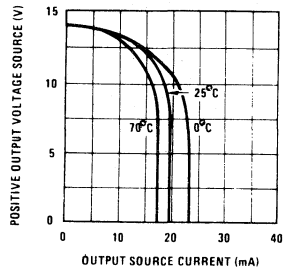
Positive Common-Mode Input Voltage Limit



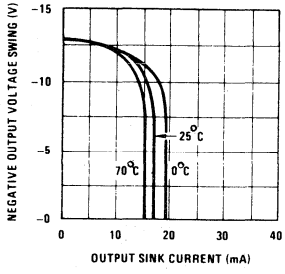
Negative Common-Mode Input Voltage Limit



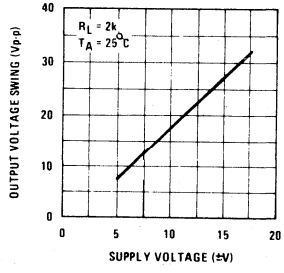
Positive Current Limit



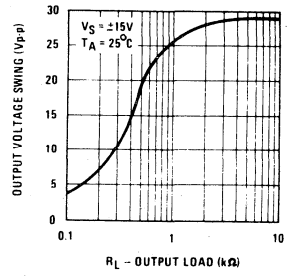
Negative Current Limit



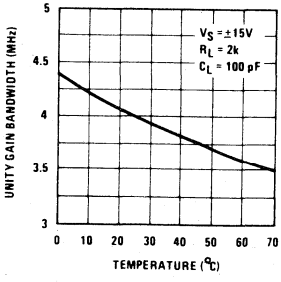
Voltage Swing



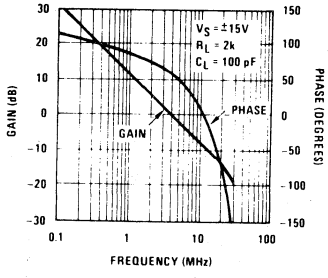
Output Voltage Swing



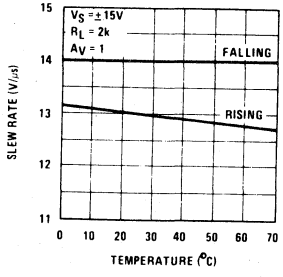
Gain Bandwidth



Bode Plot

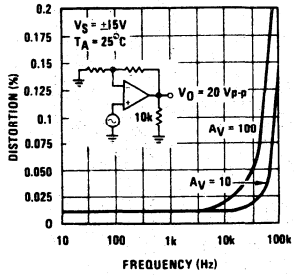


Slew Rate

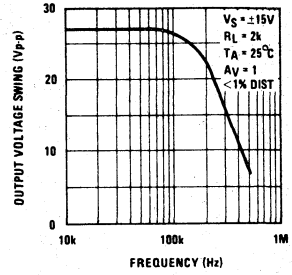


Typical Performance Characteristics (Continued)

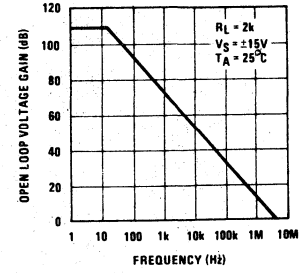
Distortion vs Frequency



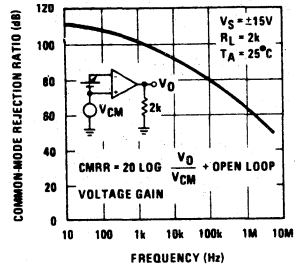
Undistorted Output Voltage Swing



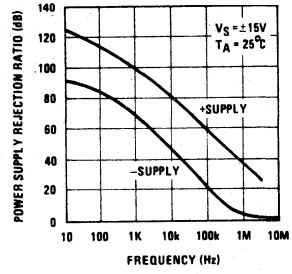
Open Loop Frequency Response



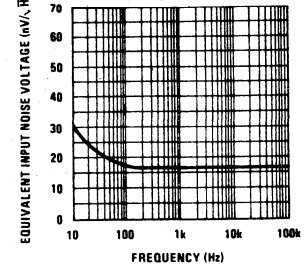
Common-Mode Rejection Ratio



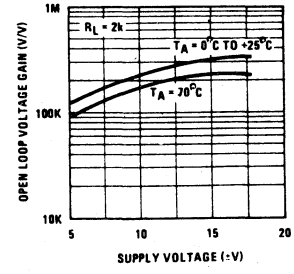
Power Supply Rejection Ratio



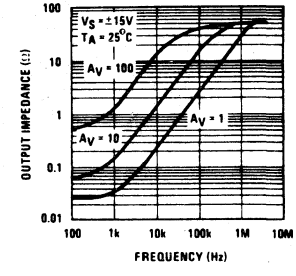
Equivalent Input Noise Voltage



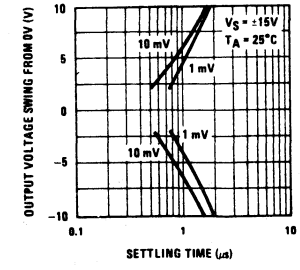
Open Loop Voltage Gain (V/V)



Output Impedance

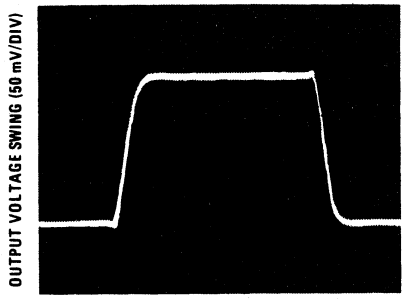


Inverter Settling Time

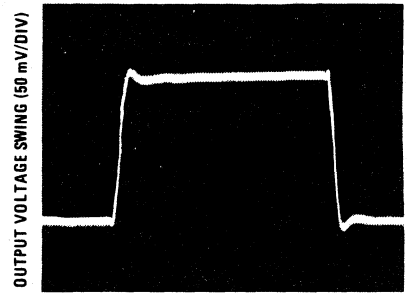


Pulse Response

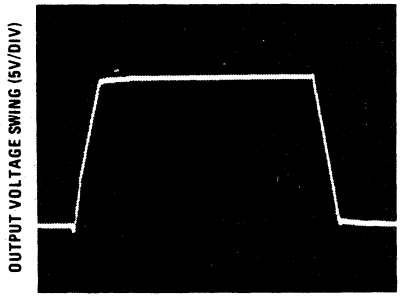
Small Signal Inverting



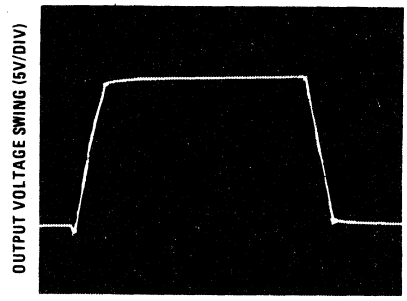
Small Signal Non-Inverting



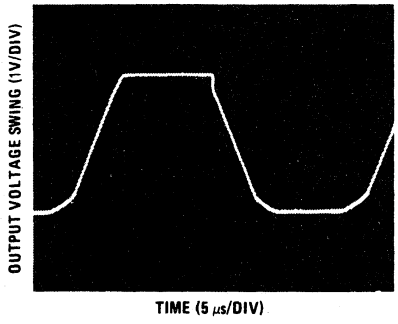
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

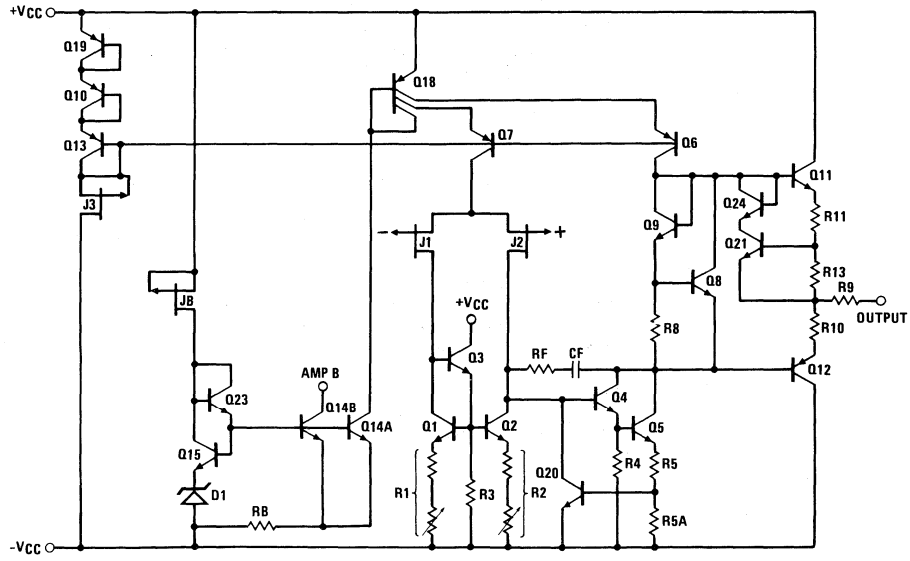
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

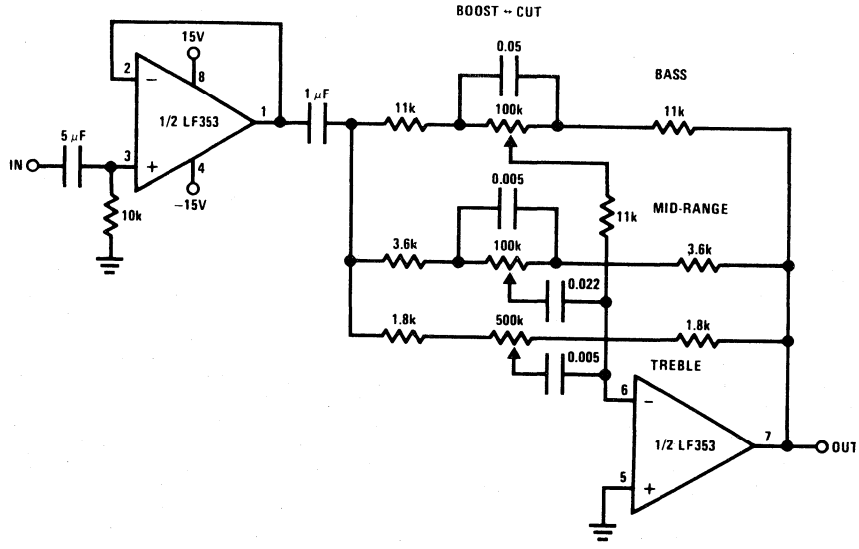
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

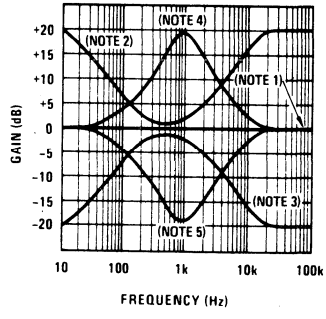
Detailed Schematic



Typical Applications

Three-Band Active Tone Control



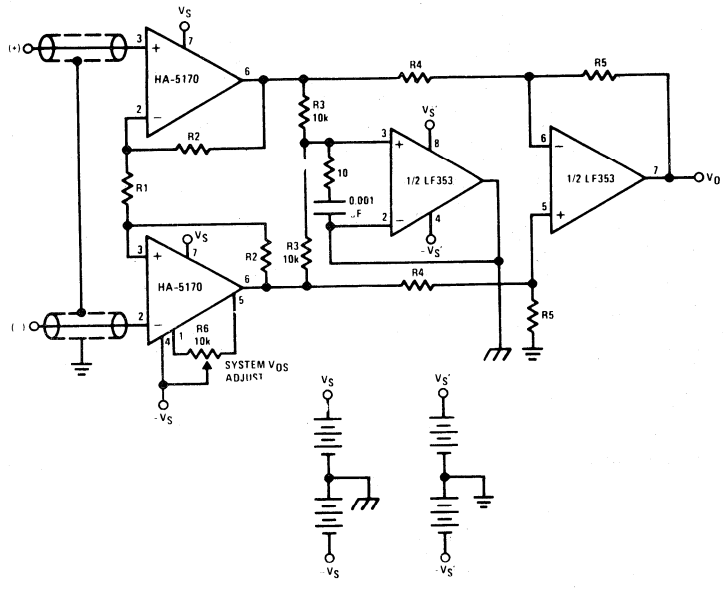


Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

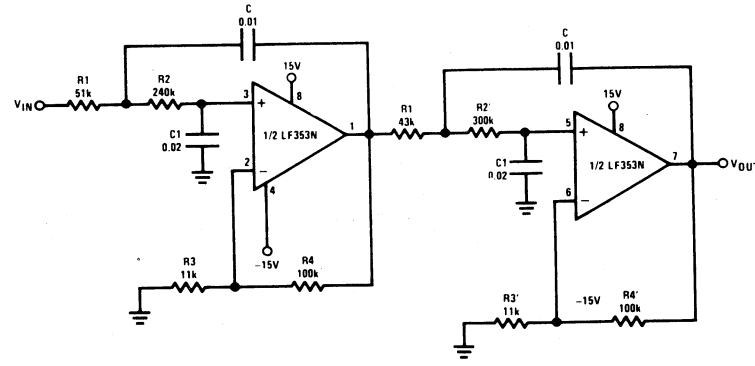
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

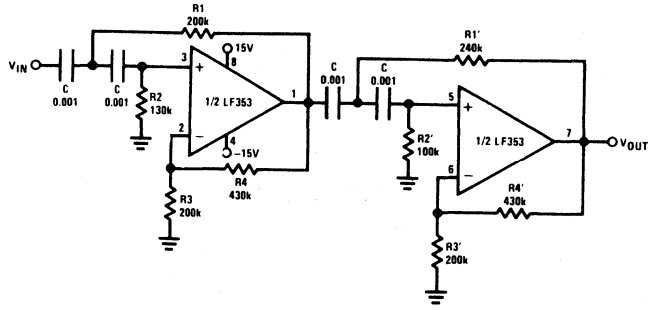
Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

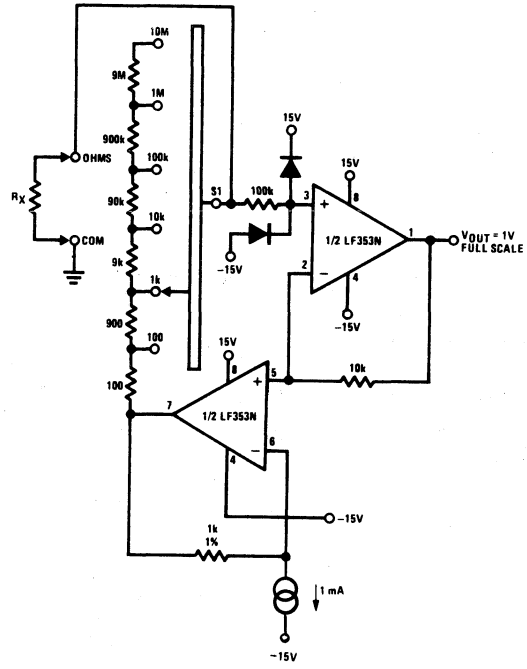
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency $(f_c) = \sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain $(H_O) = (1 + R4/R3)(1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

HARRIS

Operational Amplifiers/Buffers

LM118/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

Fabricated using the Harris process which, coupled with our unique design, affords a more predictable dynamic performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its applications since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. Overcompensation can be used with the amplifier for greater stablility when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 300ns if required.

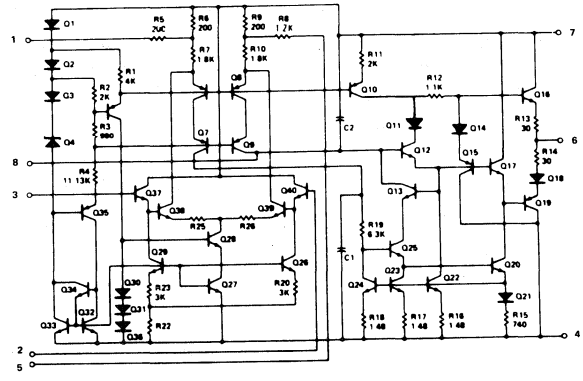
The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM318 is identical to the LM118 except that the LM318 has its performance specified over a 0°C to +70°C temperature range.

Features

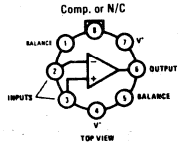
- 15MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Pin compatible with general purpose op amps

Schematic and Connection Diagrams



Section 11 for Packaging

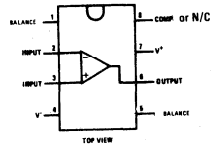
Metal Can Package*



*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H
or LM318H

Dual-In-Line Package



Order Number LM118J-8,
or LM318J-8

Order Number LM318N

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±15V
Output Short-Circuit Duration (Note 4)	Indefinite
Operating Temperature Range	
LM118	-55°C to +125°C
LM318	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 5)

PARAMETER	CONDITIONS	LM118			LM318			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	Unless Otherwise Specified: $V_S = \pm 15V$, $T_A = +25°C$		2	4		5	10	mV
Input Offset Current			6	50		30	200	nA
Input Bias Current			120	250		150	500	nA
Input Resistance		1	3		0.5	3		MΩ
Supply Current			5	8		5	10	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	12	15		10	15		V/mV
Slew Rate	$A_V = 1$	50	70		50	70		V/μs
Small Signal Bandwidth			15			15		MHz
Input Offset Voltage	Unless Otherwise Specified: $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM118), $0°C \leq T_A \leq +70°C$ (LM318)			6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = +125°C$		4.5	6		4.5	6	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	8			8			V/mV
Output Voltage Swing	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range								V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C and the LM318 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: If a differential input voltage in excess of the operating supply voltage is applied between the input, excessive current will flow unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

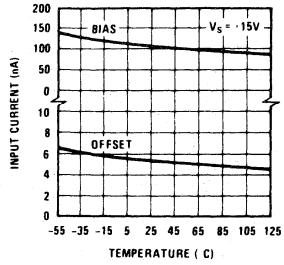
Note 4: LM118/LM318 can withstand continuous shorts to ground or either supply rail. However, good practice is to avoid exceeding the maximum junction temperature rating of the device, which could cause the circuit to be damaged.

Note 5: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, (LM118), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

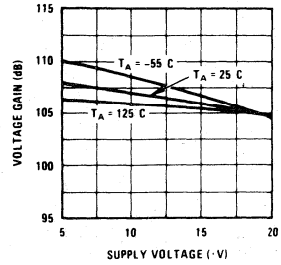
Note 6: In practically all applications the specified open loop voltage gain will be sufficient. In unusual applications requiring minimized loop gain errors, external adjustments may be necessary.

Typical Performance Characteristics LM118

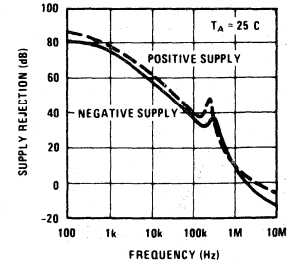
Input Current



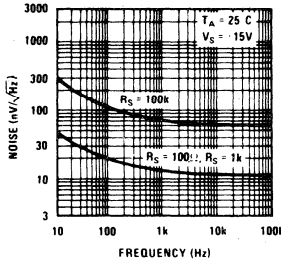
Voltage Gain



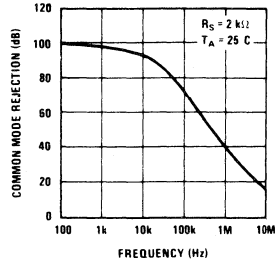
Power Supply Rejection



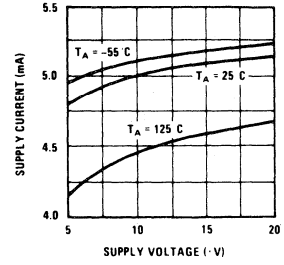
Input Noise Voltage



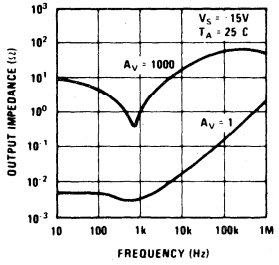
Common Mode Rejection



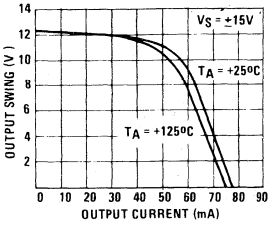
Supply Current



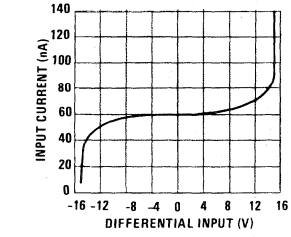
Closed Loop Output Impedance



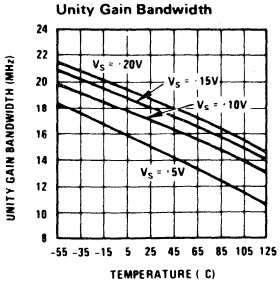
Output Current



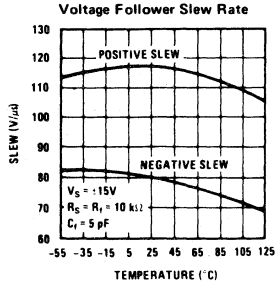
Input Current



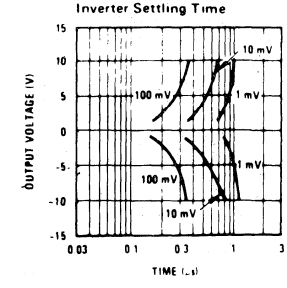
Unity Gain Bandwidth



Voltage Follower Slew Rate

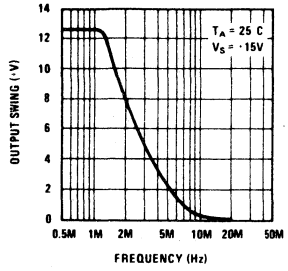


Inverter Settling Time

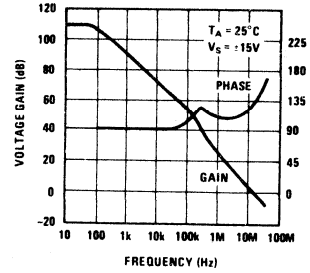


Typical Performance Characteristics LM118, (Continued)

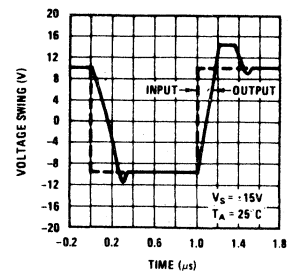
Large Signal Frequency Response



Open Loop Frequency Response

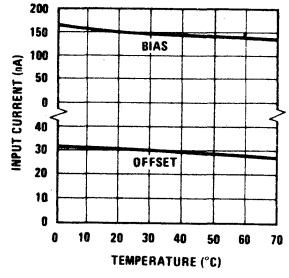


Voltage Follower Pulse Response

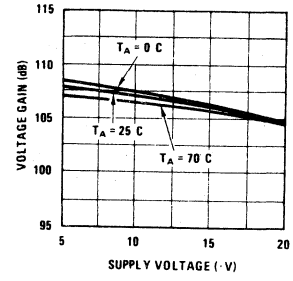


Typical Performance Characteristics LM318

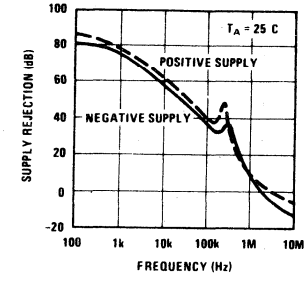
Input Current



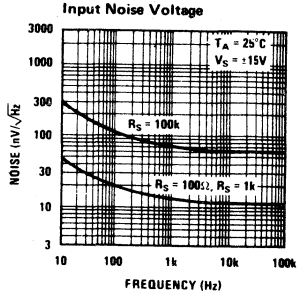
Voltage Gain



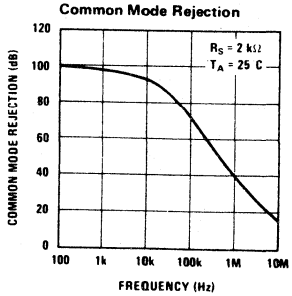
Power Supply Rejection



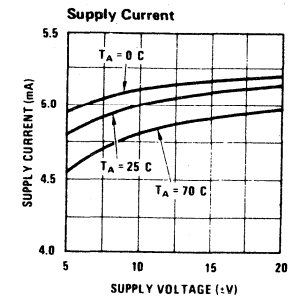
Input Noise Voltage



Common Mode Rejection

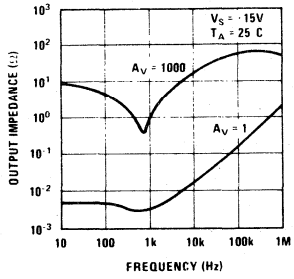


Supply Current

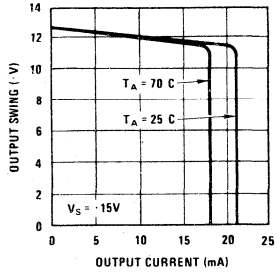


Typical Performance Characteristics LM318 (Continued)

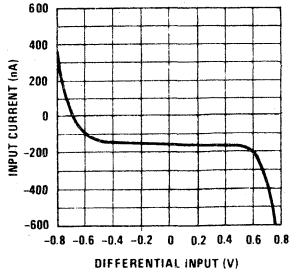
Closed Loop Output Impedance



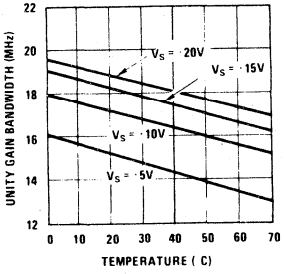
Current Limiting



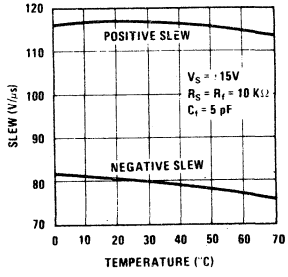
Input Current



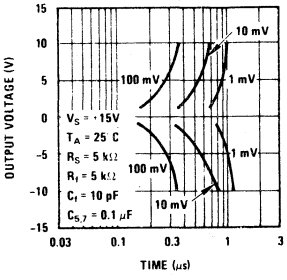
Unit Gain Bandwidth



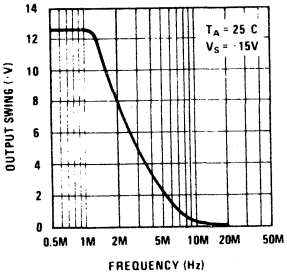
Voltage Follower Slew Rate



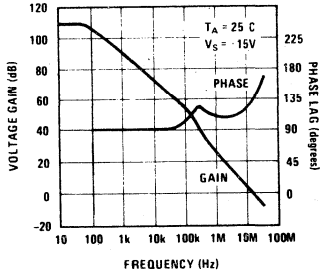
Inverter Settling Time



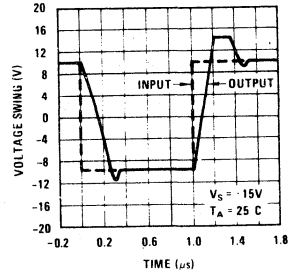
Large Signal Frequency Response



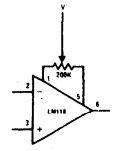
Open Loop Frequency Response



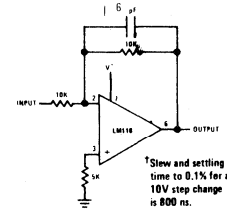
Voltage Follower Pulse Response



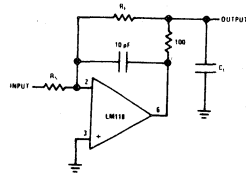
Auxiliary Circuits



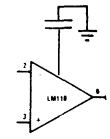
Offset Balancing



Compensation for Minimum Settling† Time

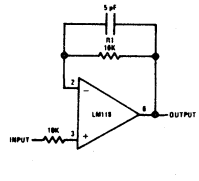


Isolating Large Capacitive Loads

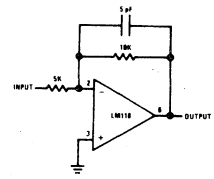


Overcompensation

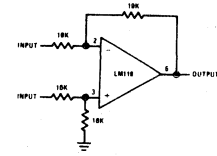
Typical Applications



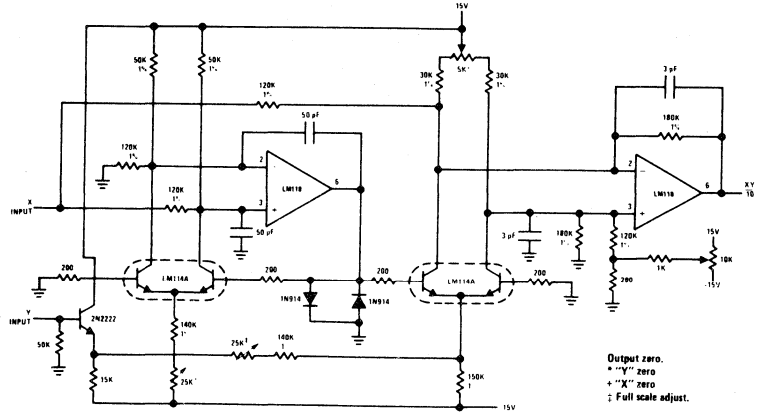
Fast Voltage Follower



Fast Summing Amplifier

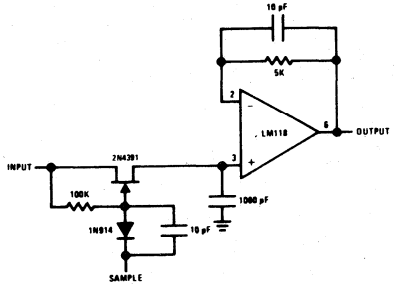


Differential Amplifier

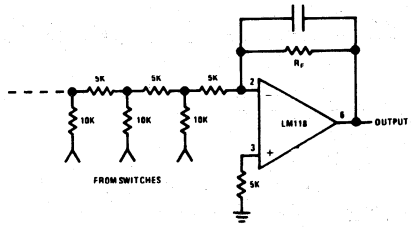


Four Quadrant Multiplier

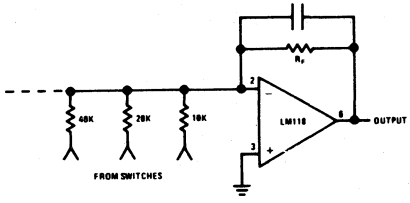
Typical Applications (Continued)



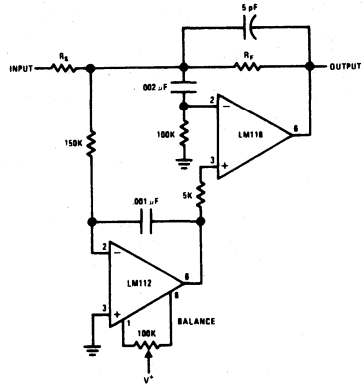
Fast Sample and Hold



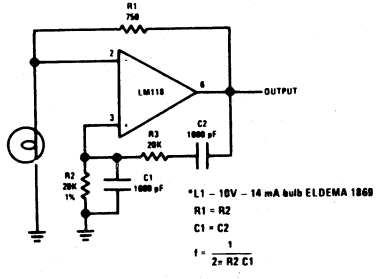
D/A Converter Using Ladder Network



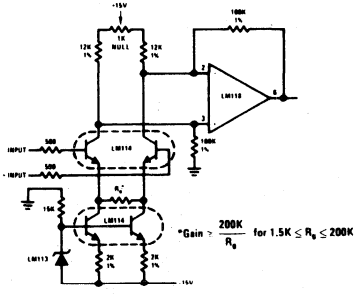
D/A Converter Using Binary Weighted Network



Fast Summing Amplifier with Low Input Current



Wein Bridge Sine Wave Oscillator



Instrumentation Amplifier

LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

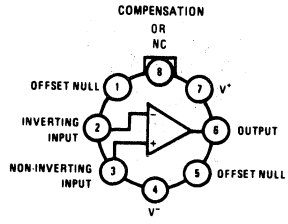
- Wide supply voltage range ±4.0V to ±40V
- Large output voltage swing ±37V
- Wide input common-mode range ±38V
- Input overvoltage protection Full ±40V
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 10.0 nA
- Low input offset current 3.0 nA
- High slew rate—essentially independent of temperature and supply voltage 2.5V/μs
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagrams Section 11 for Packaging

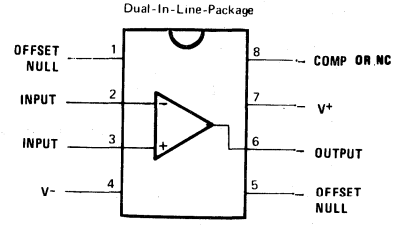
Metal Can Package



TOP VIEW

Order Number LM143H
or LM343H

Dual-In-Line-Package



TOP VIEW

Order Number LM143J
or LM343J, LM343N

Absolute Maximum Ratings (Note 1)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics

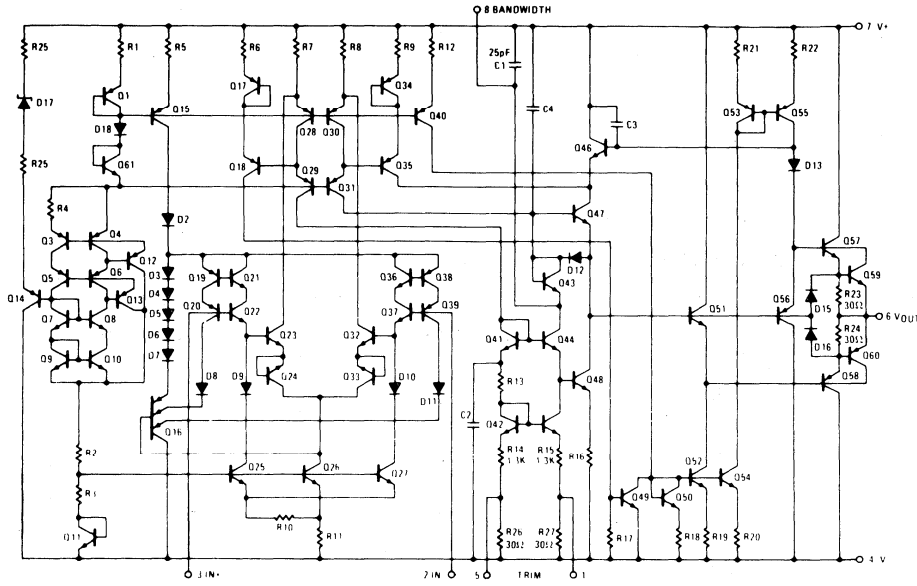
PARAMETER	CONDITIONS	LM143			LM343			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_S = \pm 28V$, $T_A = 25°C$, UNLESS OTHERWISE SPECIFIED		2.0	5.0		2.0	8.0	mV
Input Offset Current			3.0	12.0		3.0	30.0	nA
Input Bias Current			10.0	25.0		12.0	40	nA
Supply Voltage Rejection Ratio			10	100		10	200	μV/V
Output Voltage Swing	$R_L \geq 5$ k	22	25		20	25		V
Large Signal Voltage Gain	$V_{OUT} = 10V$, $R_L \geq 100$ k	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio		80	90		70	90		dB
Input Voltage Range		24	26		22	26		V
Supply Current			2.8	4.0		2.8	5.0	mA
Short Circuit Current			20			20		mA
Slew Rate	$A_V = 1$		2.5			2.5		V/μs
Power Bandwidth	$V_{OUT} = 40\ V_{p-p}$, $R_L = 5$ k THD ≤ 1%		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max (Note 3)			6.0			10	mV
	T_A = Min			6.0			10	mV
Input Offset Current	T_A = Max		0.8	4.5		0.8	14	nA
	T_A = Min		4.0	35.0		4.0	50.0	nA
Input Bias Current	T_A = Max		5.0	35		5.0	55	nA
	T_A = Min		16	50.0		16	55	nA
Large Signal Voltage Gain	$R_L \geq 100$ kΩ	50k	150k		50k	150k		V/V
	$R_L \geq 100$ kΩ	50k	220k		50k	220k		V/V
Output Voltage Swing	$R_L \geq 5.0$ kΩ	22	26		20	26		V
	$R_L \geq 5.0$ kΩ	22	25		20	25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

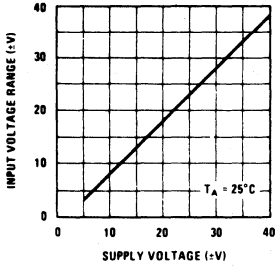
Note 3: For the LM143, $55°C \leq T_A \leq +125°C$ and for the LM343, $0°C \leq T_A \leq 70°C$.

Schematic Diagram

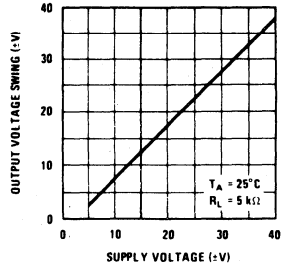


Typical Performance Characteristics

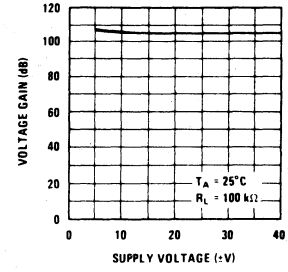
Input Voltage Range



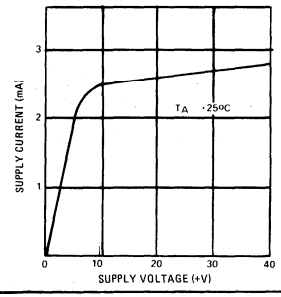
Output Voltage Swing



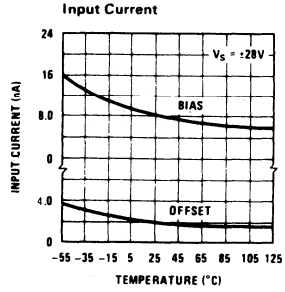
Voltage Gain



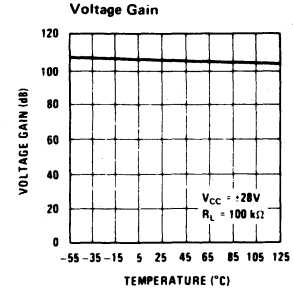
Supply Current



Input Current

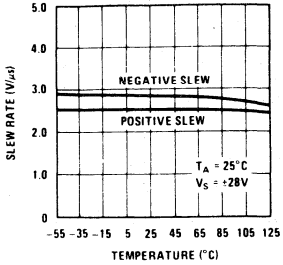


Voltage Gain

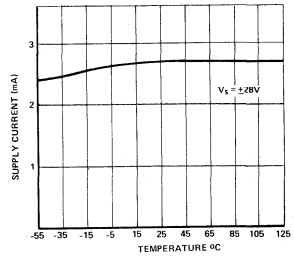


Typical Performance Characteristics (Continued)

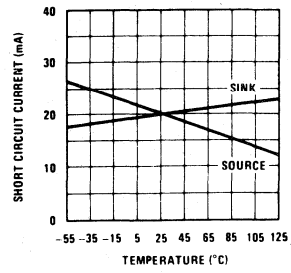
Voltage Follower Slew Rate



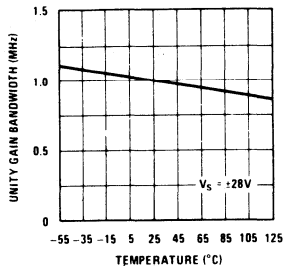
Supply Current



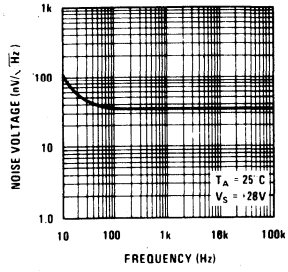
Short Circuit Current



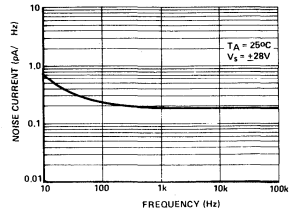
Unity Gain Bandwidth



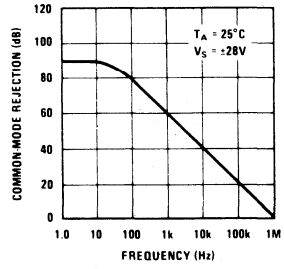
Input Noise Voltage



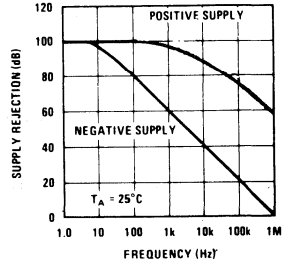
Input Noise Current



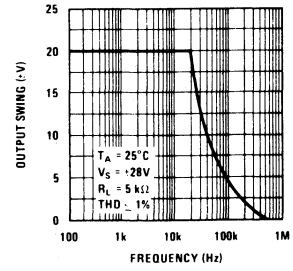
Common-Mode Rejection



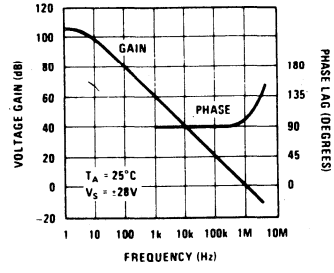
Power Supply Rejection



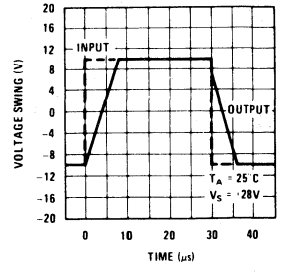
Large Signal Frequency Response



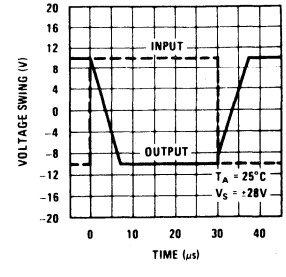
Open Loop Frequency Response



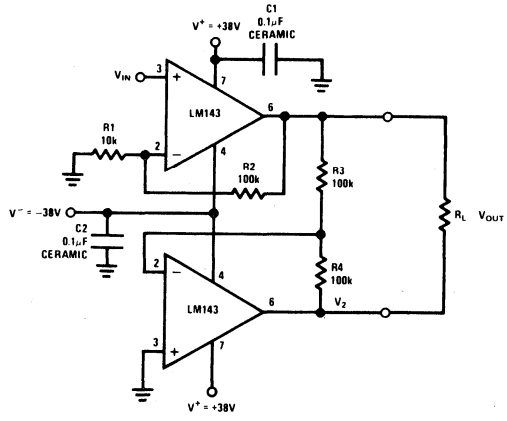
Voltage Follower Pulse Response



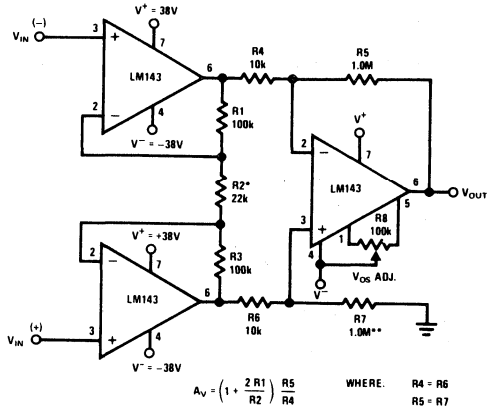
Inverter Pulse Response



Typical Applications ‡



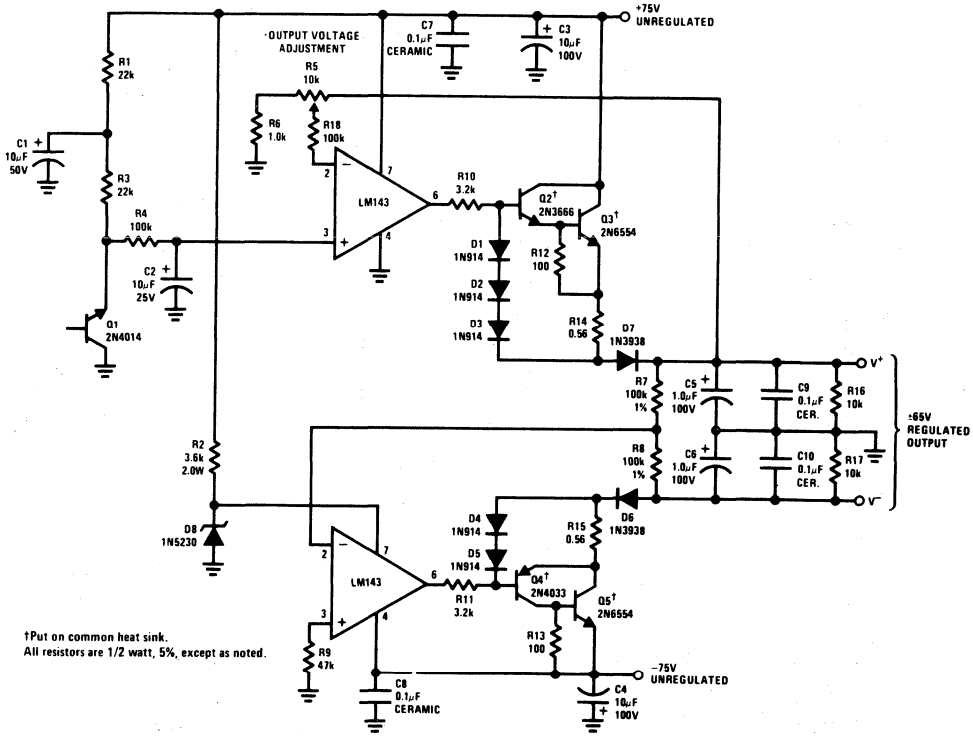
130 Vp-p Drive Across a Floating Load



*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4 – R7 for best CMR.

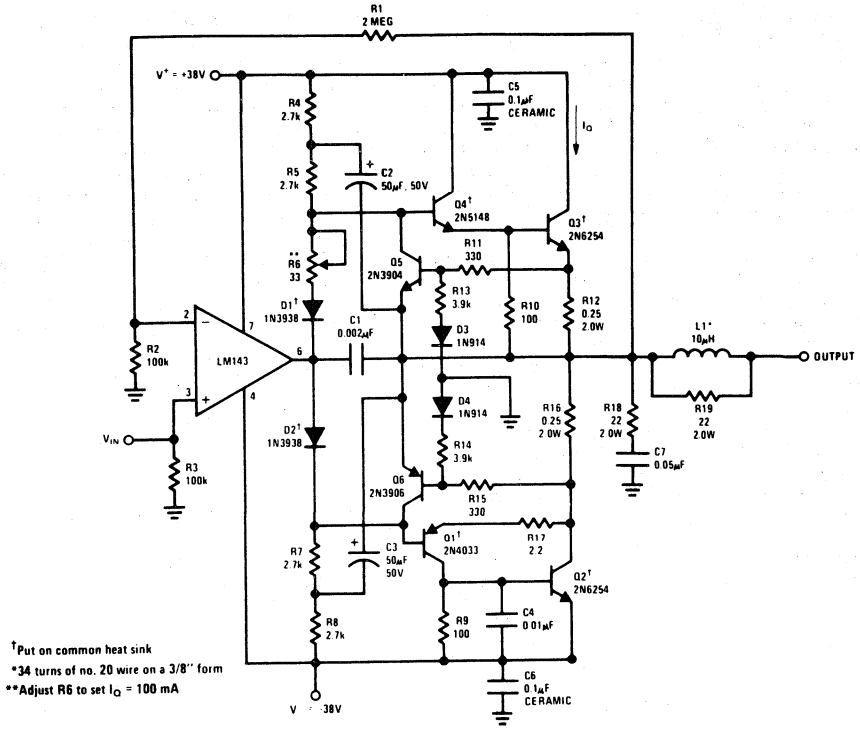
±34V Common-Mode Instrumentation Amplifier



Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection

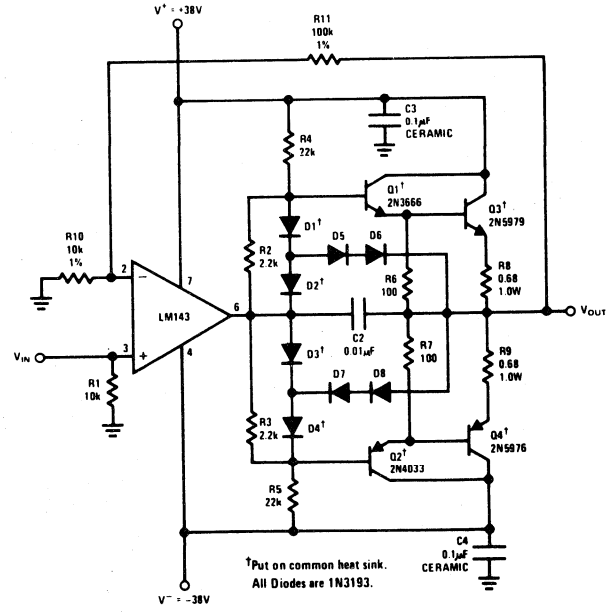
‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Typical Applications (Continued)



†Put on common heat sink
*34 turns of no. 20 wire on a 3/8" form
**Adjust R6 to set I_Q = 100 mA

90W Audio Power Amplifier with Safe Area Protection



†Put on common heat sink.
All Diodes are 1N3193.

1 Amp Power Amplifier with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Application Hints

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of unique high voltage capabilities of the LM143.

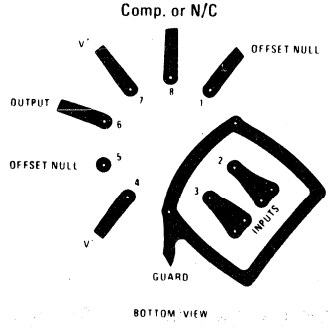


FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package

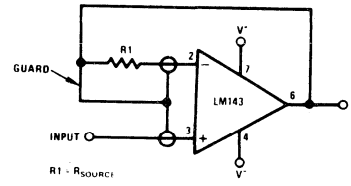


FIGURE 2. Guarded Voltage Follower

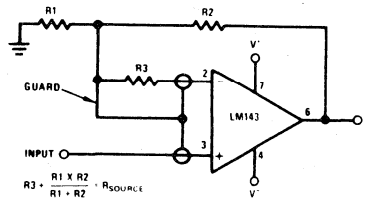


FIGURE 3. Guarded Non-Inverting Amplifier

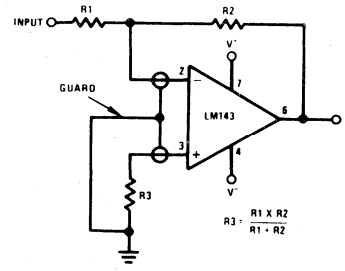


FIGURE 4. Guarded Inverting Amplifier

ANALOG

CMOS Analog Switches

3

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Glossary 3-3

Selection Guide 3-4

Product Information 3-5

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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HI-201HS	High Speed Quad SPST CMOS Analog Switch	3-17
HI-300 thru 307	CMOS Analog Switches	3-26
HI-381/384/387/390	CMOS Analog Switches	3-31
HI-5040 thru 5051	CMOS Analog Switches	3-36
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Analog Switches Glossary

ANALOG SIGNAL RANGE ($\pm V_S$) - The maximum safe input voltage range.

BREAK-BEFORE-MAKE-DELAY (t_{OPEN}) - The elapsed time between the turn-off of one switch and the corresponding turn-on of another switch for a common change in logic state. This delay is measured between the 50% points of the output transitions.

CHANNEL INPUT CAPACITANCE (C_{SOFF}) The capacitance between the analog input and ground with the channel "OFF." This capacitance consists primarily of the source-body capacitance.

CHANNEL OUTPUT CAPACITANCE (C_{DOFF}) The capacitance between the analog output and ground with the channel "OFF". This capacitance consists of the sum of the drain-body capacitances.

CHANNEL OUTPUT CAPACITANCE (C_{DON}) - The capacitance between the analog output and ground with the channel "ON".

CHARGE INJECTION - The amount of charge transferred to a specified load capacitance due to the switch changing state.

CROSSTALK - The amount of cross coupling from an "OFF" analog input to the output of another "ON" channel output.

DIGITAL INPUT CAPACITANCE - The capacitance between a digital input and ground.

INPUT LOW LEAKAGE CURRENT (I_{AL}) - The current measured at the digital input with a logic low applied.

INPUT LOW THRESHOLD (V_{AL}) - The maximum allowable voltage that can be applied to the digital inputs and still be recognized by the device as a low input.

INPUT HIGH LEAKAGE CURRENT (I_{AH}) - The current measured at the digital input with a logic high applied.

INPUT HIGH THRESHOLD (V_{AH}) - The minimum voltage that can be applied to the digital inputs and still be recognized by the device as a high input.

INPUT TO OUTPUT CAPACITANCE (CD_{SOFF}) - The capacitance between the analog input and output when the channel is "OFF".

"OFF" INPUT LEAKAGE CURRENT (I_{SOFF}) - The current measured at the input of an "OFF" channel with a specified voltage applied to both input and output. This current consists largely of the diode leakage current of the source- body junctions.

OFF ISOLATION - The feedthrough of an applied signal through an "OFF" switch to the output. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at high frequencies.

"OFF" OUTPUT LEAKAGE CURRENT (I_{DOFF}) - The current measured at the output of an "OFF" channel with a specified voltage applied to both input and output. This current is due largely to the diode leakages of the drain-body junctions.

"ON" CHANNEL LEAKAGE CURRENT (I_{DON}) - The current flowing through the source-body and drain body junctions of the "ON" channel. This current is measured with a specified voltage applied to both the input and output.

"ON" RESISTANCE (R_{ON}) - The series "ON" channel resistance measured between the input and output terminals under a specified range of input voltages.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the switch in a no load condition.

SWITCH TURN "OFF" TIME (t_{OFF}) - The time required to deactivate an "ON" switch to an "OFF" state. This time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

SWITCH TURN "ON" TIME (t_{ON}) - The time required to activate an "OFF" switch to an "ON" state. This time is measured for the 50% point of the logic input to the time the output reaches 90% of the final value.

CMOS Switches Selection Guide

FUNCTION	DEVICE	R_{ON} (Ω) (TYP)	$I_{D(OFF)}$ (NA) (TYP)	$t_{(ON)}$ (NS) (TYP)	$t_{(OFF)}$ (NS) (TYP)	P_D (mW) (TYP)
SPST	HI-5040	50	0.5	370	280	1.5
2 x SPST	HI-200	55	1	240	180	15
	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
	HI-5048	25	0.5	370	280	1.5
	HI-5041	50	0.5	370	280	1.5
4 x SPST	HI-201	55	1	180	155	15
	HI-201HS	30	0.3	30	40	120
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
	HI-5050	25	0.5	370	280	1.5
	HI-5042	50	0.5	370	280	1.5
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
	HI-5051	25	0.5	370	280	1.5
	HI-5043	50	0.5	370	280	1.5
DPST	HI-5044	50	0.5	370	280	1.5
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1
	HI-5049	25	0.5	370	280	1.5
	HI-5045	50	0.5	370	280	1.5
DPDT	HI-5046A	25	0.5	370	280	1.5
	HI-5046	50	0.5	370	280	1.5
4PST	HI-5047A	25	0.5	370	280	1.5
	HI-5047	50	0.5	370	280	1.5

NOTE: All data represents typical room temperature specifications at ±15V supplies. For guaranteed and tested specifications, consult the device data sheet.

HARRIS

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

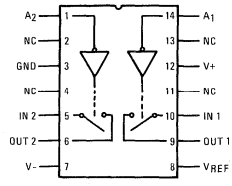
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

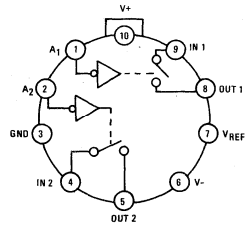
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters,and op amp gain switching networks.

HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

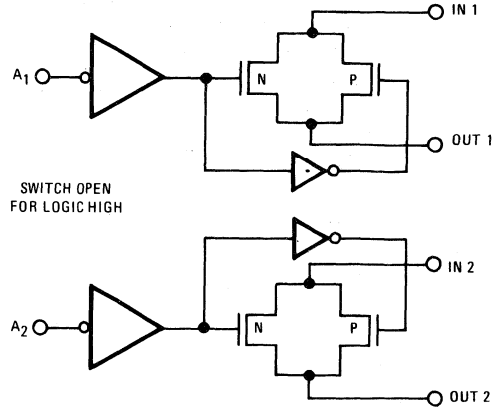
TOP VIEWS





CASE TIED TO V-

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-200-2 -55°C to +125°C MIN.	HI-200-2 -55°C to +125°C TYP.	HI-200-2 -55°C to +125°C MAX.	HI-200-5** 0°C to +75°C MIN.	HI-200-5** 0°C to +75°C TYP.	HI-200-5** 0°C to +75°C MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02	5		.02	50	nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

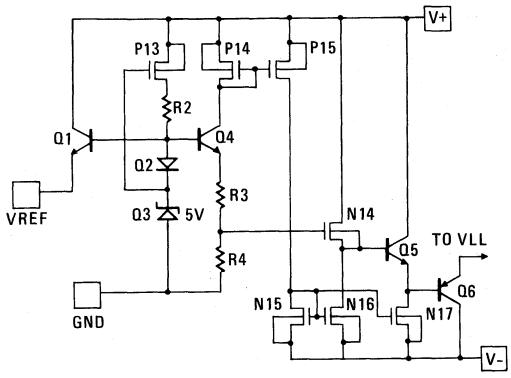
NOTES: 1. $V_{OUT} = \pm 10V$ I_{OUT} = 1mA
2. Digital Inputs are MOS gates - Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V for Both Switches
6. Refer to leakage current measurement diagram on page 3-9

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

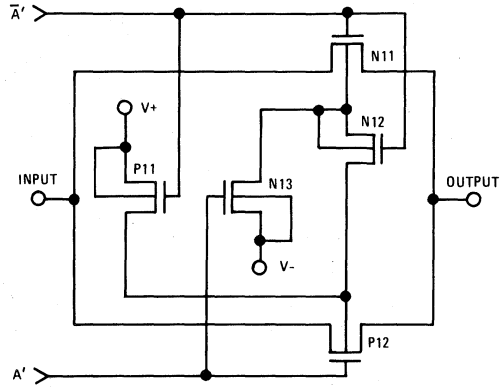
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT

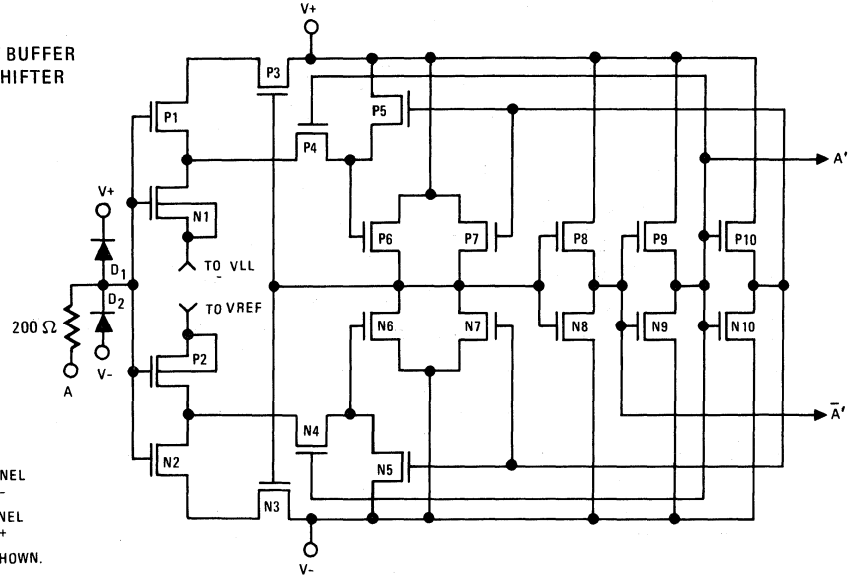
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



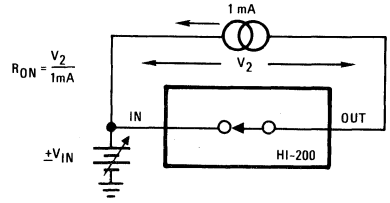
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

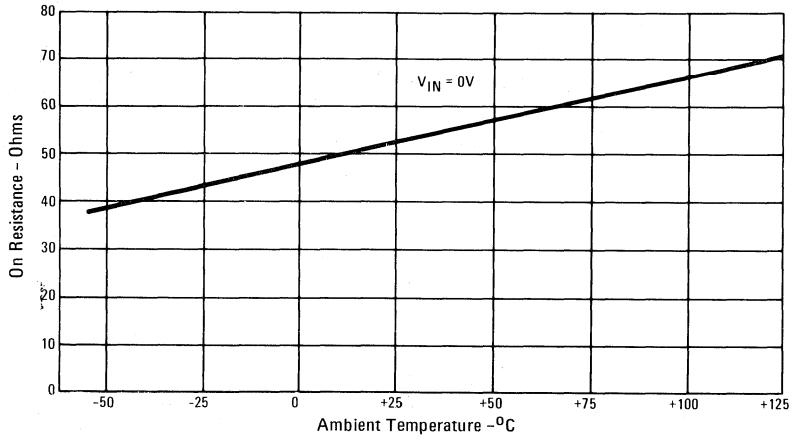
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

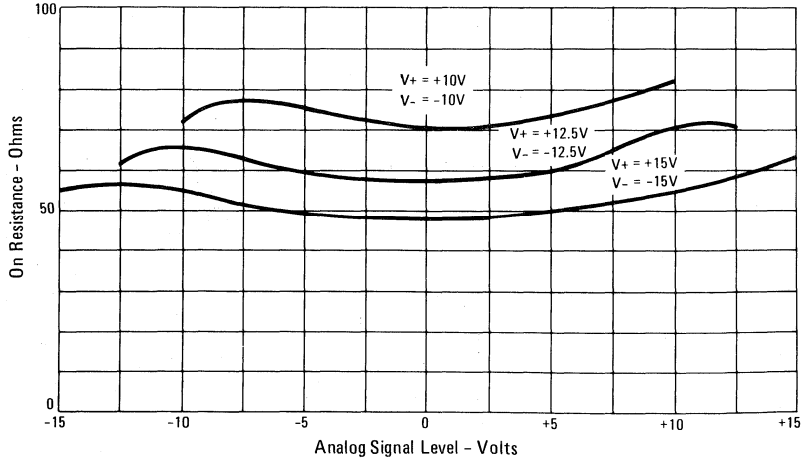
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

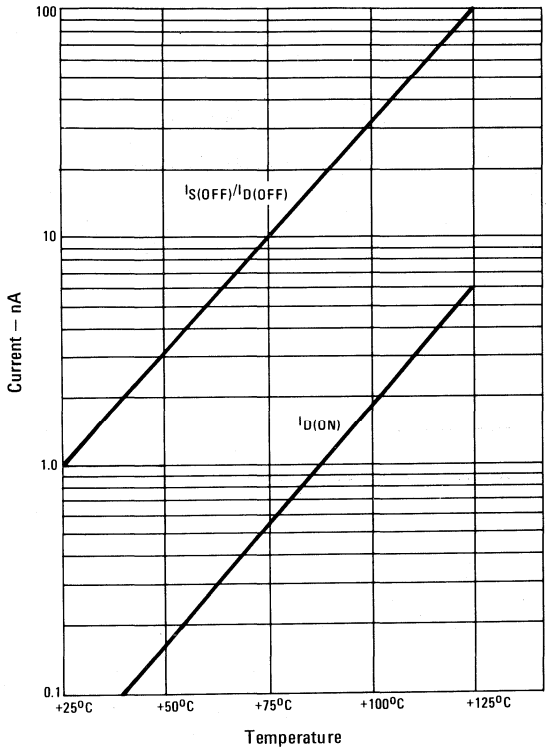


(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

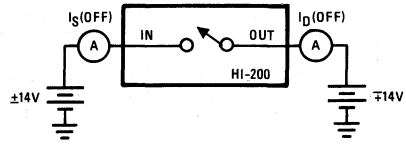


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

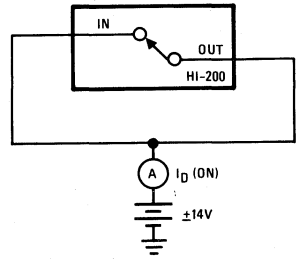
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



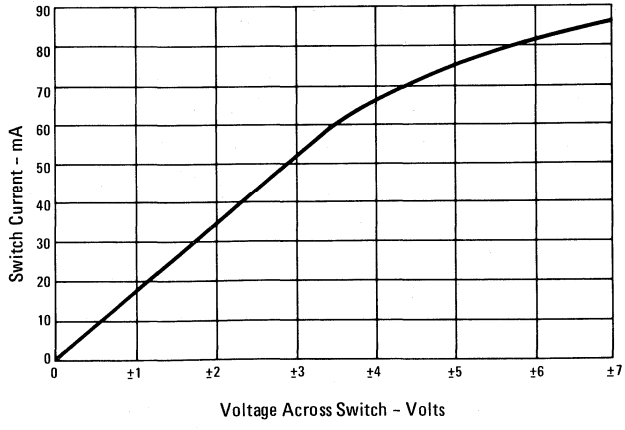
OFF LEAKAGE CURRENT vs. TEMPERATURE



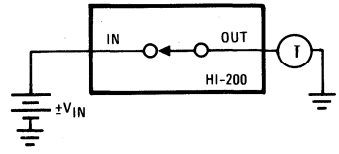
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

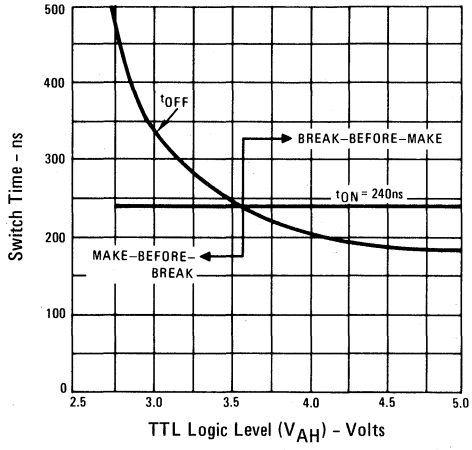


SWITCH CURRENT vs. VOLTAGE

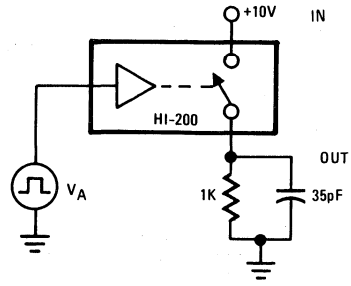


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

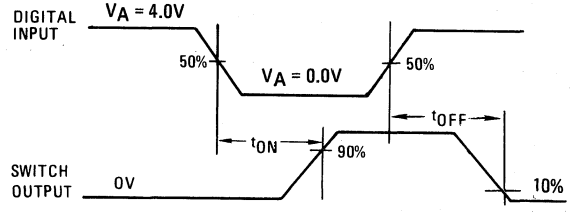
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



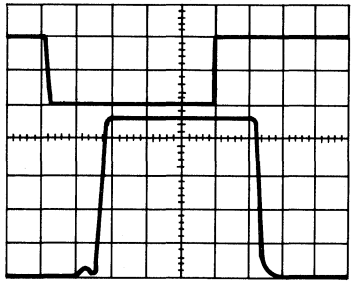
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

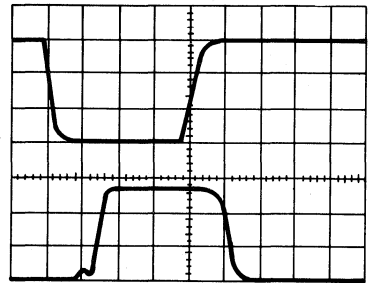


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



Top: TTL Input Vertical: 2V/Div.
Bottom: Output Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 200ns/Div.

HARRIS

HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 55 Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

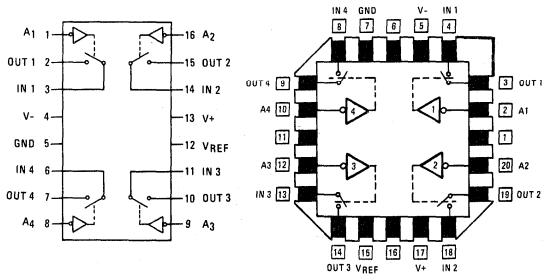
HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

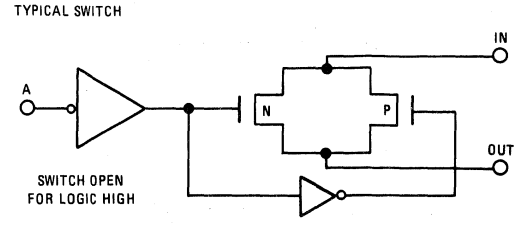
HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

PIN OUT

TOP VIEWS



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	44V (±22)	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified :
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V
For Test Conditions consult Performance Characteristics

PARAMETER	TEMP.	HI-201-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-201-5 * 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C		30			30		ns
t_{ON}, Switch ON Time	+25°C		185	500		185		ns
t_{OFF}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$ } Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$ } Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation (Note 5)	+25°C		15			15		mW
	Full			60			60	mW
I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I-, Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

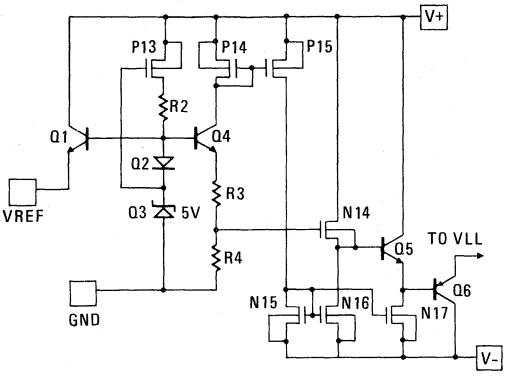
NOTES: 1. V_{OUT} = ± 10V I_{OUT} = 1mA
2. Digital Inputs are MOS gates - Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1kΩ , C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V for All Switches
6. Refer to leakage current measurement diagram on page 3-15

* Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

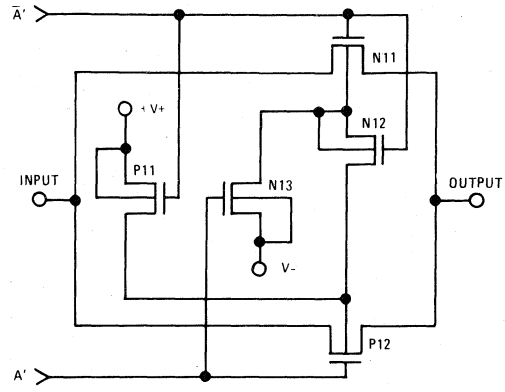
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT

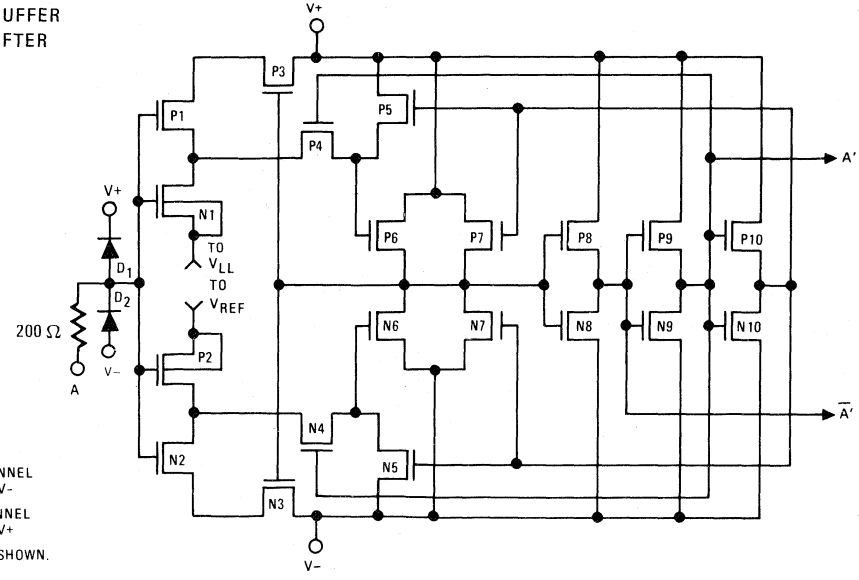
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



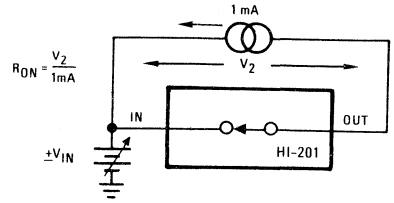
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

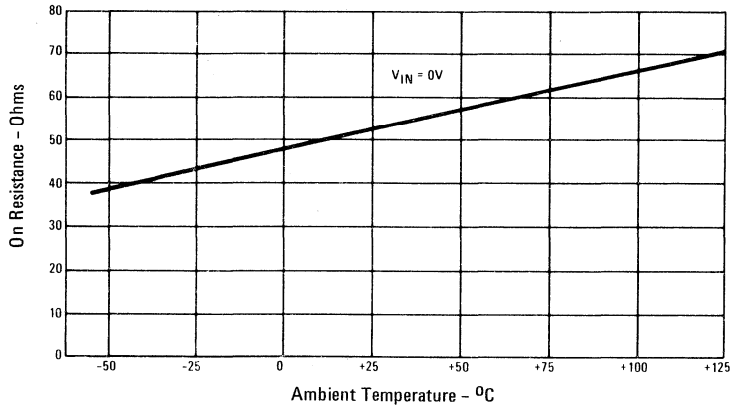
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4\ V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

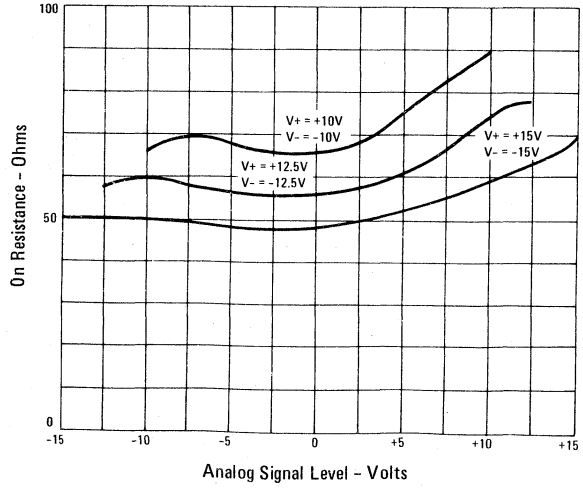
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

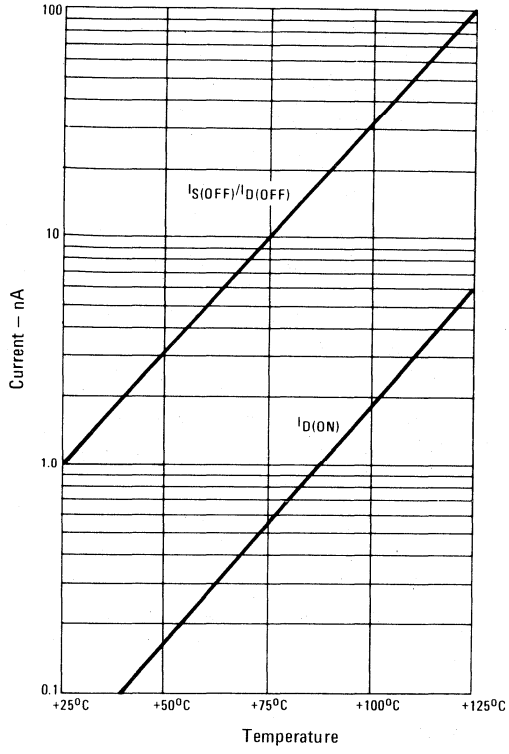


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

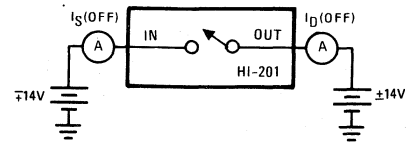


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

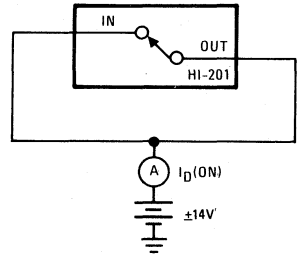
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



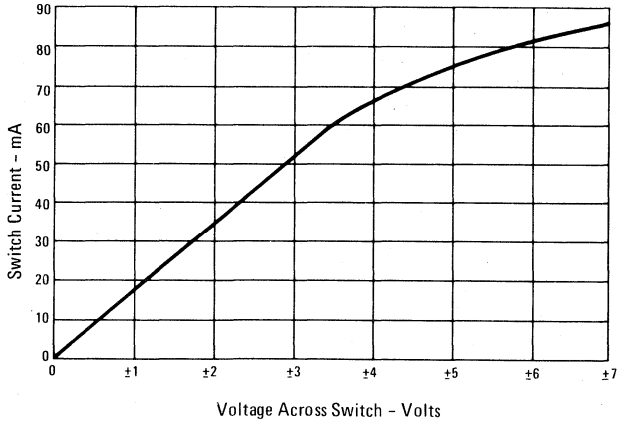
OFF LEAKAGE CURRENT vs. TEMPERATURE



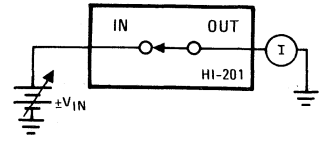
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

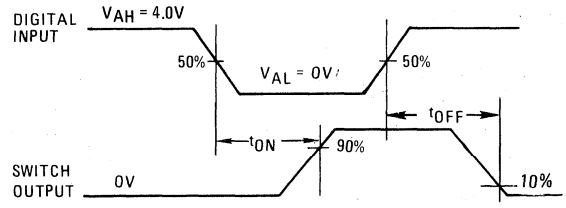


SWITCH CURRENT vs. VOLTAGE

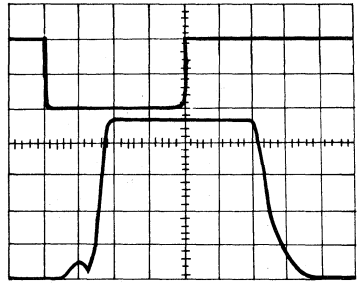


SWITCHING WAVEFORMS

LOGIC "0" = SWITCH ON



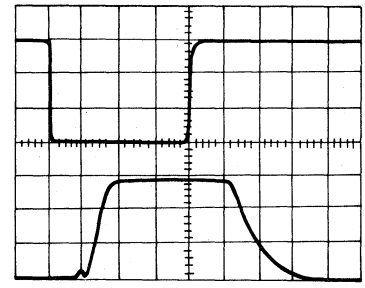
t_{ON}, t_{OFF}(TTL INPUT)
V_{IN} = 4.0V



Top: TTL Input
Bottom: Output

Horizontal: 100ns/Div.
Vertical: 2V/Div.

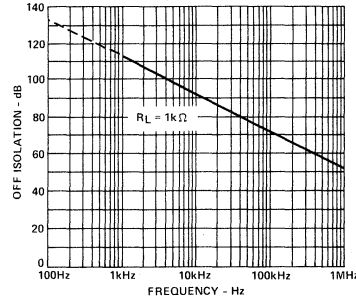
t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

OFF ISOLATION VS. FREQUENCY



HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

FEATURES

- FAST SWITCHING TIMES — t_{on} = 30ns, t_{off} = 40ns
- LOW ON RESISTANCE — 30Ω
- PIN COMPATIBLE WITH STANDARD HI-201
- WIDE ANALOG VOLTAGE RANGE (± 15V SUPPLIES) — ±15V
- LOW CHARGE INJECTION (± 15V SUPPLIES) — 10pC
- TTL COMPATIBLE
- SYMMETRICAL SWITCHING

ANALOG CURRENT RANGE — 80mA

APPLICATIONS

- HIGH SPEED MULTIPLEXING
- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS
- INTEGRATOR RESET CIRCUITS

DESCRIPTION

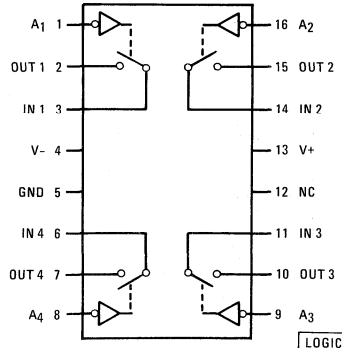
The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris dielectric isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note #543).

Available in a 16 lead dual-in-line package, the HI-201HS-2 is specified over the temperature range of -55°C to +125°C and the HI-201HS-5 from 0°C to +75°C.

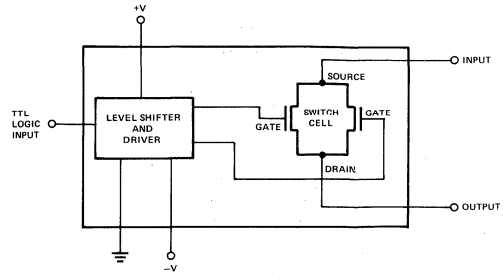
PINOUT

TOP VIEW



LOGIC	SWITCH
0	ON
1	OFF

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Between Pins 4 and 13)	36V	Total Power Dissipation (Note 2)	750mW
		Maximum Junction Temperature	175°C
Digital Input Voltage (Pins 1, 8, 9, 16)	$+V_{SUPPLY}$ +4V	Operating Temperature	
	$-V_{SUPPLY}$ -4V	HI-201HS-2	-55°C to +125°C
		HI-201HS-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{SUPPLY}$ +2.0V	HI-201HS-5	0°C to +75°C
Pins 2, 3, 6, 7, 10, 11, 14, 15	$-V_{SUPPLY}$ -2.0V	Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V, GND = 0V

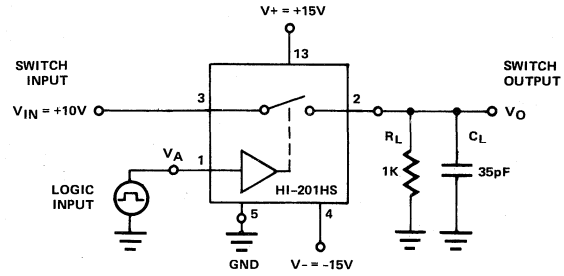
PARAMETER	TEMP.	HI-201HS-2 MIN.	HI-201HS-2 TYP.	HI-201HS-2 MAX.	HI-201HS-5 MIN.	HI-201HS-5 TYP.	HI-201HS-5 MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 3)	+25°C		30	50		30	50	Ω
	Full			75			75	Ω
R_{ON} Match	+25°C		3			3		%
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		.3	1		.3	1	nA
	Full			100			50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		.3	1		.3	1	nA
	Full			100			50	nA
$I_{D(ON)}$, On Leakage Current	+25°C		.1	1		.1	1	nA
	Full			100			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	+25°C	2.0			2.0			V
	Full	2.4			2.4			V
I_{AL}, Input Leakage Current (Low)	+25°C		200			200		μA
	Full			-500			-500	μA
I_{AH}, Input Leakage Current (High)	+25°C		20			20		μA
	Full			+40			+40	μA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch ON Time (Note 4)	+25°C		30	50		30	50	ns
t_{OFF1}, Switch OFF Time (Note 4)	+25°C		40	50		40	50	ns
t_{OFF2}, Switch OFF Time (Note 4)	+25°C		150			150		ns
Output Settling Time 0.1%	+25°C		180			180		ns
"Off Isolation" (Note 5)	+25°C		72			72		dB
Crosstalk (Note 6)	+25°C		86			86		dB
Charge Injection (Note 7)	+25°C		10			10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10			10		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		10			10		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		30			30		pF
C_A, Digital Input Capacitance	+25°C		18			18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5			.5		pF
POWER REQUIREMENTS (Note 8)								
P_D, Power Dissipation	+25°C		120			120		mW
	Full			240			240	mW
I^+, Current (Pin 13)	+25°C		4.5			4.5		mA
	Full			10.0			10.0	mA
I^-, Current (Pin 4)	+25°C		3.5			3.5		mA
	Full			6			6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate 8mW/°C Above T_A = +75°C
   θ_{jA} = 100°C/W θ_{jC} = 32°C/W
3. V_{OUT} = ±10V, I_{OUT} = 1mA
4. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +3V
   (See Switching Waveforms)
5. V_A = 3V, R_L = 1KΩ, C_L = 10pF, V_{IN} = 3 VRMS, f = 100kHz
6. V_A = 3V, R_L = 1KΩ, f = 100kHz, V_{IN} = 3 VRMS
7. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω
   $\Delta Q = C_L \times \Delta V_O$
8. V_A = 3V or V_A = 0 for all switches

TEST CIRCUIT

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

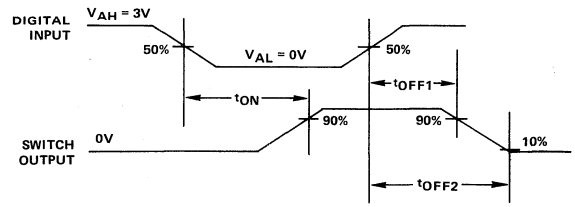


$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

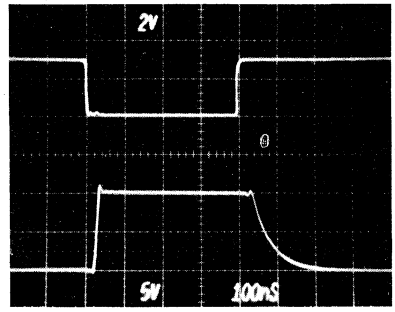
C_L INCLUDES $C_{FIXTURE}$ + C_{PROBE}

SWITCHING WAVEFORMS

LOGIC "0" = SWITCH ON



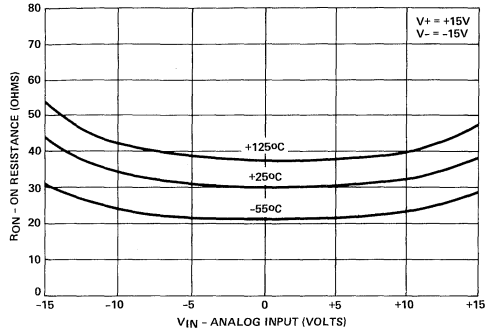
t_{ON}, t_{OFF}(TTL INPUT)
V_{AH} = +3.0V



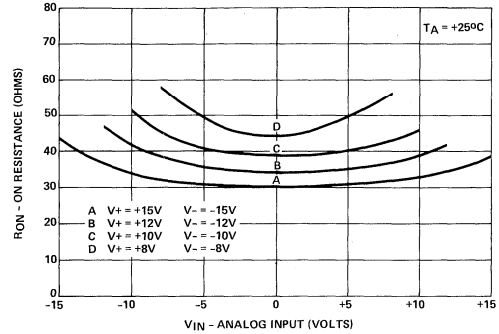
Top: TTL Input (2V/ON)
Bottom: Output (5V/Div.) Horizontal: 100ns/Div.

TYPICAL PERFORMANCE CURVES

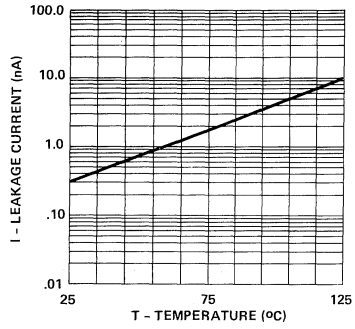
ON RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE



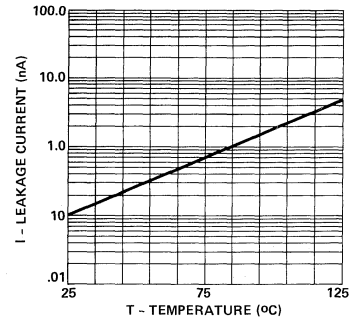
ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



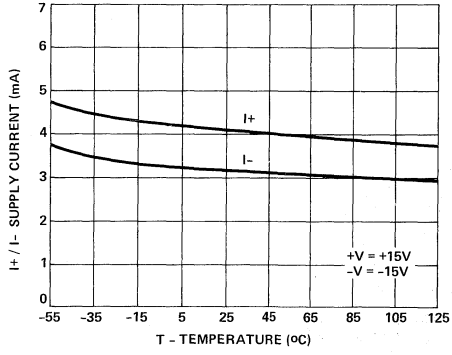
$I_{S(OFF)}$ or $I_{D(OFF)}$ vs TEMPERATURE *



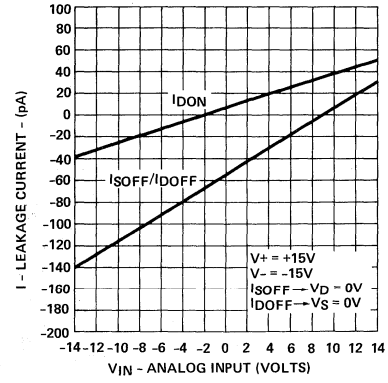
$I_{D(ON)}$ vs TEMPERATURE *



SUPPLY CURRENT vs TEMPERATURE



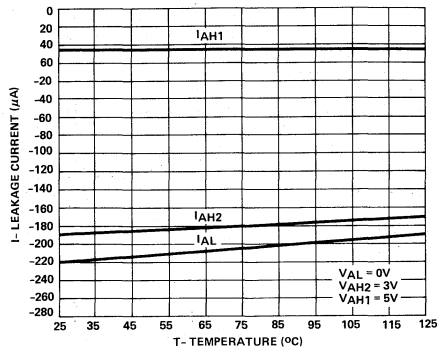
LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE



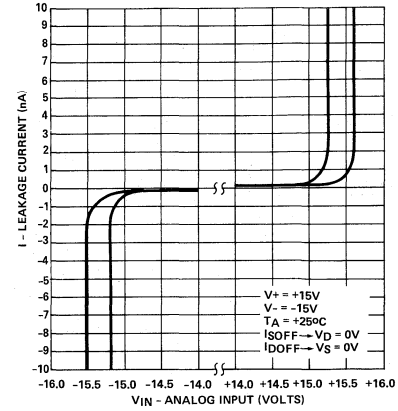
*THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

TYPICAL PERFORMANCE CURVES (Continued)

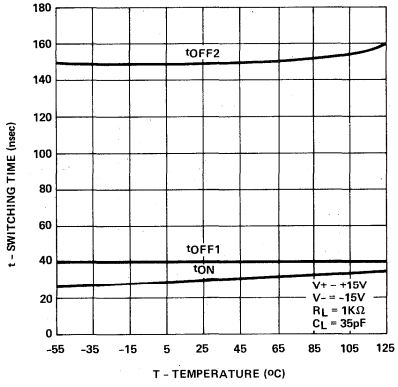
DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE *



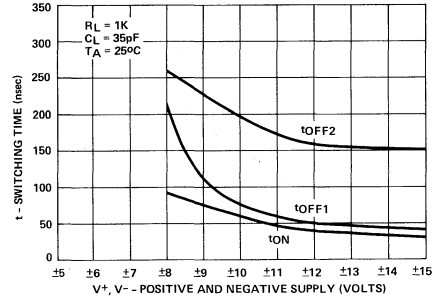
LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE ($V_{IN} \geq +14V$, $V_{IN} \leq -14V$)



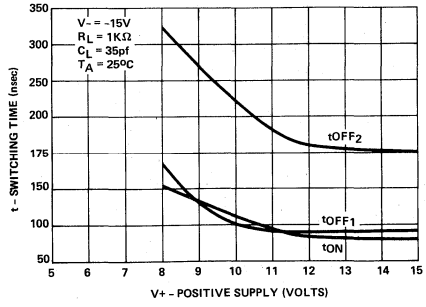
SWITCHING TIME vs TEMPERATURE



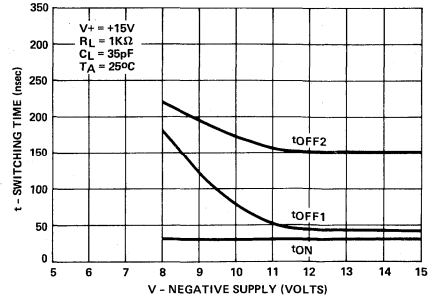
SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE



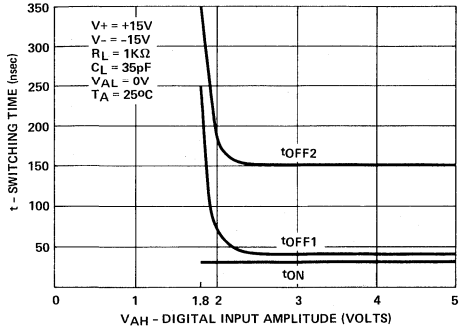
SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE



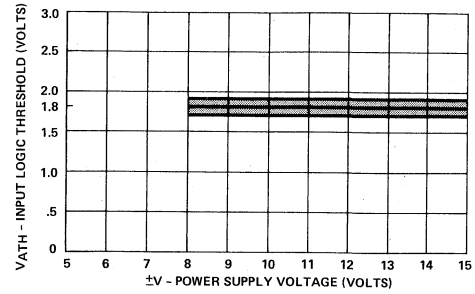
*THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

TYPICAL PERFORMANCE CURVES (Continued)

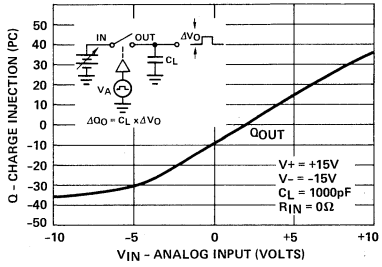
SWITCHING TIME vs INPUT LOGIC AMPLITUDE



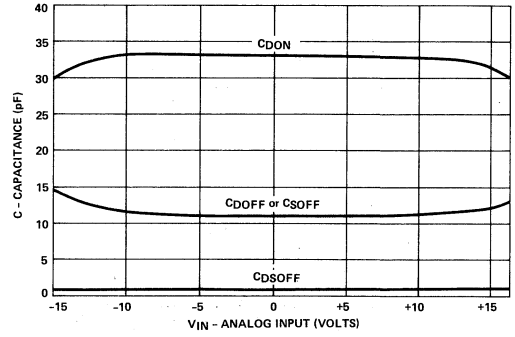
INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGES



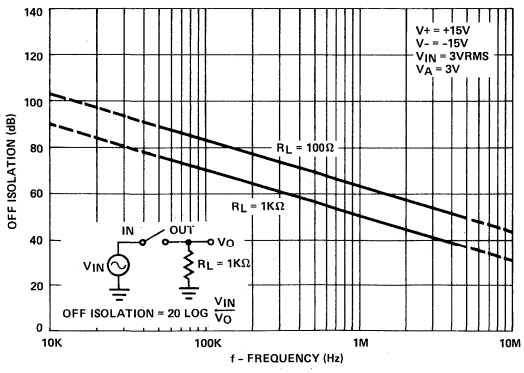
CHARGE INJECTION vs ANALOG INPUT



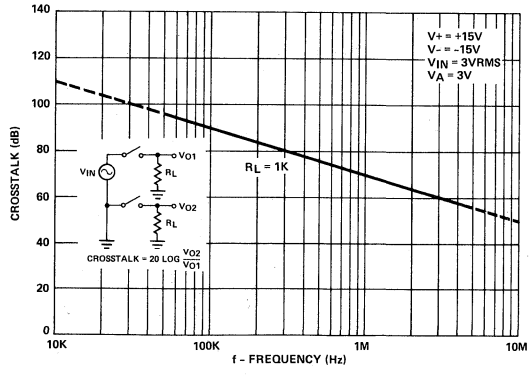
CAPACITANCE vs ANALOG INPUT



OFF ISOLATION vs FREQUENCY

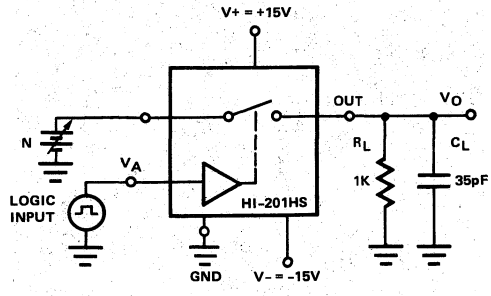


CROSSTALK vs FREQUENCY



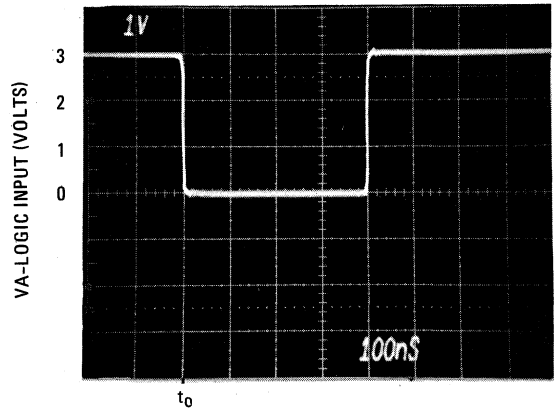
SWITCHING CHARACTERISTICS vs INPUT VOLTAGE

Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit.

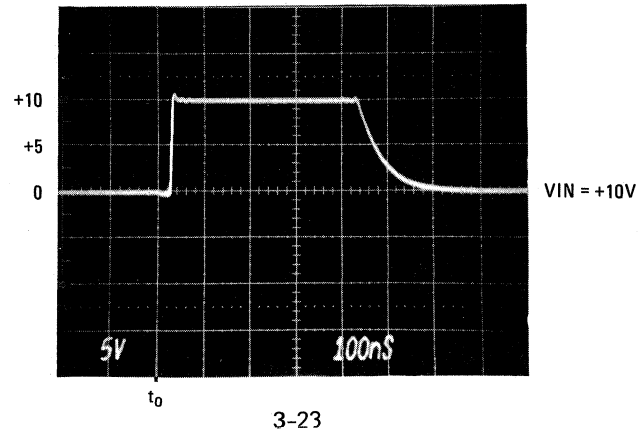


If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times.

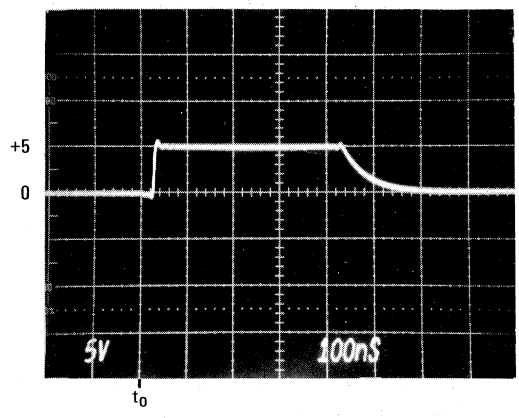
LOGIC INPUT



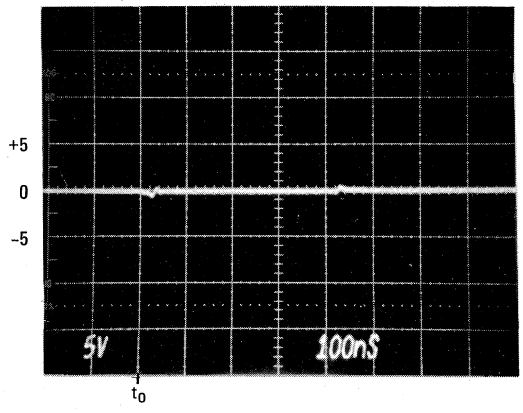
VO – OUTPUT SWITCHING WAVEFORMS



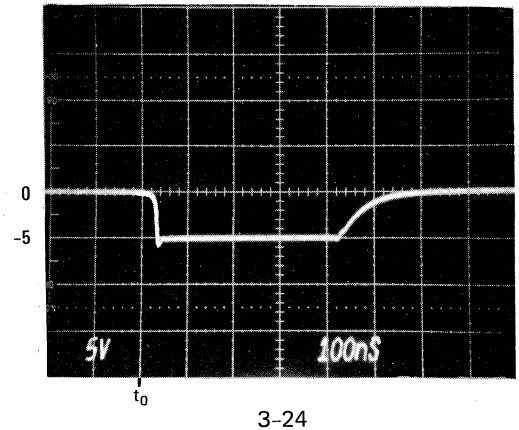
VO – OUTPUT SWITCHING WAVEFORMS



VIN = +5V



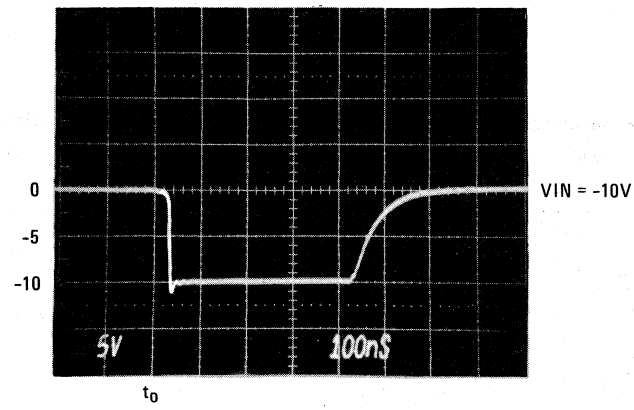
VIN = 0V



VIN = -5V

SWITCHING CHARACTERISTICS (Continued)

VO – OUTPUT SWITCHING WAVEFORMS



APPLICATION INFORMATION

LOGIC COMPATIBILITY

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

CHARGE INJECTION

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

POWER SUPPLY CONSIDERATIONS

The electrical characteristics specified in this data sheet are guaranteed for power supplies of $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only;

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 \leq \pm V_S \pm 15V$	Minimal variation
$\pm V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$\pm V_S < \pm 10V$	Not recommended

SINGLE SUPPLY

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ± 15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (± 15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

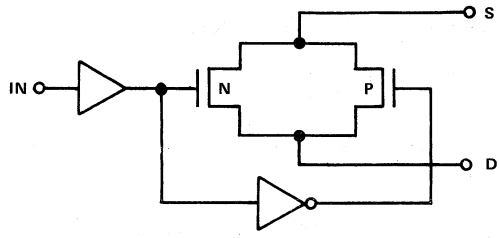
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP. @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL, CMOS COMPATIBLE
- SYMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER (TYP. FOR HI-300 - 303) 1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE, BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH 300 SERIES

DESCRIPTION

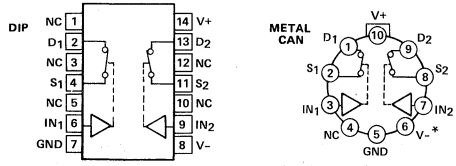
The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only) , low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300-303, a few hundred microwatts for the HI-304-307).

The HI-300-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

All the devices are available in a 14 pin epoxy or ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin metal can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

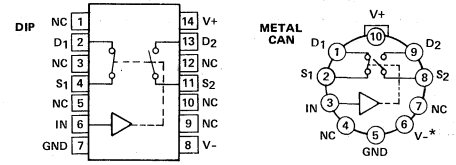
DUAL SPST HI-300 & HI-304
(TOP VIEWS)



LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

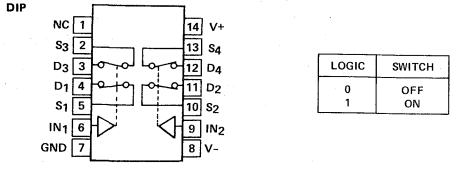
SPDT HI-301 & HI-305
(TOP VIEWS)



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

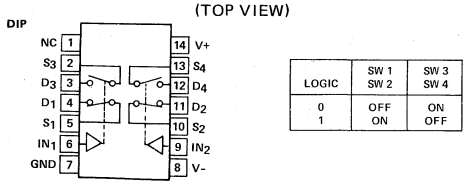
*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306
(TOP VIEW)



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SPECIFICATIONS HI-300 - HI-307

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies 44V (±22V)

Digital Input Voltage V^+ +4.0V
V^- -4.0V

Analog Input Voltage V^+ 1.5V
V^- 1.5V

Total Power Dissipation
14 Pin Epoxy DIP 526mW
14 Pin Ceramic DIP 588mW
10 Pin Metal Can* 435mW
*Derate 6.9mW/0°C Above T_A = 70°C

Operating Temperature HI-3XX-2 -55°C to +125°C
HI-3XX-5 0°C to +75°C

Storage Temperature -65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified; Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303 : V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307 : V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	Full		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		0.03	1		0.03	5	nA
	Full		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level *	Full			0.8			0.8	V
V_{INH} Input High Level *	Full	4			4			V
V_{INL} Input Low Level **	Full			3.5			3.5	V
V_{INH} Input High Level **	Full	11			11			V
I_{INL} Input Leakage Current (Low) (Note 5)	Full			1			1	μA
I_{INH} Input Leakage Current (High) (Note 5)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN} Break-Before-Make Delay ***	+25°C		60			60		ns
t_{ON} Switch On Time *	+25°C		210	300		210	300	ns
t_{OFF} Switch Off Time *	+25°C		160	250		160	250	ns
t_{ON} Switch On Time **	+25°C		160	250		160	250	ns
t_{OFF} Switch Off Time **	+25°C		100	150		100	150	ns
Off Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current * (Note 8)	+25°C		0.09	0.5		0.09	0.5	mA
	Full			1			1	mA
I- Current * (Note 8)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA

* HI-300 thru HI-303 Only; ** HI-304 thru HI-307 Only; *** HI-301, HI-303, HI-305, HI-307 Only

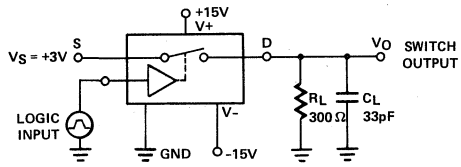
ELECTRICAL CHARACTERISTICS NOTES:

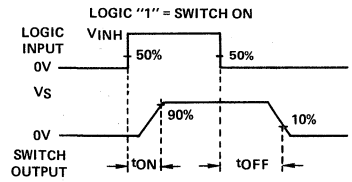
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm$ 10V, I_{OUT} = -10mA On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V, V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k. $C_L = C_{FIXTURE} + C_{PROBE}$, "Off Isolation" = 20logVS/VD.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 -303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304-307)
8. V_{IN} = 4V (one input) (all other inputs = 0V)
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

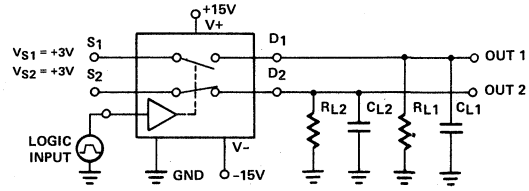
SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

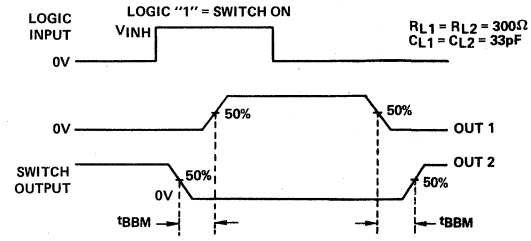




BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

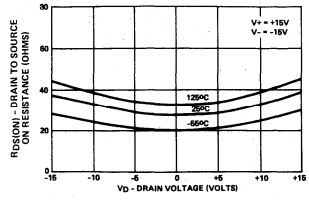
SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V



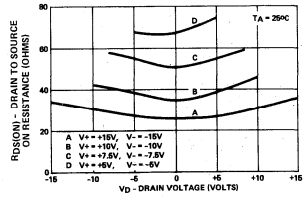


TYPICAL PERFORMANCE CURVES

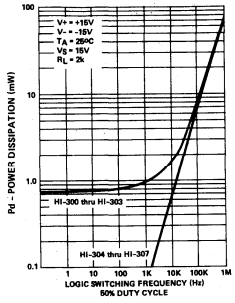
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



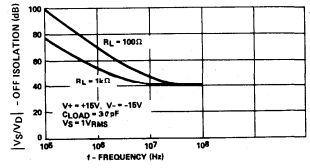
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



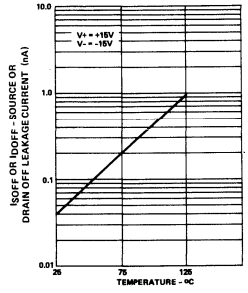
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



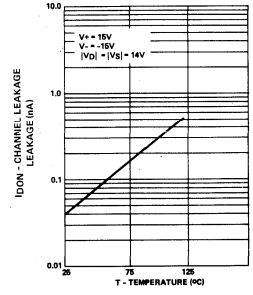
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *

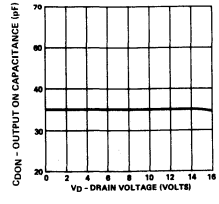


$I_{D(ON)}$ VS. TEMPERATURE *

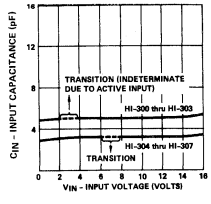


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

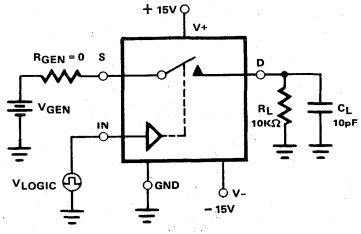
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



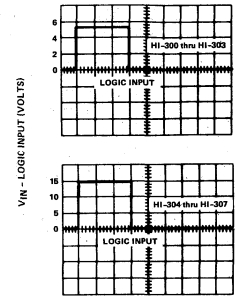
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

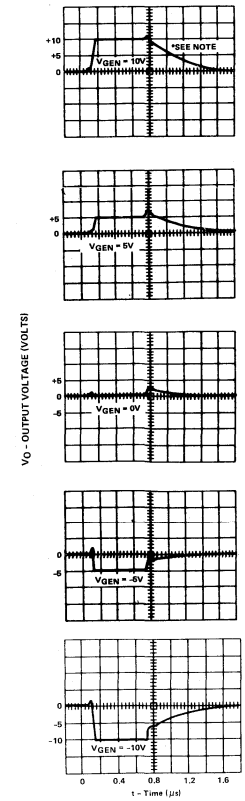


Typical delay, rise, fall, settling times, and switching transients in this circuit.

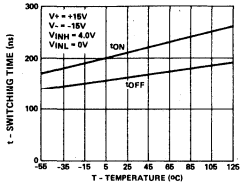


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

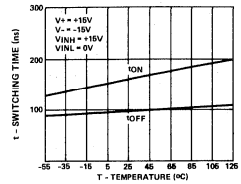




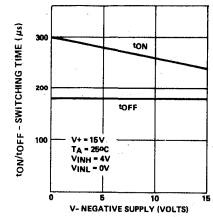
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



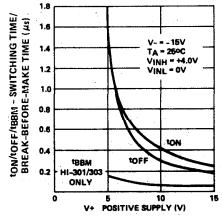
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



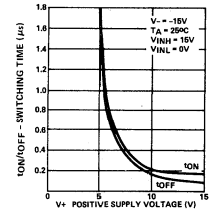
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



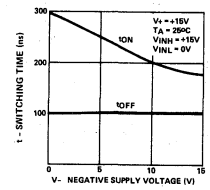
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



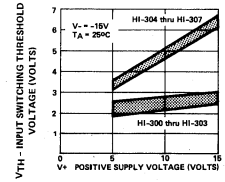
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307



INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307



HARRIS

HI-381/384/387/390

CMOS Analog Switches

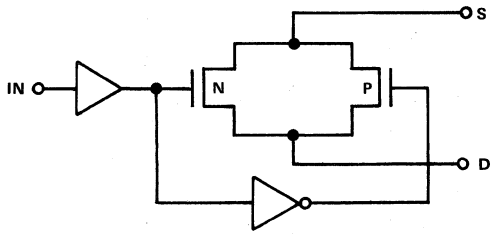
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL COMPATIBLE
- SYMMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER (TYP.) 1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH - 300 SERIES

DESCRIPTION

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

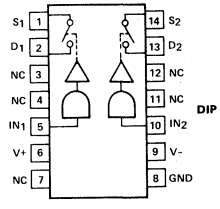
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

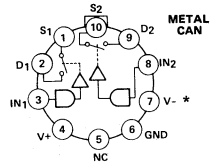
The HI-381 and HI-387 switches are available in a 14 pin epoxy or ceramic DIP or10 pin metal can. The HI-384 and HI-390 are available in a 16 pin epoxy or ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

DUAL SPST HI-381

(TOP VIEWS)



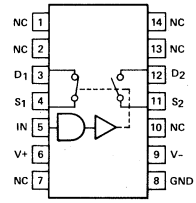


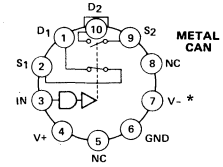
LOGIC	SW 1 SW 2
0	ON
1	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387

(TOP VIEWS)



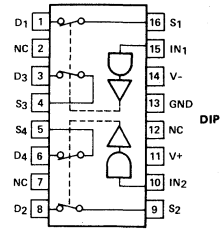


LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384

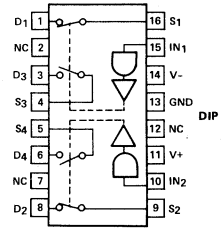
(TOP VIEW)



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390

(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies 44V (±22)

Digital Input Voltage
V^++4.0V
V^- -4.0V

Analog Input Voltage
V^++1.5V
V^- -1.5V

Storage Temperature Range -65°C to +150°C

Total Power Dissipation

14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
16 Pin Epoxy DIP	625mW
16 Pin Ceramic DIP	685mW
10 Pin Metal Can*	435mW

*Derate 6.9mW/°C above T_A = 70°C

Operating Temperature

HI-3XX-2	-55°C to +125°C
HI-3XX-5	0°C to +75°C

ELECTRICAL CHARACTERISITICS

Unless otherwise specified; Supplies = +15V, -15V; VIN = Logic Input, VIN for logic "1" = 4V, for logic 0 = .8V

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	FULL	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	FULL		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current	+25°C		.04	1		.04	5	nA
(Note 3)	FULL		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		.03	1		.03	5	nA
	FULL		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level	FULL			.8			.8	V
V_{INH} Input High Level	FULL	4			4			V
I_{INH} Input Leak. Current (High) (Note 5)	FULL			1			1	μA
I_{INL} Input Leak. Current (Low) (Note 5)	FULL			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 only)	+25°C		60			60		ns
t_{ON}, Switch ON Time	+25°C		210	300		210	300	ns
t_{OFF}, Switch OFF Time	+25°C		160	250		160	250	ns
OFF Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current (Note 8)	+25°C		.09	.5		.09	.5	mA
	FULL			1			1	mA
I- Current (Note 8)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I+ Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I- Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA

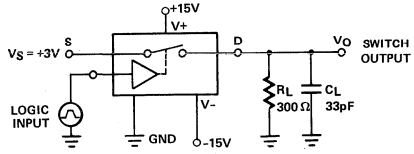
ELECTRICAL CHARACTERISTICS NOTES :

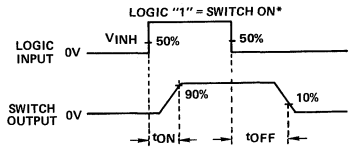
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ on resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20\log V_S/V_D$.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. V_{IN} = 4V. (one input) (all other inputs = 0)
9. V_{IN} = 0.8V. (all inputs)
10. To drive from DTL/TTL circuits, pull-up resistors to +5V Supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V

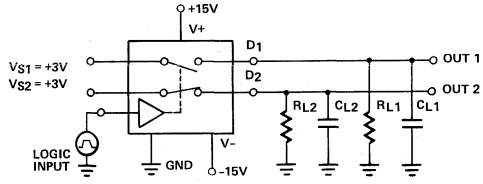


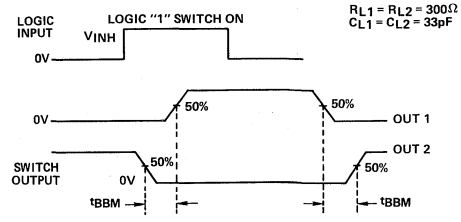


*Inverted logic for HI-381

BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

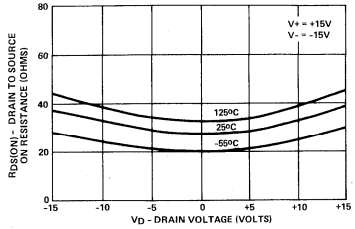
SWITCH TYPE	V_{INH}
HI-387 and HI-390	5V



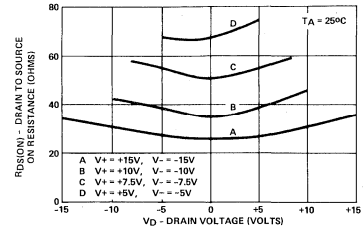


TYPICAL PERFORMANCE CURVES

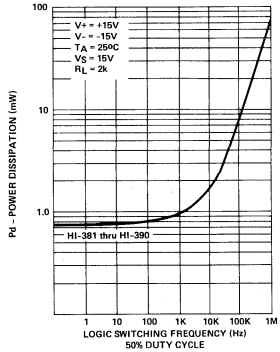
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



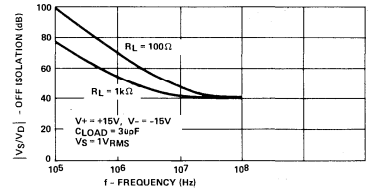
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



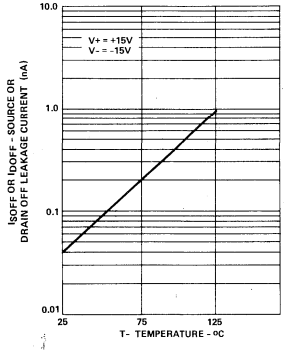
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



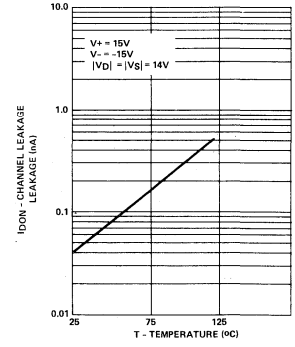
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE*

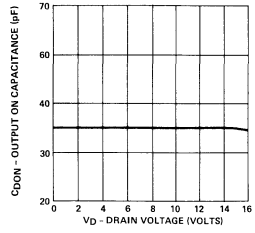


$I_{D(ON)}$ VS. TEMPERATURE*

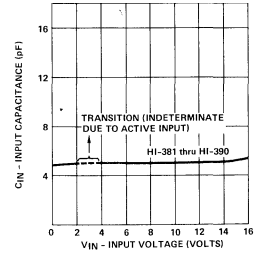


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE

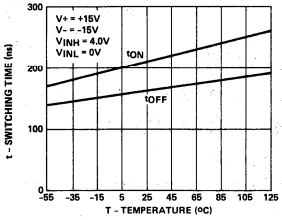


DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

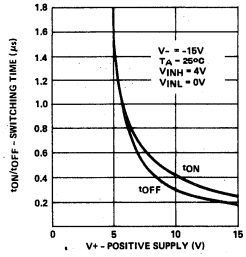


TYPICAL PERFORMANCE CURVES (Continued)

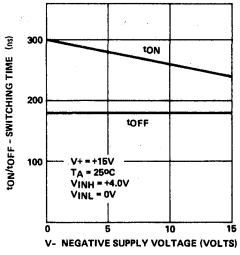
SWITCHING TIME VS. TEMPERATURE HI-381 thru HI-390



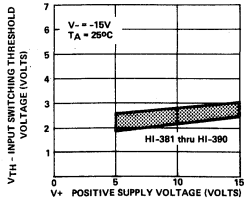
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390



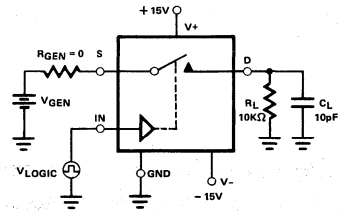
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-381 thru HI-390



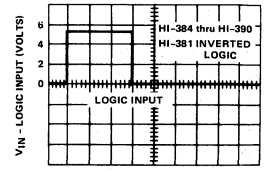
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390

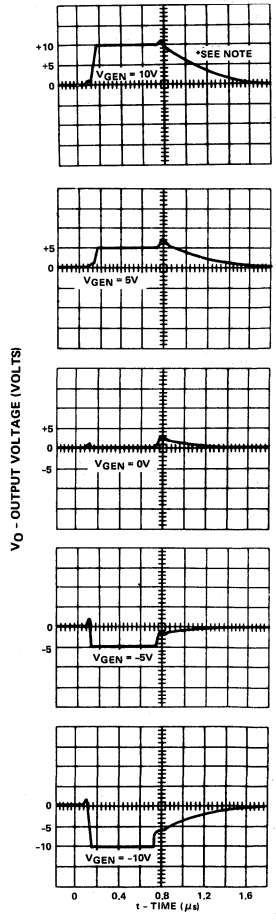


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.





* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

HI-5040 thru HI-5051
HI-5046A and
HI-5047A
CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

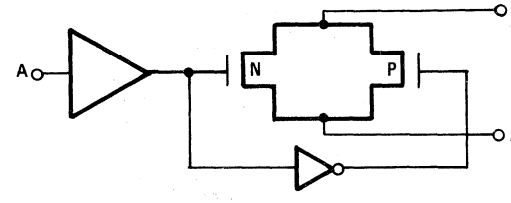
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog	$V^+ + 4V$	Operating Temperature	
Input Voltage	$V^- - 4V$	HI-50XX-2	-55^oC to $+125^oC$
		HI-50XX-5	0^oC to $+75^oC$
		Storage Temperature	-65^oC to $+150^oC$

*Derate 6mW/^oC above $T_A = 75^oC$

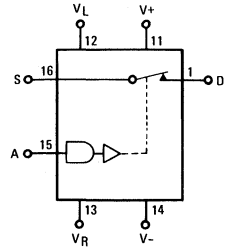
ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

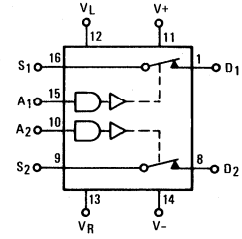
PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
$I_{S(OFF)}$ = $I_{D(OFF)}$, Off Input or Output	+25°C		0.8			0.8		nA
Leakage Current	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370	1000	ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280	500	ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+, +15V Quiescent Current	Full			0.3			0.5	mA
I^-, -15V Quiescent Current	Full			0.3			0.5	mA
I_L, +5V Quiescent Current	Full			0.3			0.5	mA
I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

NOTES: 1. $V_{OUT} = \pm 10V$, I_{OUT} = 1mA
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. $R_L = 100\Omega$, f= 100 KHz, V_{IN} = 2 V_{PP}, C_L = 5pF

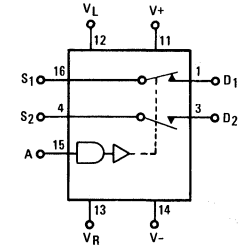
SPST
HI-5040 (75Ω)



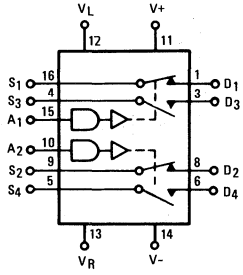
DUAL SPST
HI-5041 (75Ω)



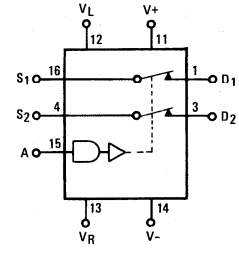
SPDT
HI-5042 (75Ω)



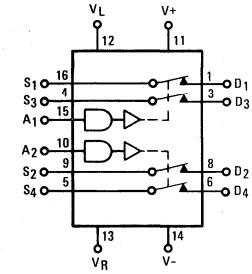
DUAL SPDT
HI-5043 (75Ω)



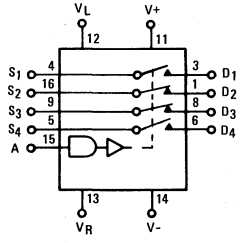
DPST
HI-5044 (75Ω)



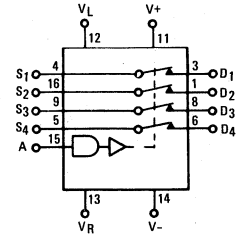
DUAL DPST
HI-5045 (75Ω)



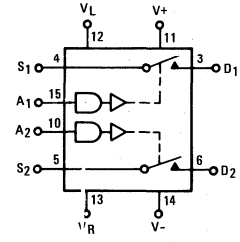
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



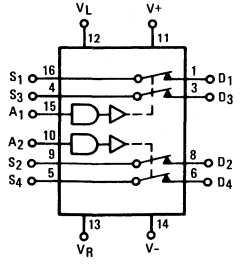
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



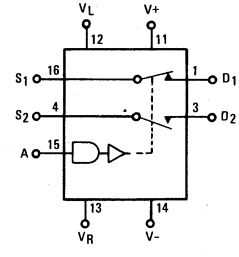
DUAL SPST
HI-5048 (30Ω)



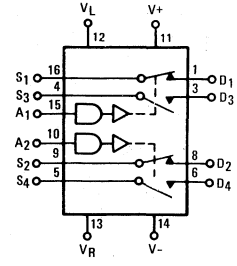
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)



DUAL SPDT
HI-5051 (30Ω)

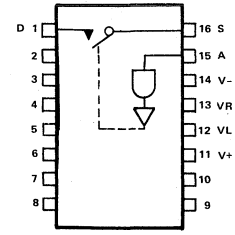


PIN CONFIGURATIONS

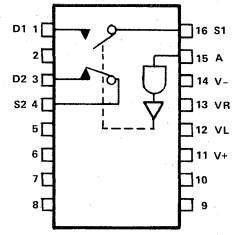
SWITCH STATES ARE FOR LOGIC "0" INPUT

SINGLE CONTROL

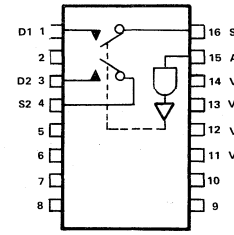
SPST
HI-5040 (75Ω)



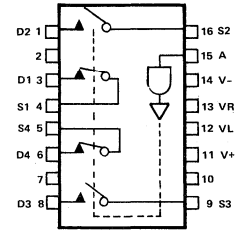
SPDT
HI-5042 (75Ω)
HI-5050 (25Ω)



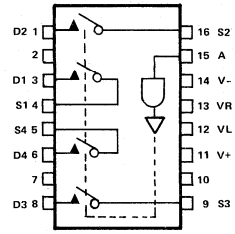
DPST
HI-5044 (75Ω)



DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)

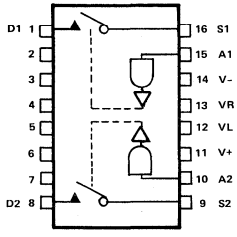


4 SPST
HI-5047 (75Ω)
HI-5047A (25Ω)

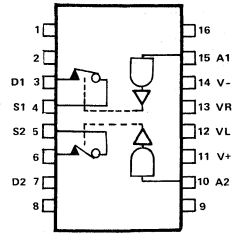


DUAL CONTROL

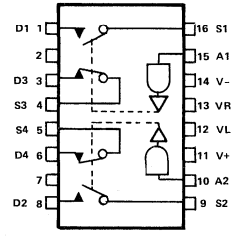
DUAL SPST
HI-5041 (75Ω)



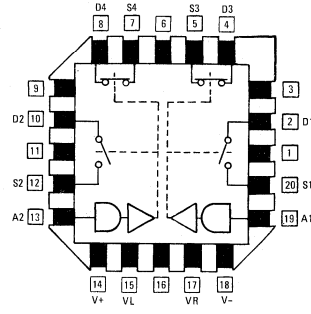
DUAL SPST
HI-5048 (25Ω)



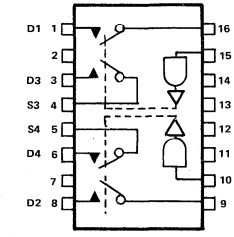
DUAL SPDT
HI-5043 (75Ω)
HI-5051 (25Ω)



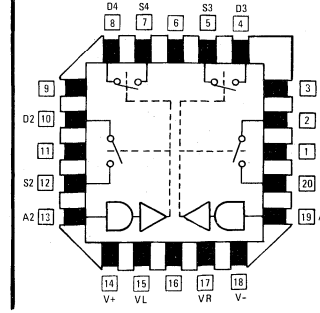
HI-5043 ONLY



DUAL DPST
HI-5045 (75Ω)
HI-5049 (25Ω)



HI-5045 ONLY

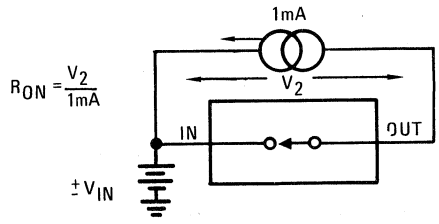


Note: Unused pins may be internally connected.

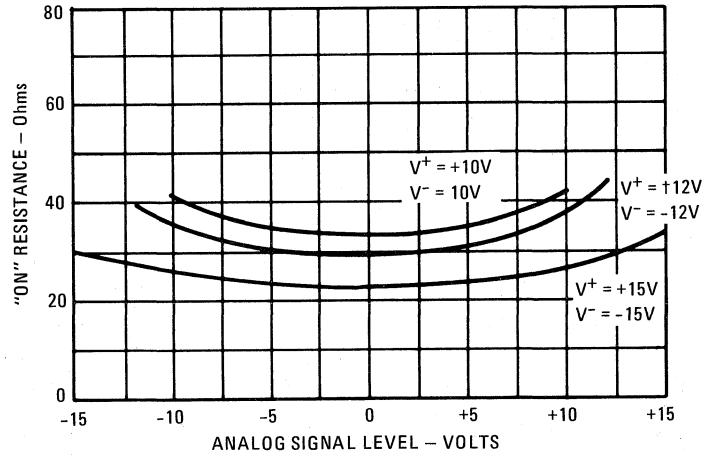
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

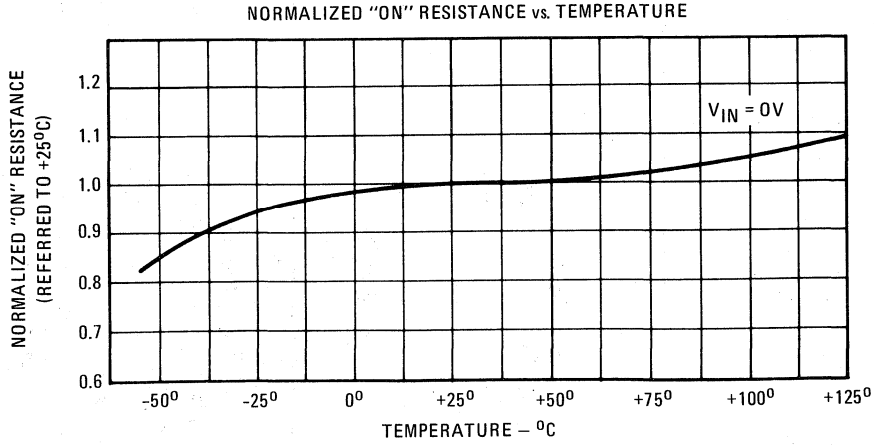
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



"ON"" RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

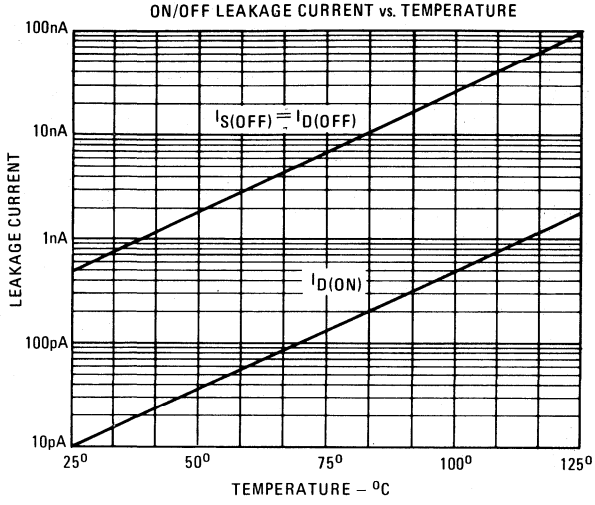


NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

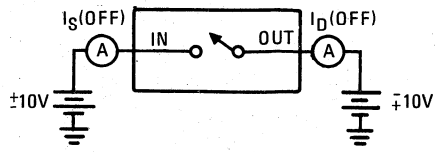


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

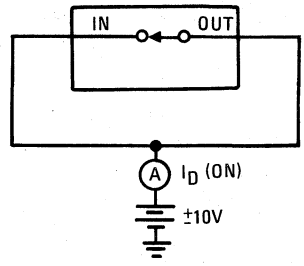
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



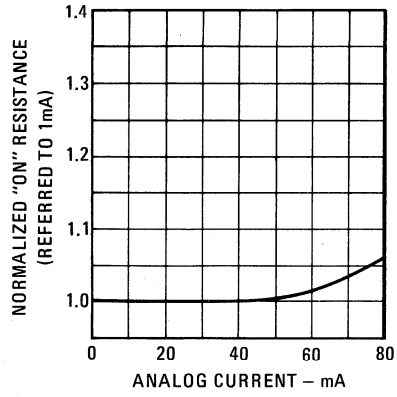
OFF LEAKAGE CURRENT vs. TEMPERATURE



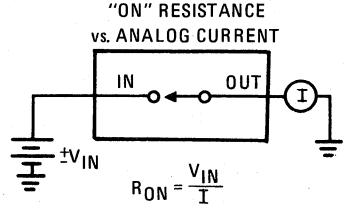
ON LEAKAGE CURRENT vs. TEMPERATURE



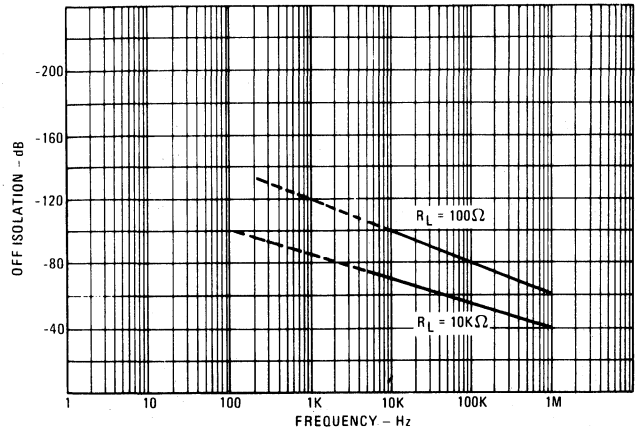
NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

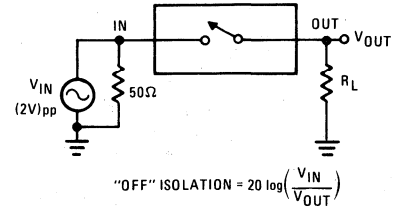


"ON" RESISTANCE vs. ANALOG CURRENT



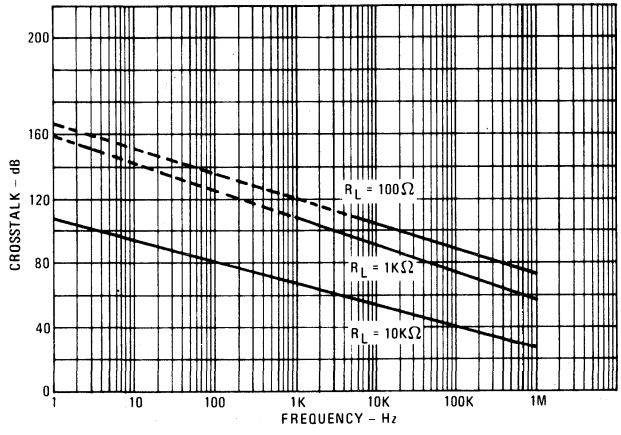
"OFF" ISOLATION vs. FREQUENCY

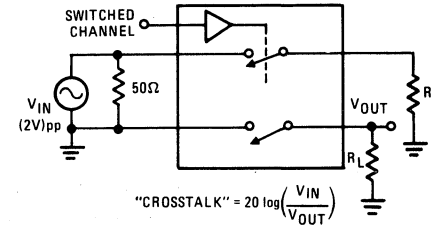




"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

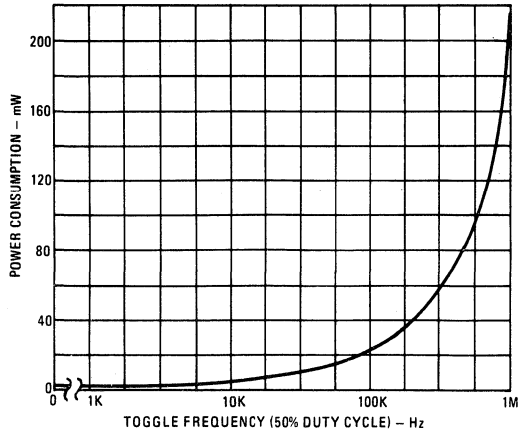
CROSSTALK vs. FREQUENCY

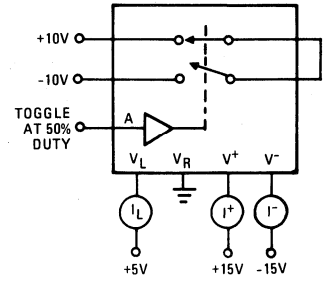




"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

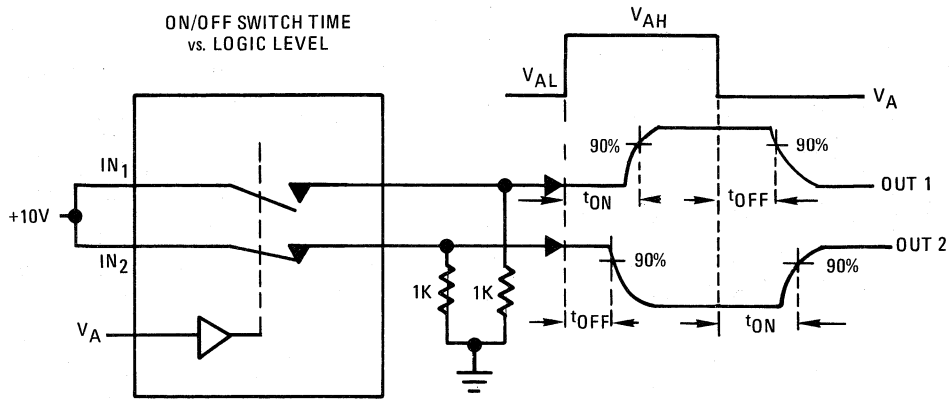
POWER CONSUMPTION vs. FREQUENCY

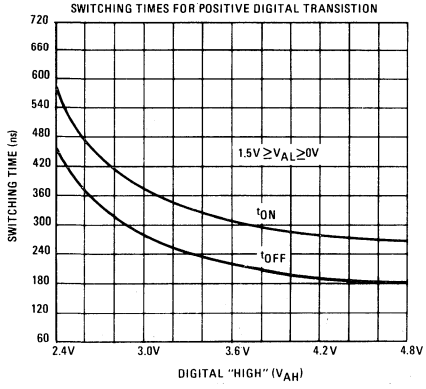


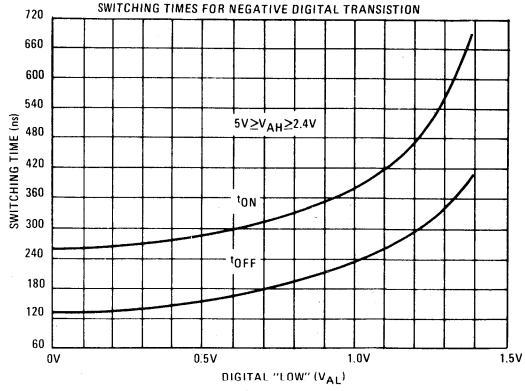


SWITCHING CHARACTERISTICS

ON/OFF SWITCH TIME
vs. LOGIC LEVEL

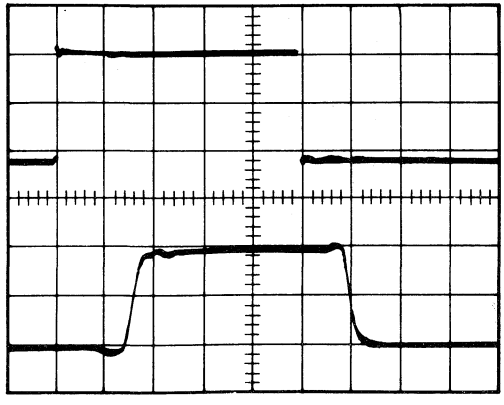






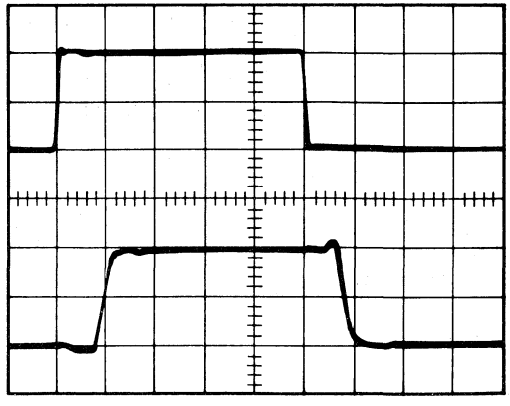
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

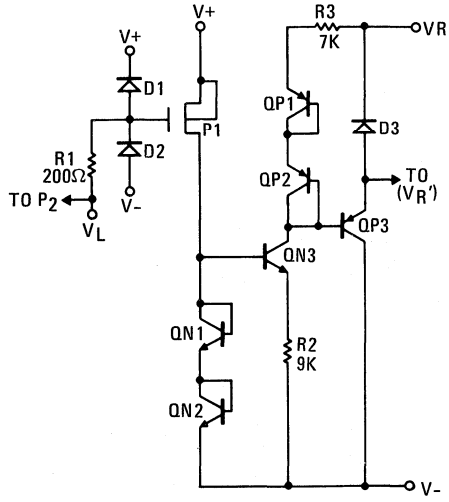
TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



200ns/DIV

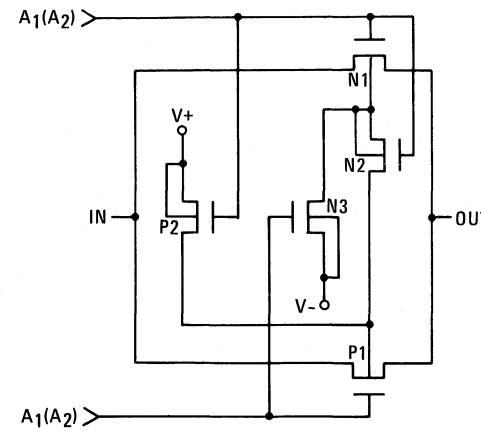
SCHEMATIC DIAGRAMS

TTL/CMOS REFERENCE CIRCUIT*

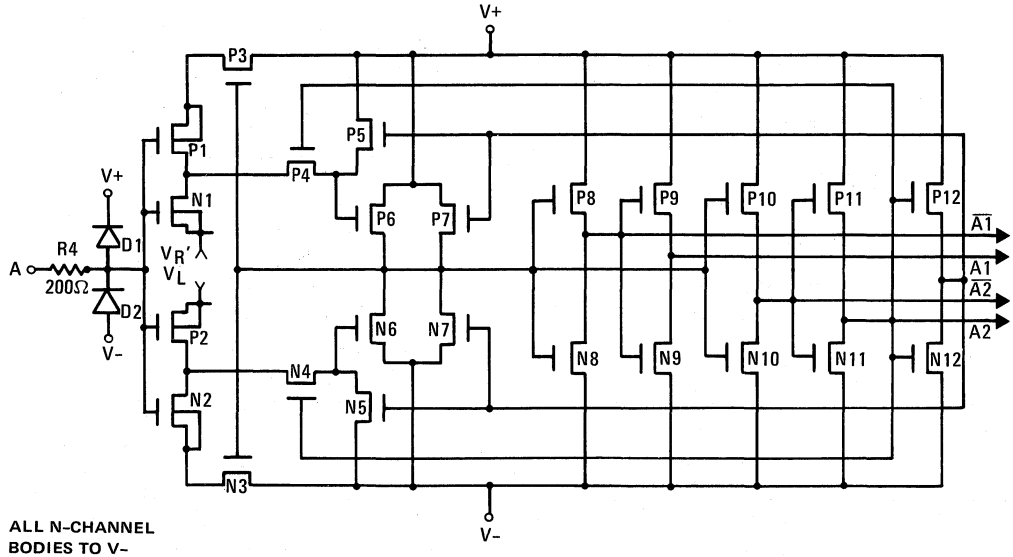


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN

ANALOG

Multiplexers

4

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Product Information 4-4

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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CMOS Multiplexers Selection Guide

FUNCTION	DEVICE	FEATURE	TTL "HIGH" MIN (V)	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$ (nA) (TYP)	$t_{(ON)}$ (ns) (TYP)	$t_{(OFF)}$ (ns) (TYP)	P_D(mW) (TYP)	PAGE
4-CHANNEL DIFFERENTIAL	HI-1828A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.05	350	250	5	4-70
	HI-508	LOW R_{ON}	2.4	180	0.3	210	180	23	4-24
	HI-509A	ANALOG INPUT OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	4-31
	HI-509L	ADDRESS LATCHES AND OVERVOLTAGE PROTECTION	2.0	1K	2.0	500	500	40	4-37
8-CHANNEL	HI-1818A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.1	350	250	5	4-70
	HI-509	LOW R_{ON}	2.4	180	0.3	210	180	23	4-24
	HI-508A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	4-31
	HI-508L	ADDRESS LATCHES AND OVERVOLTAGE PROTECTION	2.0	1K	4.0	500	500	40	4-37
8-CHANNEL DIFFERENTIAL	HI-507	LOW R_{ON}	2.4	170	1.0	300	300	30	4-3
	HI-507A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	4-9
	HI-507L	ADDRESS LATCHES AND OVERVOLTAGE PROTECTION	2.0	1K	4.0	500	500	60	4-15
16 CHANNEL	HI-506	LOW R_{ON}	2.4	170	1.0	300	300	30	4-3
	HI-506A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	4-9
	HI-506L	ADDRESS LATCHES AND OVERVOLTAGE PROTECTION	2.0	1K	8.0	500	500	60	4-15
8-CHANNEL 4-CHANNEL	HI-518	HIGH SPEED LOW LEAKAGE	2.4	480	0.1	80	60	360	4-51
16-CHANNEL 8 DIFFERENTIAL	HI-516	HIGH SPEED LOW LEAKAGE	2.4	620	0.035	100	80	525	4-46
4-CHANNEL	HI-524	VIDEO BANDWIDTH	2.4	700	0.2	180	180	540	4-56
4-CHANNEL DIFFERENTIAL	HI-539	LOW LEVEL SIGNALS	4.0	650 ΔR_{ON} = 4 Ω	0.03 $\Delta I_{D(OFF)}$ = .003	250	160	2.5	4-61

NOTE: All data typical room temperature specifications at ±15V supplies. For guaranteed and tested specifications consult the device data sheet.

HARRIS

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

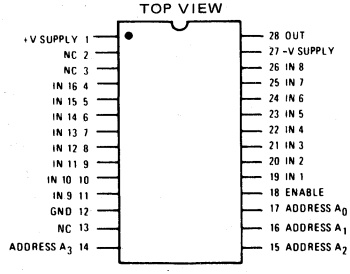
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. Each device is packaged in a 28 pin DIP. The recommended supply voltage is ±15V, and reasonable performance is available down to ±7V; however, a power-up reset routine may be required for operation below ±10V. For more information, request Harris Analog Tech Brief # 20.

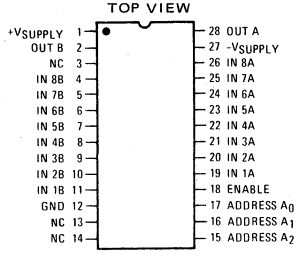
The HI-506/507 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUT

HI-506

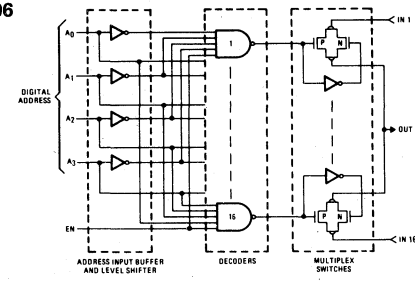


HI-507

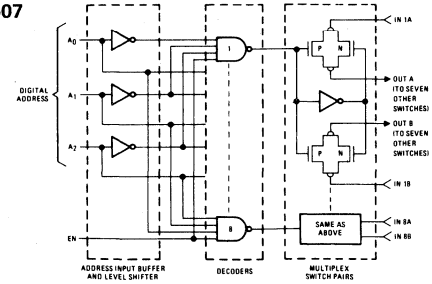


FUNCTIONAL DIAGRAM

HI-506



HI-507



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 44V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* 1200 mW

Operating Temperature:

HI-506/HI-507-2 -55°C to +125°C

HI-506/HI-507-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 19.7mW/°C above T_A = 110°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506/HI-507-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506/HI-507-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
*ΔR_{ON}, (Between Channels)	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current	+25°C		0.3			0.3		nA
HI-506	Full			±300			±300	nA
HI-507	Full			±200			±200	nA
*I_D (ON), On Channel Leakage Current	+25°C		0.3			0.3		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			±50			±50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
*I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OPEN}, Break-Before Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		4			4		pF
C_D (OFF), Channel Output Capacitance HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
*I+, Current Pin 1 (Note 4)	Full		1.7	3.0		1.7	3.0	mA
*I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.4	1.0	mA
*I+, Standby (Note 5)	Full		1.7	3.0		1.7	3.0	mA
*I-, Standby (Note 5)	Full		0.4	1.0		0.4	1.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

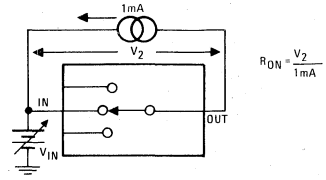
A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

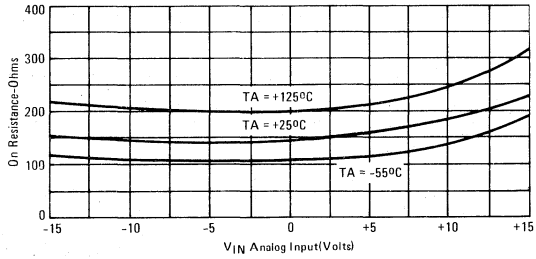
Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

TEST CIRCUIT NO. 1

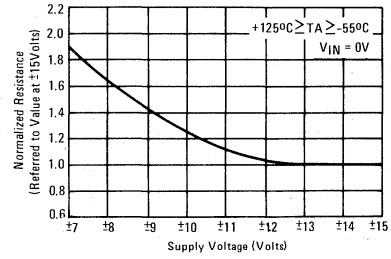
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



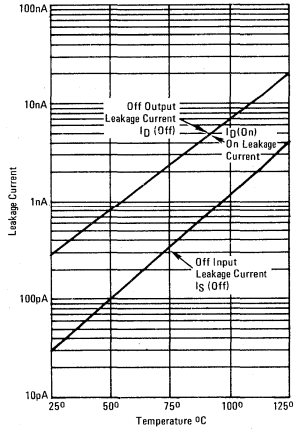
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



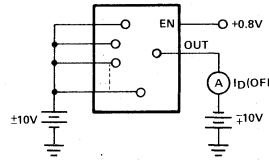
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



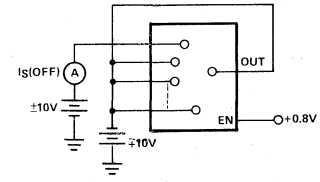
LEAKAGE CURRENT VS. TEMPERATURE



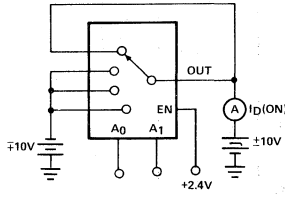
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

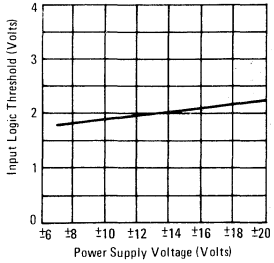


TEST CIRCUIT NO. 4*

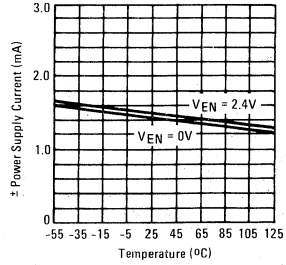


***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)**

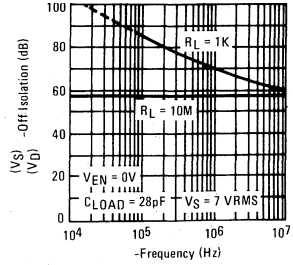
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

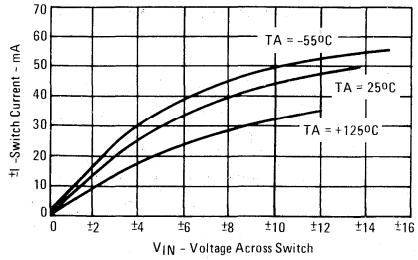


OFF ISOLATION vs. FREQUENCY

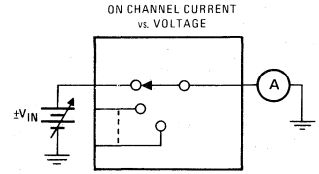


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

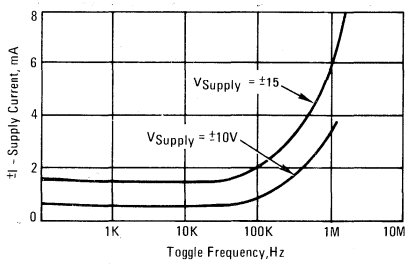
ON CHANNEL CURRENT vs. VOLTAGE



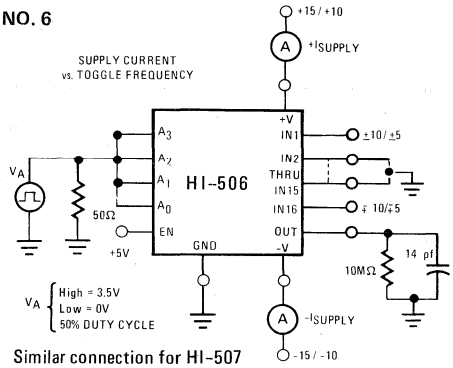
TEST CIRCUIT NO. 5



SUPPLY CURRENT vs. TOGGLE FREQUENCY

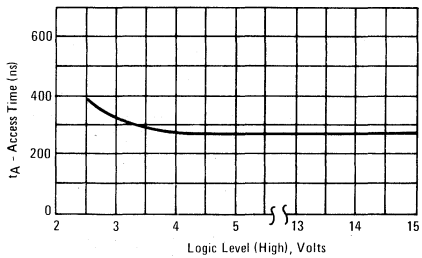


TEST CIRCUIT NO. 6

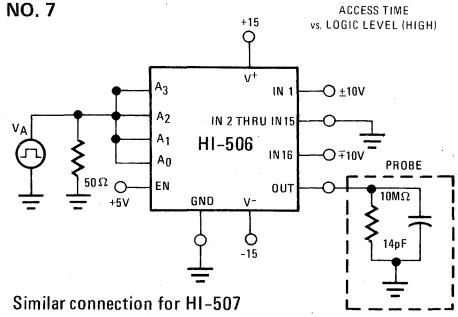


Similar connection for HI-507

ACCESS TIME vs. LOGIC LEVEL (HIGH)

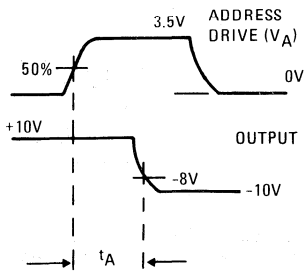


TEST CIRCUIT NO. 7

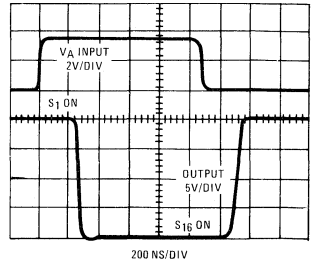


Similar connection for HI-507

SWITCHING WAVEFORMS

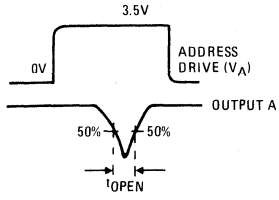


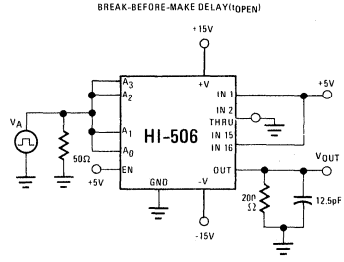
ACCESS TIME



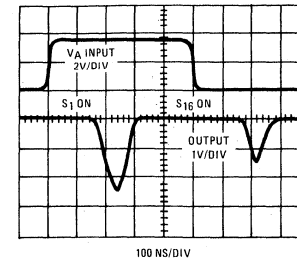
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT NO. 8



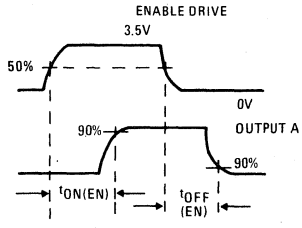


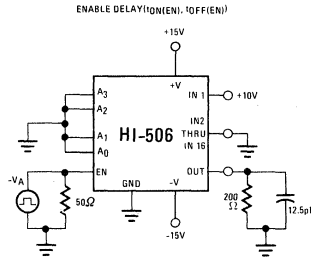
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



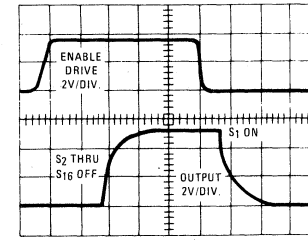
Similar connection for HI-507

TEST CIRCUIT NO. 9





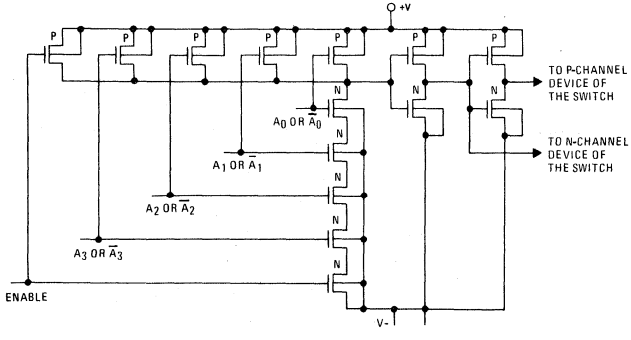
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



Similar connection for HI-507

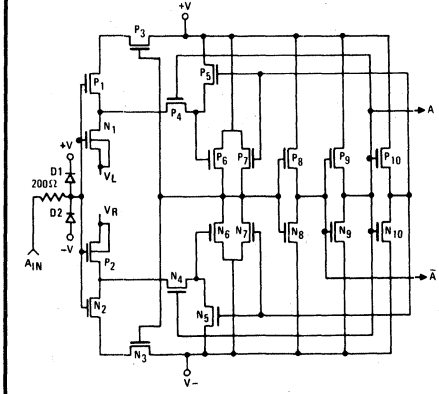
SCHEMATIC DIAGRAMS

ADDRESS DECODER



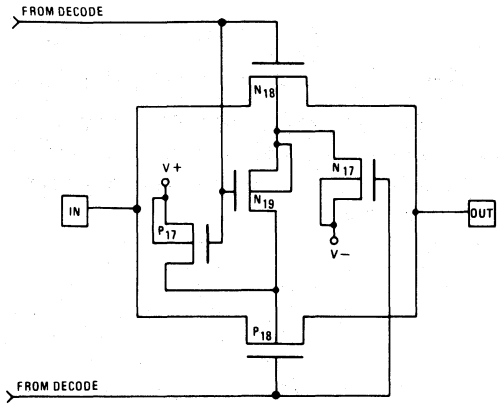
Delete A_3 or $\overline{A_3}$ Input for HI-507

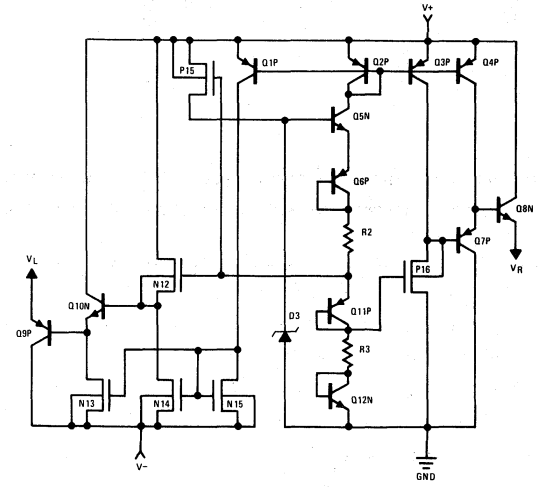
ADDRESS INPUT BUFFER LEVER SHIFTER



All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

SCHEMATIC DIAGRAM (Continued)





DIE CHARACTERISTICS

Transistor Count		421
Die Size		110 x 83 mils
Thermal Constants	θ_{ja}	51°C/W
	θ_{jc}	20°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

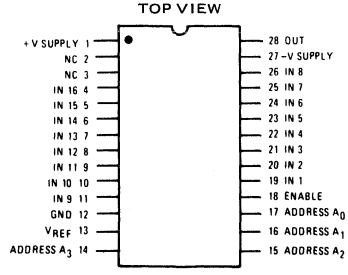
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A/507A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUT

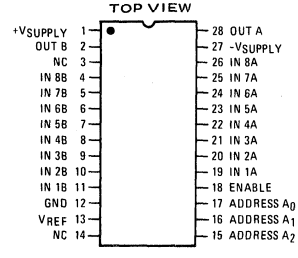
HI-506A

TOP VIEW



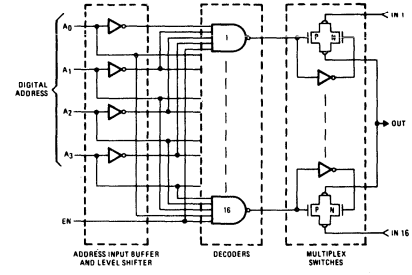
HI-507A

TOP VIEW

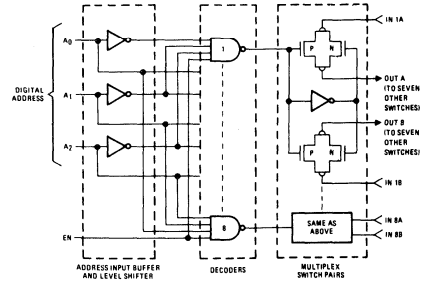


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	44V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	22V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A { V_{Supply} (+)	+4V	HI-506A/507A-5	0°C to +75°C
V_A { V_{Supply} (–)	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S { V_{Supply} (+)	+20V		
V_S { V_{Supply} (–)	-20V	*Derate 19.7mW/°C above T_A = 110°C.	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±300			±300	nA
HI-507A	Full			±200			±200	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±300			±300	nA
HI-507A	Full			±200			±200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			±50			±50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold { TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold { (Note 7)	Full	4.0			4.0			V
V_{AL} { MOS Drive (Note 3)	+25°C			0.8			0.8	V
V_{AH} {	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
t_{OPEN}, Break-Before Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.3			1.3		μs
(0.025%)	+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	2.0	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	1.0	mA
*I+, Standby (Note 6)	Full		0.5	2.0		0.5	2.0	mA
*I-, Standby (Note 6)	Full		0.02	1.0		0.02	1.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L =15pF, V_S = 7VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩpull-up resistors to +5.0V supply are recommended.

*100% tested for Dash 8 at +25°C and +125°C only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

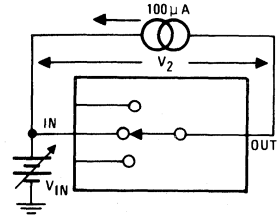
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^0C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

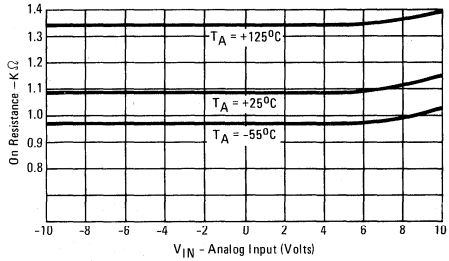
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

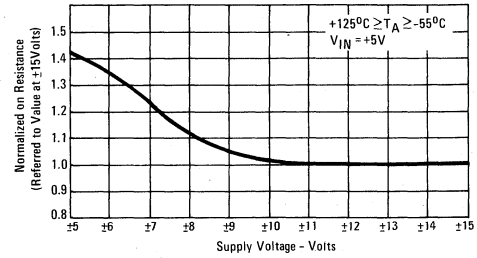
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



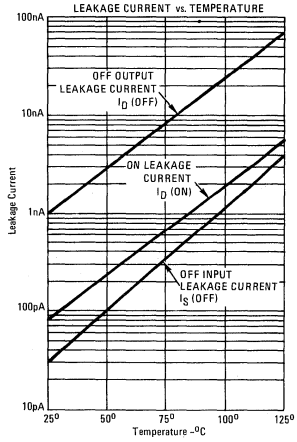
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



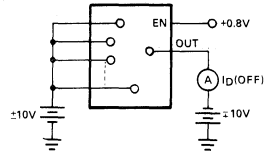
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



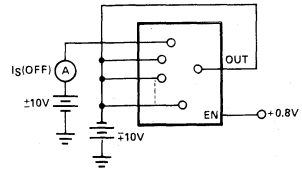
LEAKAGE CURRENT vs. TEMPERATURE



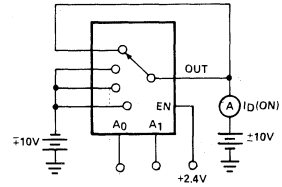
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

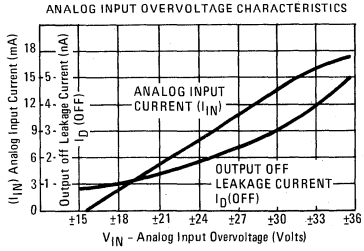


TEST CIRCUIT NO. 4*



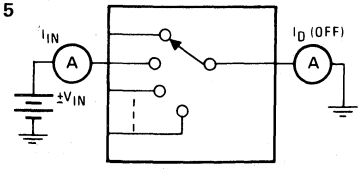
***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

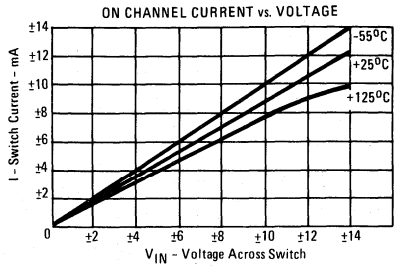


TEST CIRCUIT NO. 5

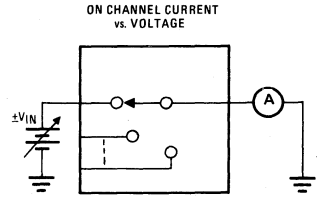
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

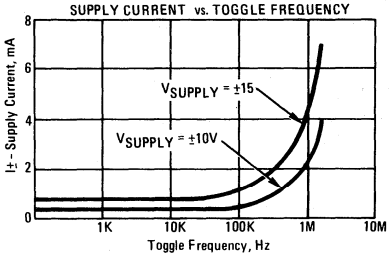


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

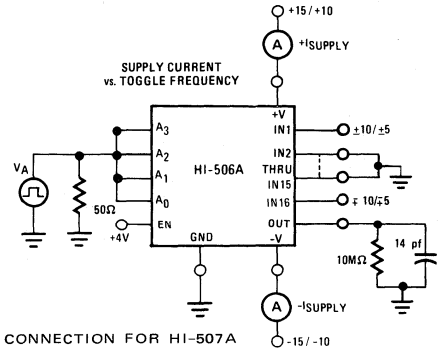


TEST CIRCUIT NO. 6

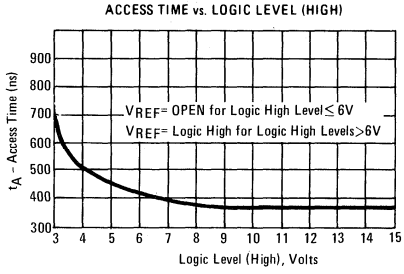




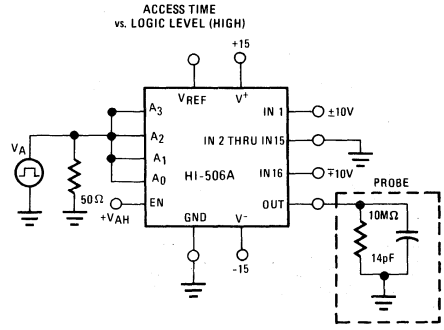
TEST CIRCUIT NO. 7



SIMILAR CONNECTION FOR HI-507A

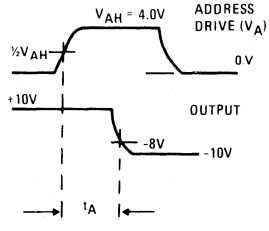


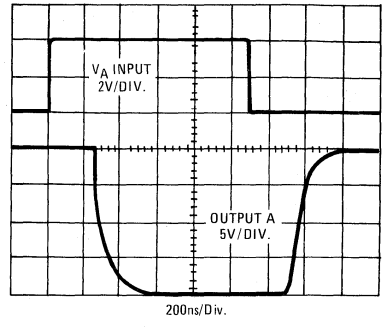
TEST CIRCUIT NO. 8



SIMILAR CONNECTION FOR HI-507A

SWITCHING WAVEFORMS

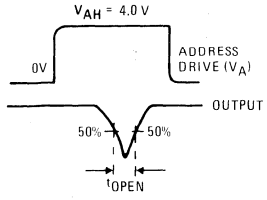


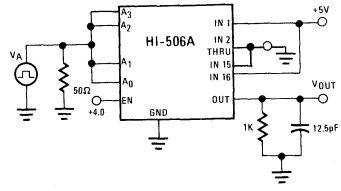


SWITCHING WAVEFORMS (continued)

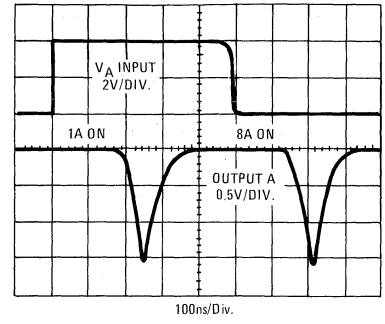
TEST CIRCUIT NO. 9

BREAK BEFORE MAKE DELAY (t_{OPEN})





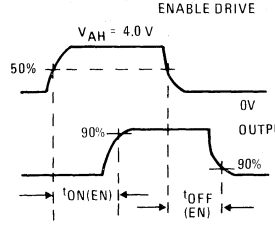
BREAK BEFORE MAKE DELAY (t_{OPEN})

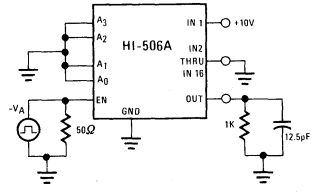


SIMILAR CONNECTION FOR HI-507A

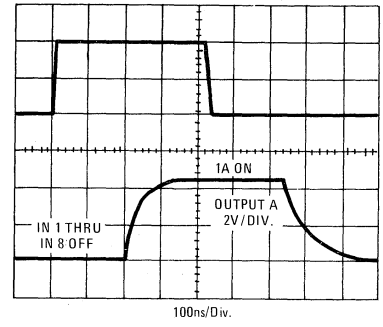
TEST CIRCUIT NO. 10

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

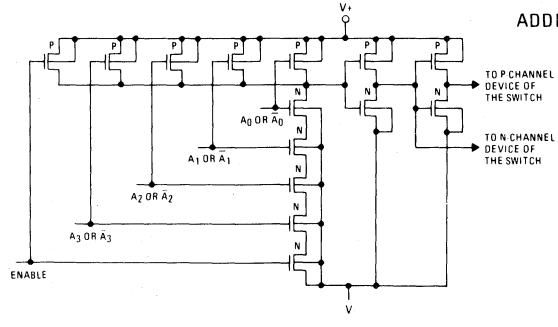


SIMILAR CONNECTION FOR HI-507A

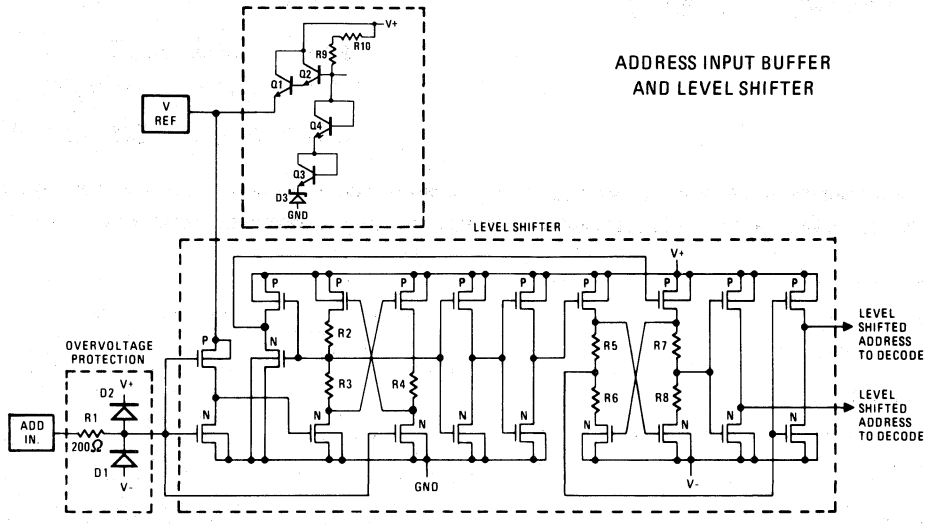
SCHEMATIC DIAGRAMS

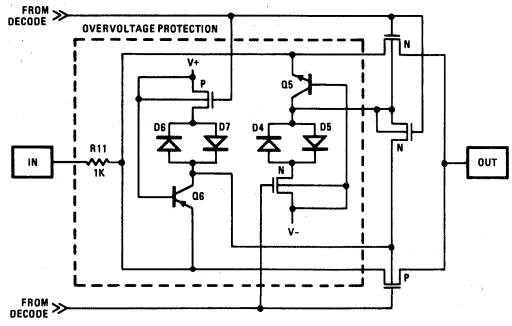
DELETE A_3 or $\overline{A}_3$ INPUT FOR HI-507A

ADDRESS DECODER



SCHEMATIC DIAGRAMS (continued)





DIE CHARACTERISTICS

Transistor Count		485
Die Size		161 x 85 mils
Thermal Constants	θ_{ja}	50°C/W
	θ_{jc}	18°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HARRIS

HI-506L/HI-507L

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Latches And Overvoltage Protection

FEATURES

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq$ 8nA (typ) over full temp range
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

DESCRIPTION

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each model includes digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write ($\overline{WR}$) and Reset ($\overline{RS}$) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output must present a high impedance when power is off. This is achieved by a switch cell with three MOSFET's in series, rather than the conventional transmission gate design.

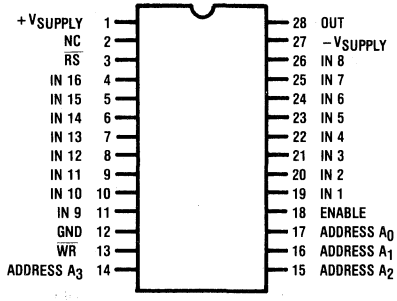
Each channel can withstand overvoltage to ±25VDC with respect to ground with power ON or OFF. An OFF channel remains OFF in the presence of overvoltage. If the channel is ON, output voltage is clamped below the supply rail, which protects the load circuit.

The HI-506L offers 16 single-ended channels, and the HI-507L is an 8 channel differential version. The recommended supply voltages are ±15V, though operation at reduced levels or with a single supply may also be implemented. The package is a 28 pin ceramic or plastic DIP.

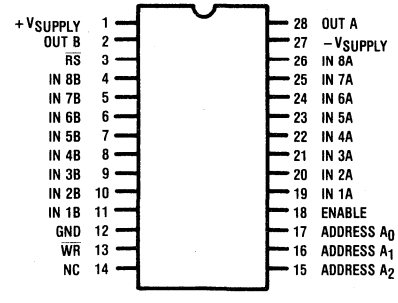
Each product is specified for the commercial temperature range (0°C to +75°C, −5 suffix) and the military range (−55°C to +125°C, −2 suffix). Military high reliability burned-in product is available as a "−8" suffix.

PINOUT

HI-506L

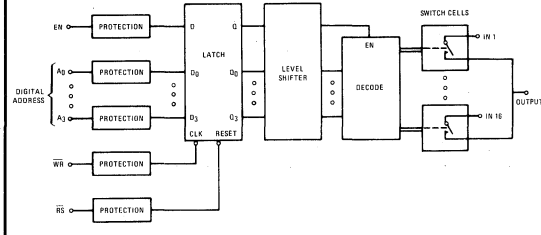


HI-507L

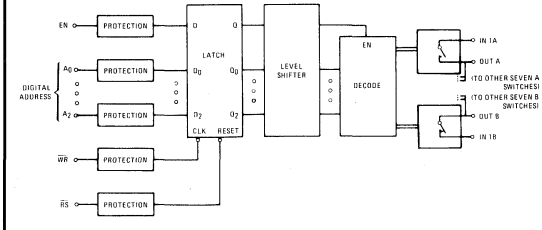


FUNCTIONAL DIAGRAM

HI-506L



HI-507L



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note1)

Supply Voltage Between Pins 1 and 27	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$;			
V supply (+)	+4V	HI-506L/507L-2	−55°C to 125°C
V supply (−)	−4V	HI-506L/507L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

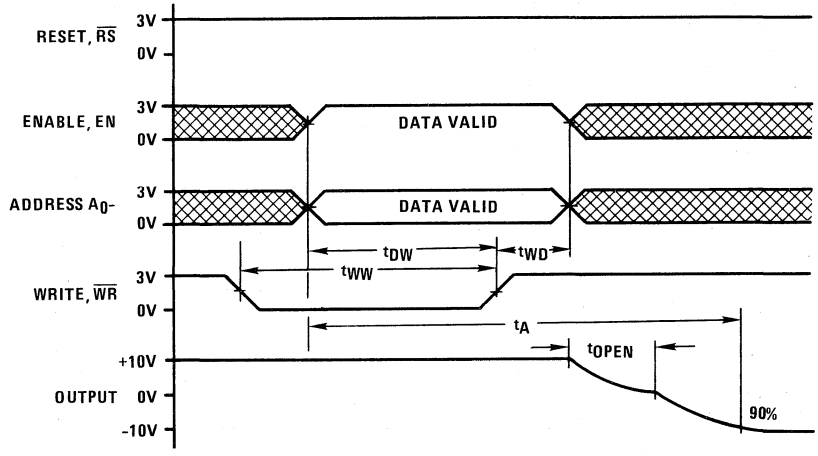
	HI-506L/507L-2 −55°C to +125°C				HI-506L/507L-5 0°C to +75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note 2)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
$\triangle R_{ON}$, Change In R_{ON} (Note 3) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		5	50		5	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-506L	Full		8	200		8	200	nA
HI-507L	Full		4	100		4	100	nA
$I_{D(On)}$, ON Channel leakage current	+25°C		5	10		5	10	nA
HI-506L	Full		10	200		10	200	nA
HI-507L	Full		5	100		5	100	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 4)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-	+25°C		5			5		nA
voltage applied (Note 4)	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current (Note 5)	Full		10	40		10	40	μA
I_{AL}, Input Low Current (Note 5)	Full		40	200		40	200	μA
DYNAMIC SWITCHING CHARACTERISTICS (Note 6)								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	μS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		.025	0.1		μS
t_{ON}, (EN), Enable Delay (ON)	+25°C		0.5	1.0		0.5	1.0	μS
t_{OFF}, (EN), Enable	+25°C		0.5	1.0		0.5	1.0	μS
Delay (OFF)								
Settling Time (±0.1%)	+25°C		1.0			1.0		μS
(±0.01%)	+25°C		1.75			1.75		μS
OFF Isolation (Note 7)	+25°C	50	68		50	68		dB
OFF Isolation POWER OFF (Note 8)	+25°C		56			56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-506L	+25°C		50			50		pF
HI-507L	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 9)	Full		60	100		60	100	mW
I +, Current Pin 1 (Note 9)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 27 (Note 9)	Full		0.3	0.6		0.3	0.6	mA

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, I out = -100μa
3. $\Delta R_{ON} = \frac{R_{ON}(Max) - R_{ON}(Min)}{R_{ON}(Avg.)}$, $V_{IN} = \pm 10V$
4. Analog Overvoltage = ±25V
5. I_{AH} and I_{AL} tested at 2.4V and 0.4 V respectively
6. For measurements irf this section, input logic levels are 3.0V (High) and 0V (Low).
7. V_{EN} = 0.8V, R_L = 1KΩ, C_L = 15pF, V_S = 7Vrms, f = 500kHz
Off isolation = 20 log $\frac{|V_D|}{|V_S|}$
8. V+ , V- = 0V, R_L = 1KΩ , C_L = 50pF, V_S = 3Vrms, f = 500 kHz.
9. See Test Circuit #8 for high toggle frequency applications.

MINIMUM TIMING REQUIREMENTS

PARAMETER	MIN LIMITS FULL TEMP RANGE	UNITS
t_{WW}, Write Pulse Width	300	nS
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	225	nS
t_{WD}, A, EN Data Valid After Write (hold Time)	100	nS
t_{RS}, RESET pulse width	400	nS
t_{OFF} ($\overline{RS}$) Reset Delay	1000	nS
t_{ON} ($\overline{WR}$) Write Turn-on Time	1000	nS

TIMING REQUIREMENTS



1. $+V_{SUPPLY}$ = +15V; $-V_{SUPPLY}$ = -15V.
2. Logic Levels: V_{AL} = 0V; V_{AH} = +3.0V.
3. Time intervals are measured between 50% levels unless otherwise noted.
4. Minimum values for $t_{\overline{RS}}$, t_{DW}, t_{WW} and t_{WD} are guaranteed separately but not simultaneously.

Figure 1

SCHEMATIC DIAGRAM

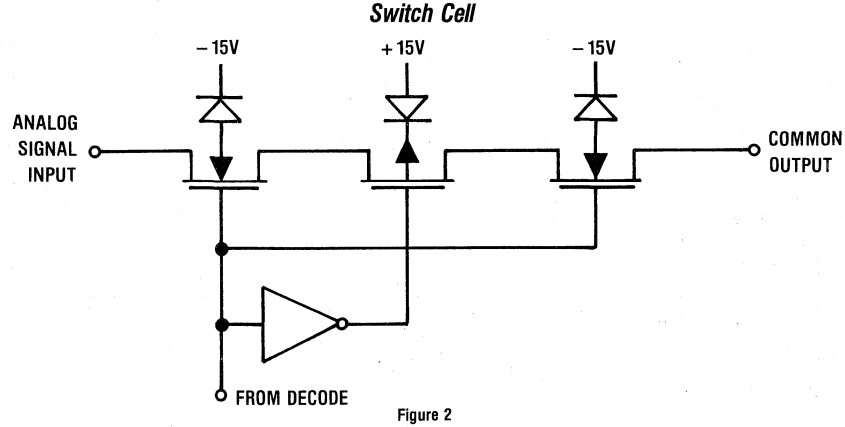


Figure 2

TRUTH TABLES

506L

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL
X	X	X	X	L	L	H	None
X	X	X	X	X	↓	H	Previous ON Channel.
X	X	X	X	X	X	L	None (latches cleared)
L	L	L	L	H	L	H	Channel 1
L	L	L	H	H	L	H	Channel 2
L	L	H	L	H	L	H	Channel 3
L	L	H	H	H	L	H	Channel 4
L	H	L	L	H	L	H	Channel 5
L	H	L	H	H	L	H	Channel 6
L	H	H	L	H	L	H	Channel 7
L	H	H	H	H	L	H	Channel 8
H	L	L	L	H	L	H	Channel 9
H	L	L	H	H	L	H	Channel 10
H	L	H	L	H	L	H	Channel 11
H	L	H	H	H	L	H	Channel 12
H	H	L	L	H	L	H	Channel 13
H	H	L	H	H	L	H	Channel 14
H	H	H	L	H	L	H	Channel 15
H	H	H	H	H	L	H	Channel 16

507L

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL PAIR
X	X	X	L	L	H	None
X	X	X	X	↓	H	Previous ON Channel.
X	X	X	X	X	L	None (latches cleared)
L	L	L	H	L	H	Channel 1A and 1B
L	L	H	H	L	H	Channel 2A and 2B
L	H	L	H	L	H	Channel 3A and 3B
L	H	H	H	L	H	Channel 4A and 4B
H	L	L	H	L	H	Channel 5A and 5B
H	L	H	H	L	H	Channel 6A and 6B
H	H	L	H	L	H	Channel 7A and 7B
H	H	H	H	L	H	Channel 8A and 8B

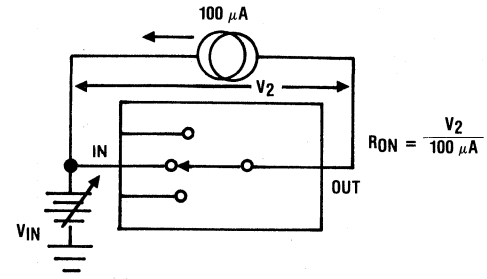
DESCRIPTION AND APPLICATION

The switch cell of the HI-506L/507L has a different structure than earlier Harris designs (HI-506, HI506A). The new switch (Figure 2) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the transmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers higher Off Isolation with power off, and better fault performance. Channel overvoltage protection is inherent since one of the three MOSFETs turn off in the presence of overvoltage. this turn-off process begins well below the supply rail so the V_{IN} range is less than the power supply range. Electrical performance is guaranteed to ±10V for each channel, and the usable range extends above ±11 Volts.

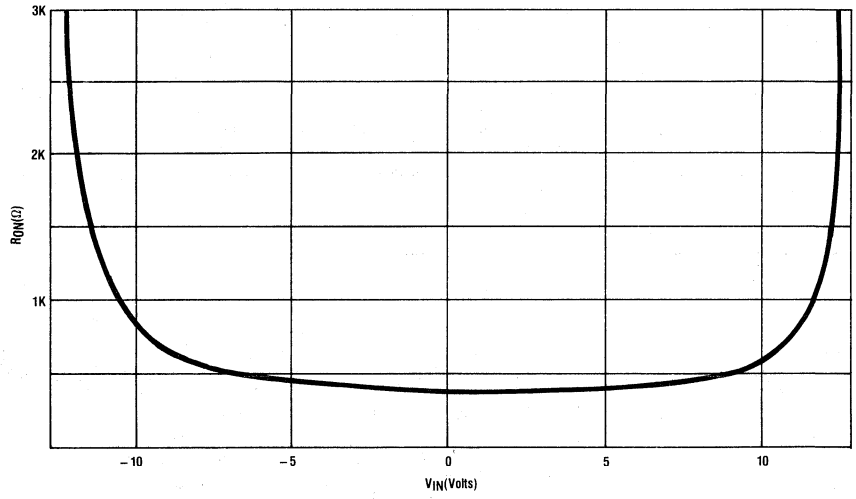
The address inputs A_0, A_1, A_2, A_3, and ENABLE are latched into an internal buffer when $\overline{WR}$ goes high. Each latch output is level shifted into the decode section, which activates the appropriate channel. The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system RESET line, to assure that all channels are OFF following a turn-on of power. The reset function overrides all others, just as $\overline{WR}$ overrides the address inputs (A_0-A_3 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e. the latches are "transparent". Refer to Figure 1.

TEST CIRCUIT NO. 1

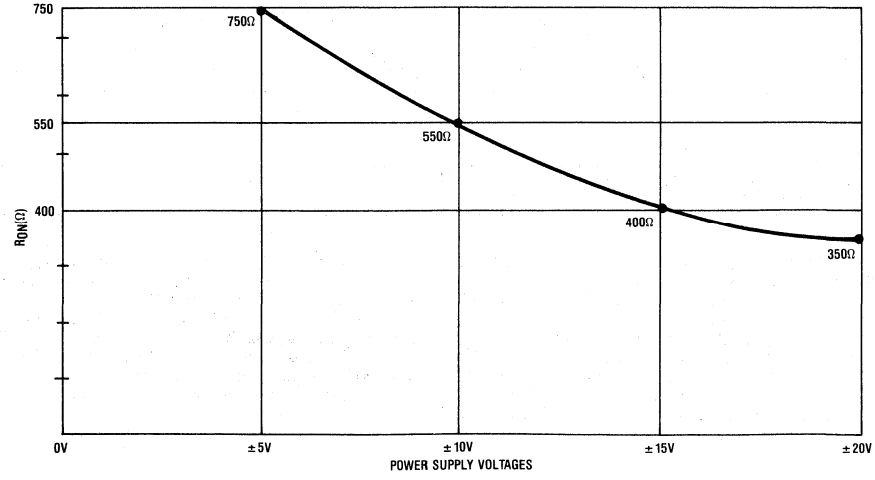
ON RESISTANCE vs.
INPUT SIGNAL LEVEL



VIN vs. RON

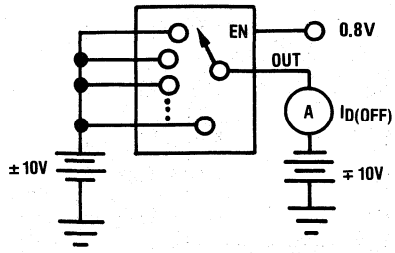


RON vs. POWER SUPPLY VOLTAGES
INPUT = 0V

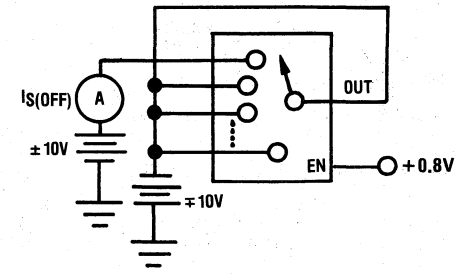


HI-506L TEST CIRCUITS

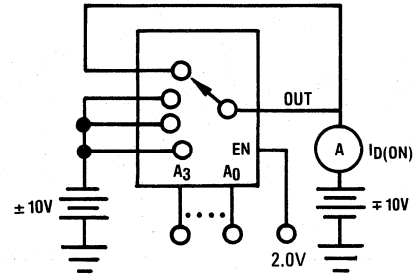
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*



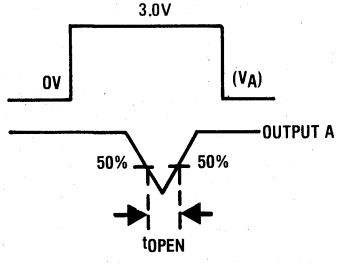
TEST CIRCUIT NO. 4*



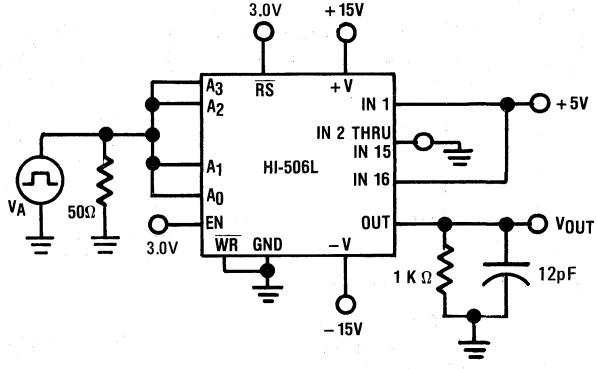
*Two measurements per channel: +10V/−10V and −10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/−10V and −10V/+10V.)

TEST CIRCUIT NO. 5

ADDRESS DRIVE

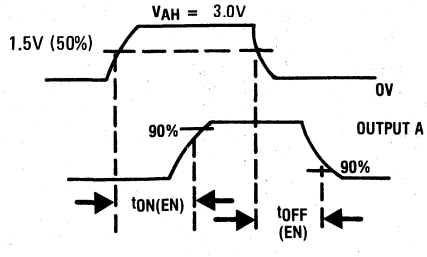


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

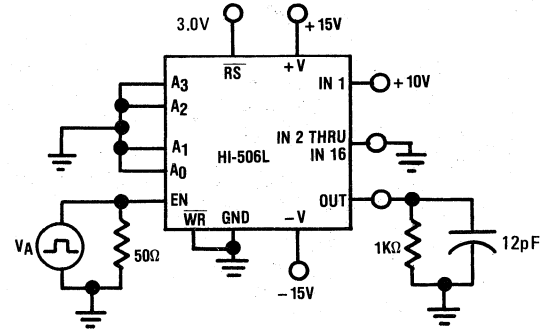


TEST CIRCUIT NO. 6

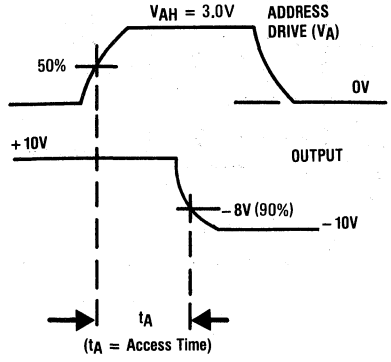
ENABLE DRIVE



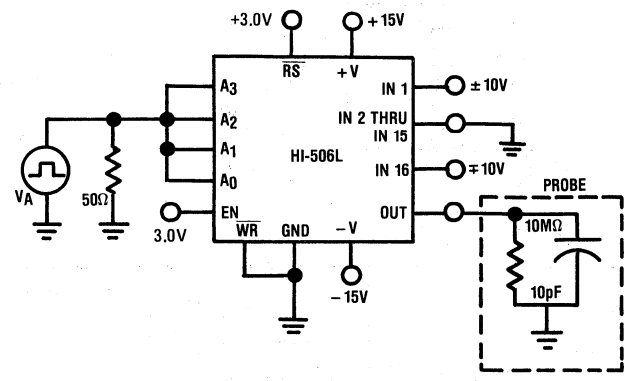
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



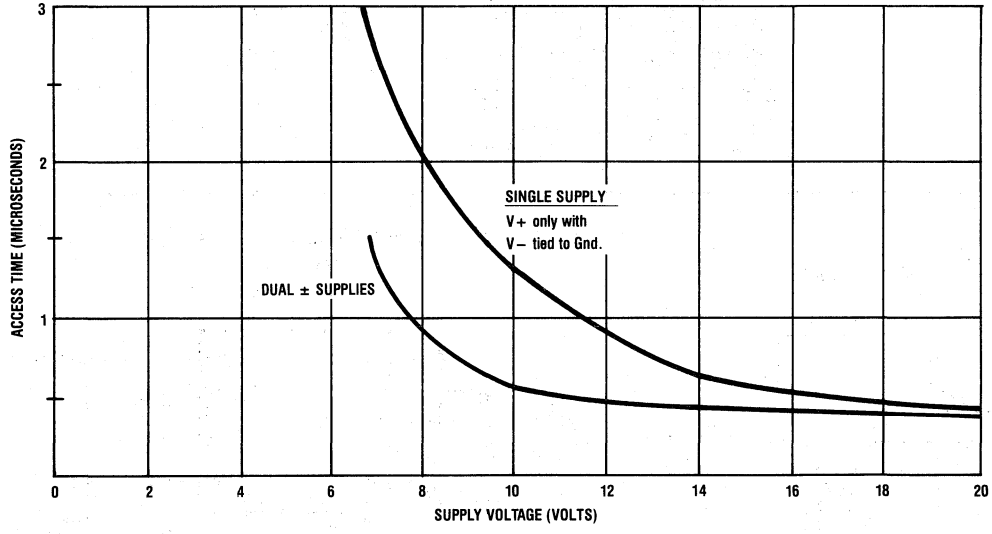
TEST CIRCUIT NO. 7



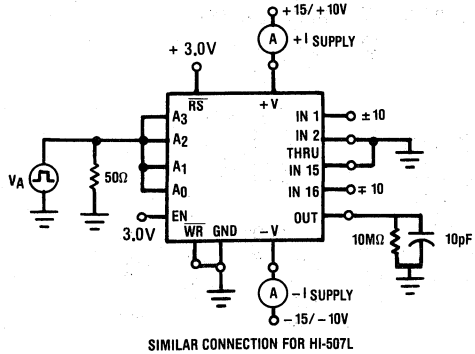
ACCESS TIME



ACCESS TIME vs. SUPPLY VOLTAGE

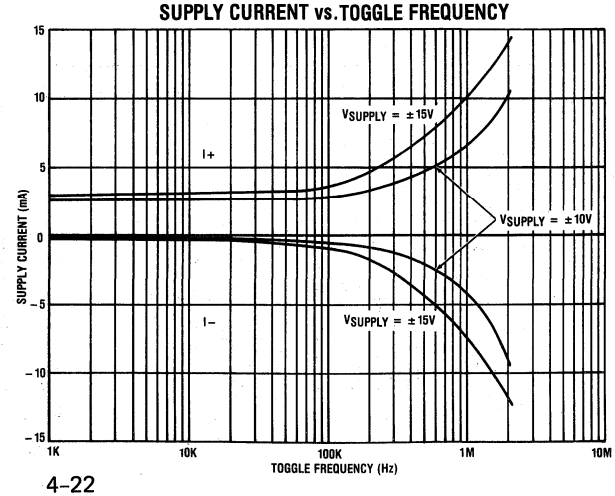


TEST CIRCUIT NO. 8
SUPPLY CURRENTS vs. TOGGLE FREQUENCY

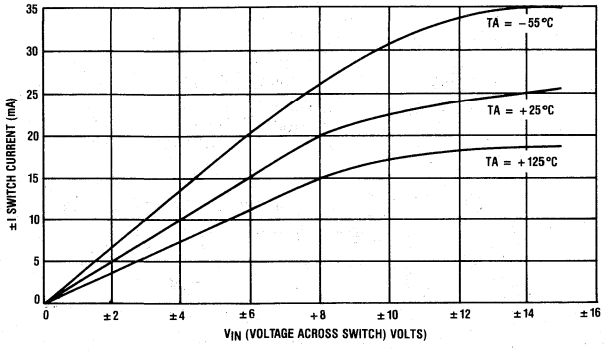


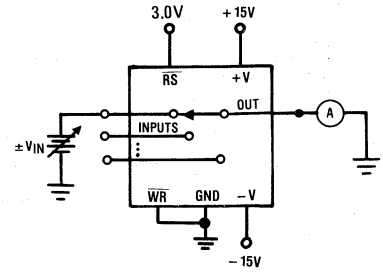
SIMILAR CONNECTION FOR HI-507L

SUPPLY CURRENT vs. TOGGLE FREQUENCY

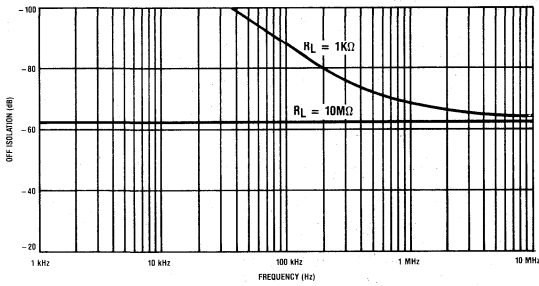


TEST CIRCUIT NO. 9
ON CHANNEL CURRENT vs. INPUT VOLTAGE

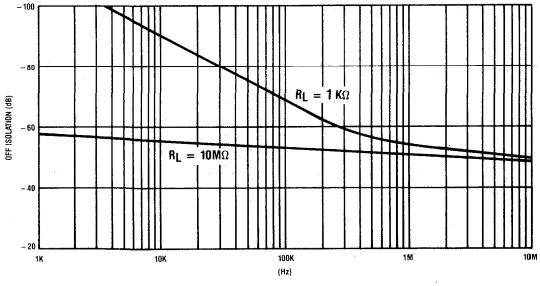




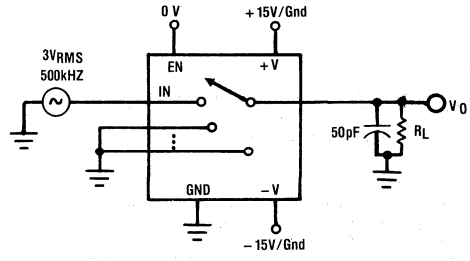
OFF ISOLATION vs. FREQUENCY POWER ON



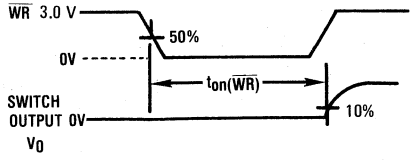
OFF ISOLATION vs. FREQUENCY (POWER OFF)



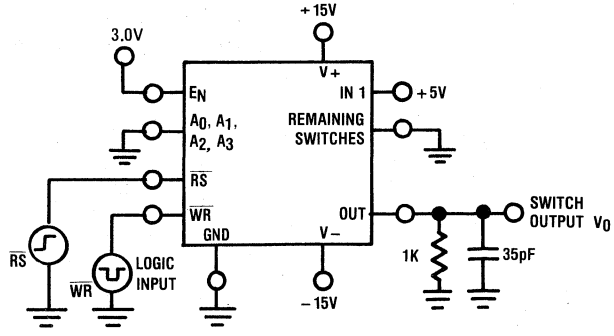
TEST CIRCUIT NO. 10
OFF ISOLATION



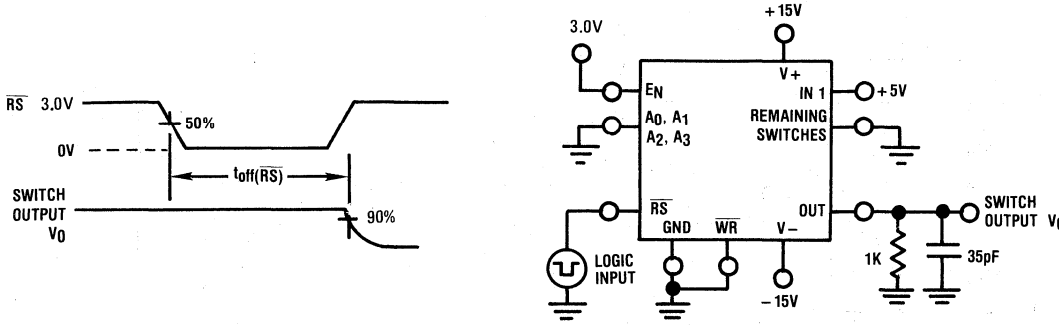
TEST CIRCUIT 11
WRITE TURN-ON TIME $t_{ON(\overline{WR})}$



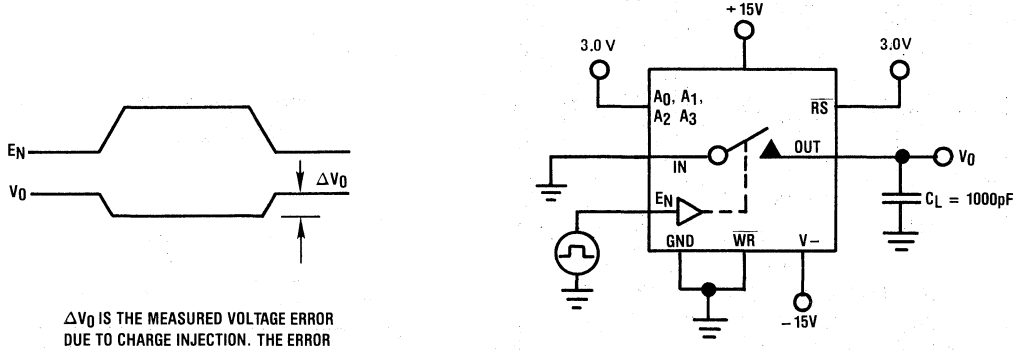
DEVICE MUST BE RESET PRIOR TO APPLYING $\overline{WR}$ PULSE



TEST CIRCUIT 12
RESET TURN-OFF TIME $t_{off(\overline{RS})}$



TEST CIRCUIT 13
CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L X \Delta V_O$.

DIE CHARACTERISTICS

Transistor Count	672
Die Size	168x124mils.
Thermal Impedance	
θ_{JA}	48°C/W
θ_{JC}	15°C/W
Tie Substrate to:	$-V_{Supply}$
Process	CMOS-DI

HARRIS

HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180 Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and Maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

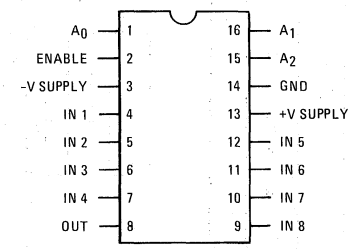
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ± 15V; however, reasonable performance is available down to ± 7V. Each device is packaged in a 16 pin DIP.

The HI-508/509 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUTS

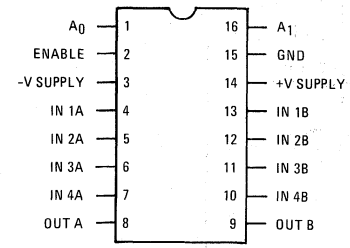
HI-508

TOP VIEW



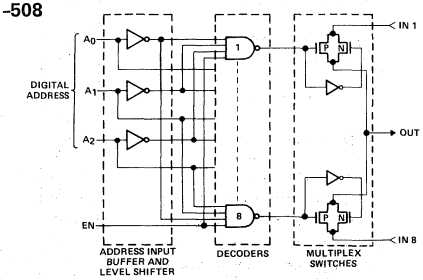
HI-509

TOP VIEW

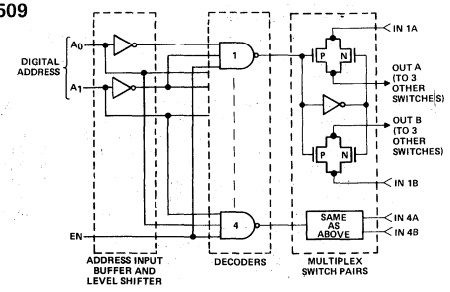


FUNCTIONAL DIAGRAMS

HI-508



HI-509



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}^{(+)}$ to $V_{Supply}^{(-)}$ 44V

$V_{Supply}^{(+)}$ to GND 22V

$V_{Supply}^{(-)}$ to GND 22V

Digital Input Overvoltage:

V_{EN}, V_A { $V_{Supply}^{(+)}$ +4V; $V_{Supply}^{(-)}$ -4V

Analog Input Overvoltage (Note 6):

V_D, V_S { $V_{Supply}^{(+)}$ +2V; $V_{Supply}^{(-)}$ -2V

Power Dissipation * 750mW

Operating Temperature Ranges:

HI-508/509-2, -8 -55°C to +125°C

HI-508/509-5, 0°C to 75°C

HI-508/509-1 -55°C to +200°C

Storage Temperature Range -65°C to +150°C

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified: Supplies = ± 15V, GND = 0V

		HI-508/HI-509-2 -55°C to +125°C			HI-508/HI-509-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance	+25°C		180	300		180	400	Ω
	Full		230	400		230	500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
$I_{S(OFF)}$, Off Input Leakage Current (Note 2)	+25°C		0.03	10		0.03		nA
	Full			50			50	nA
$I_{D(OFF)}$, Off Output Leakage Current								
HI-508	Full		0.3	200		0.3	200	nA
HI-509	Full		0.3	100		0.3	100	nA
$I_{D(ON)}$, On Channel Leakage Current								
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	+25°C			5			5	nA
	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AH}, High Threshold	Full	2.4			2.4			V
V_{AL}, Low Threshold	Full			0.8			0.8	V
I_A, Input Leakage Current (High or Low) (Note 3)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_A, Access (Transition) Time	+25°C		220	500		220		ns
	Full			1000			1000	ns
t_{OPEN}, Break-Before-Make Interval	+25°C	25	70		25	70		ns
$t_{ON(EN)}$, Enable Turn-On	+25°C		210	500		210		ns
	Full			1000			1000	ns
$t_{OFF(EN)}$, Enable Turn-Off	+25°C		180	500		180		ns
	Full			1000			1000	ns
t_S, Settling Tme to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
Off Isolation (Note 4)	+25°C	50	68		50	68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		21			21		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
I+, Positive Supply Current (Note 5)	Full			2			2	mA
I-, Negative Supply Current (Note 5)	Full			1			1	mA
P_D, Power Dissipation	Full			45			45	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Ten nanoamps is the practical limit for high speed measurement in the production test environment. Actually, I_S (off) is below 100pA for most devices, at 25°C.
3. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
4. V_{EN} = 0.8V, R_1 = 1K, C_1 = 15pF, V_S = 7V_{RMS}, f = 500kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
5. V_{EN} = 0V or 5V. All V_A = 0.
6. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

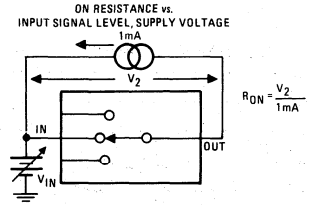
HI-509

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

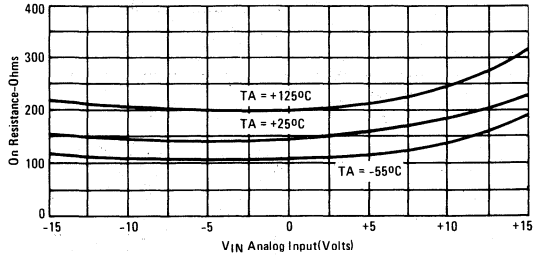
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

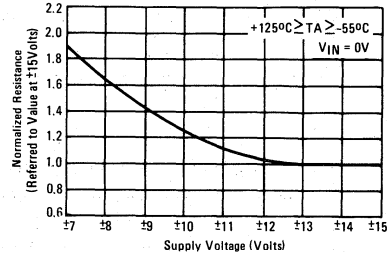
TEST CIRCUIT NO. 1



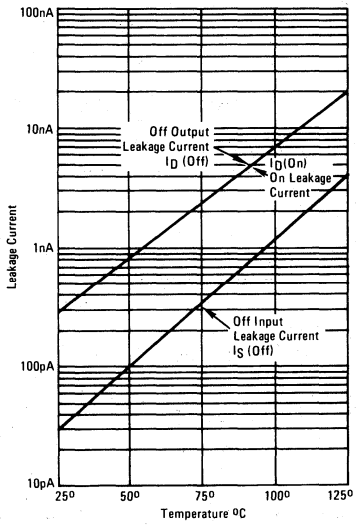
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



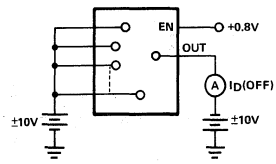
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



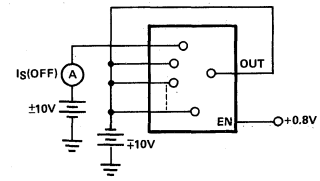
LEAKAGE CURRENT vs. TEMPERATURE



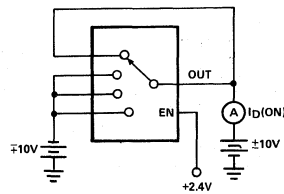
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

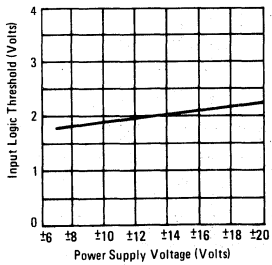


TEST CIRCUIT NO. 4*

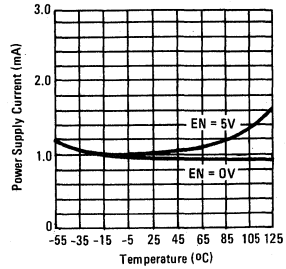


***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)**

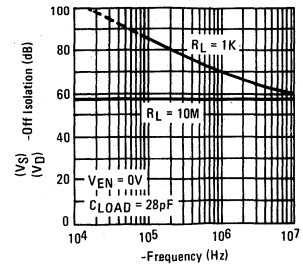
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

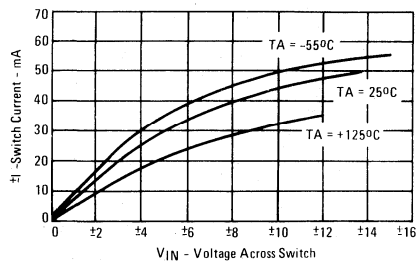


OFF ISOLATION vs. FREQUENCY

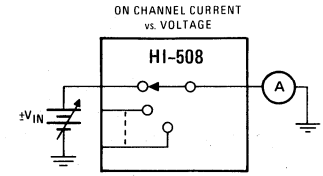


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

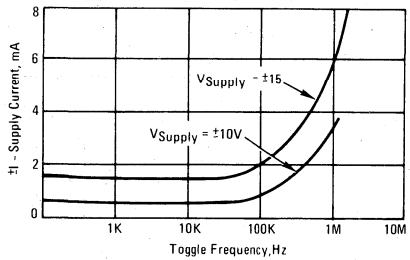
ON CHANNEL CURRENT vs. VOLTAGE



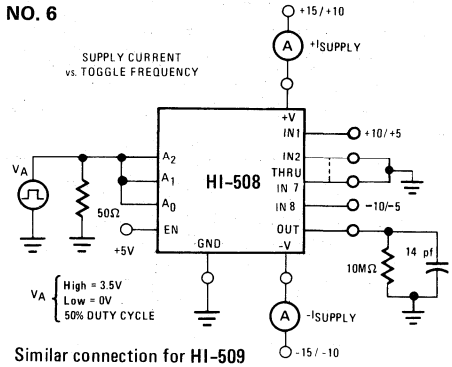
TEST CIRCUIT NO. 5



SUPPLY CURRENT vs. TOGGLE FREQUENCY

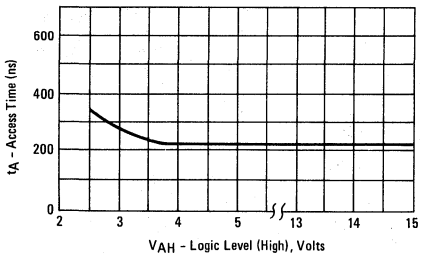


TEST CIRCUIT NO. 6

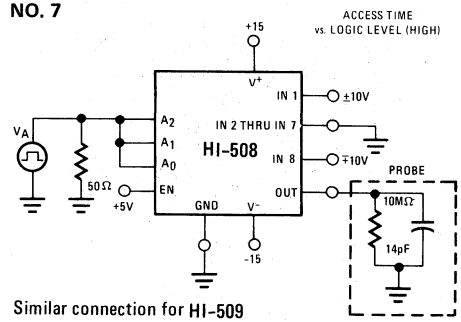


Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)

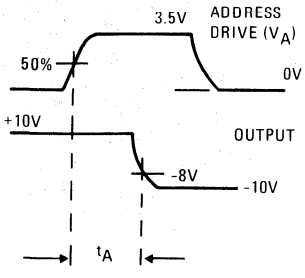


TEST CIRCUIT NO. 7

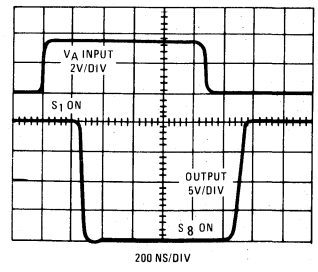


Similar connection for HI-509

SWITCHING WAVEFORMS



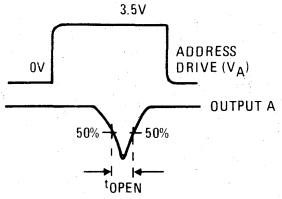
ACCESS TIME



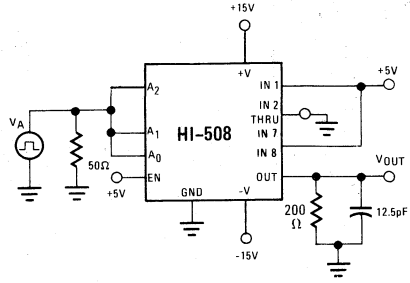
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT NO. 8

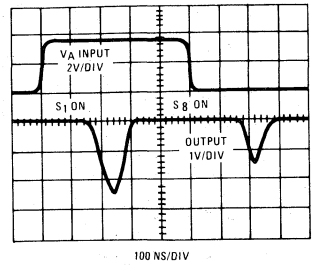
ADDRESS DRIVE



BREAK-BEFORE MAKE DELAY(t_{OPEN})



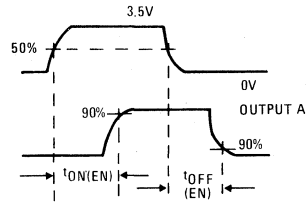
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



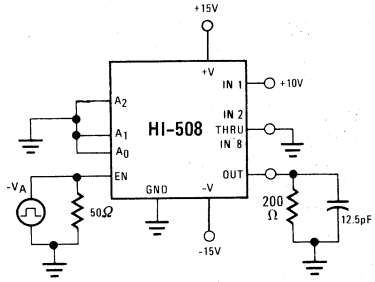
Similar connection for HI-509

TEST CIRCUIT NO. 9

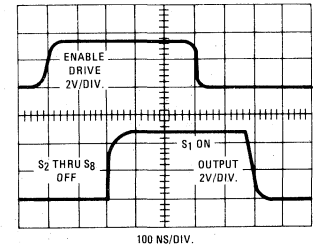
ENABLE DRIVE



ENABLE DELAY($t_{ON(EN)}$, $t_{OFF(EN)}$)



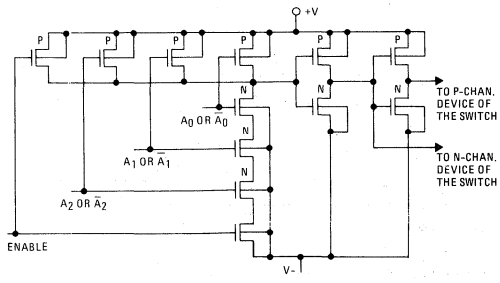
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



Similar connection for HI-509

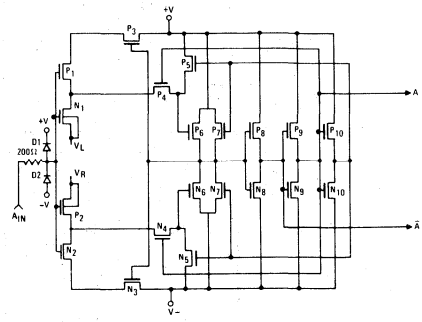
SCHEMATIC DIAGRAMS

ADDRESS DECODER



DELETE (A_2 OR $\bar{A}_2$) INPUT FOR HI-509

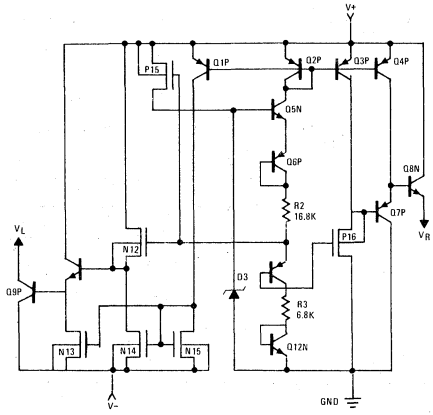
ADDRESS INPUT BUFFER LEVER SHIFTER



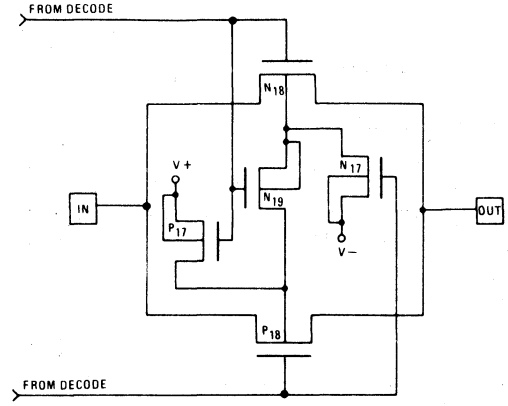
All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

SCHEMATIC DIAGRAMS (continued)

TTL REFERENCE CIRCUIT

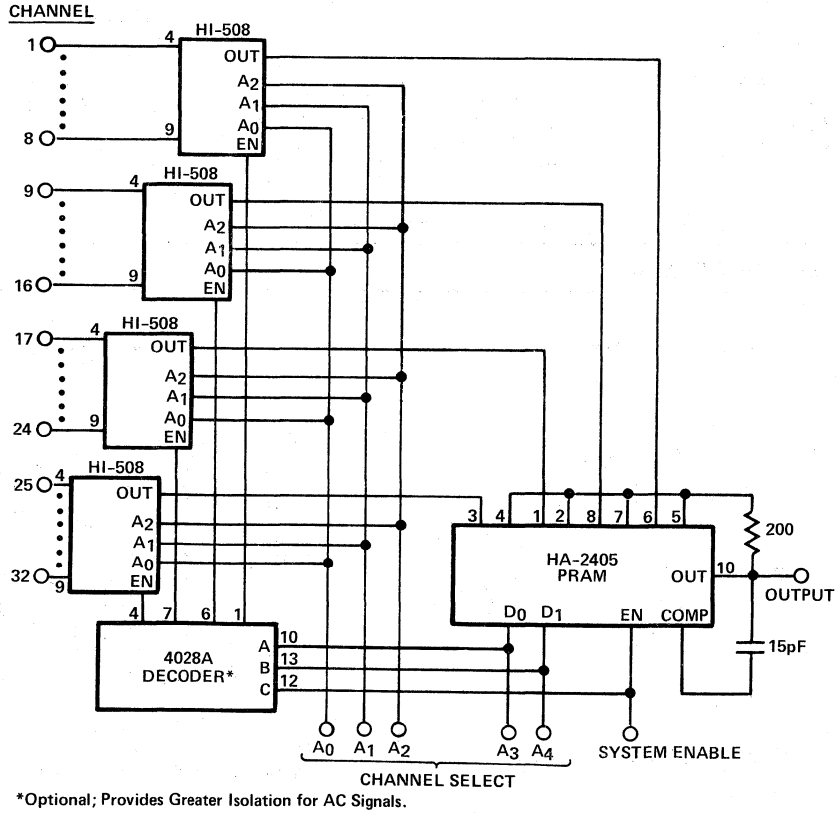


MULTIPLEX SWITCH



APPLICATIONS

32 CHANNEL BUFFERED MULTIPLEXER

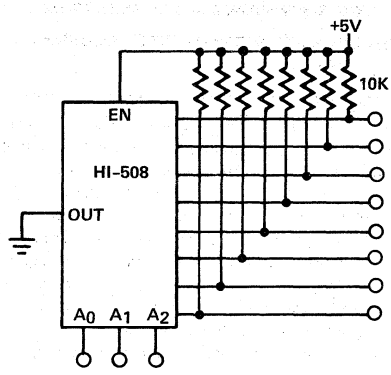


*Optional; Provides Greater Isolation for AC Signals.

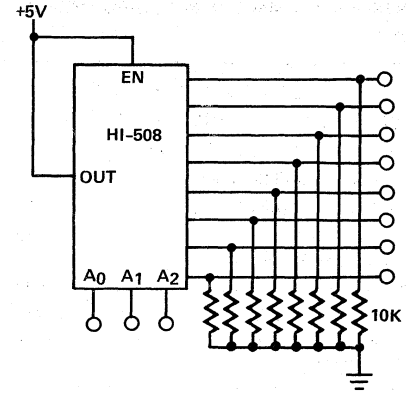
APPLICATIONS (continued)

ONE OF 8 DECODER

ACTIVE LOW



ACTIVE HIGH



DIE CHARACTERISTICS

Transistor Count		243
Die Size		86 x 79 mils
Thermal Constants	θ_{ja}	92°C/W
	θ_{jc}	37°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

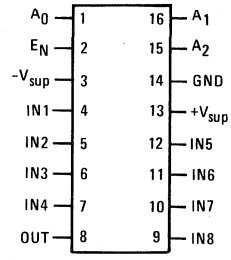
The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-508A/509A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUT

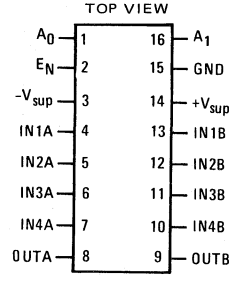
HI-508A

TOP VIEW



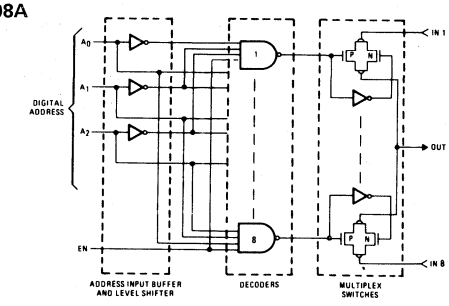
HI-509A

TOP VIEW

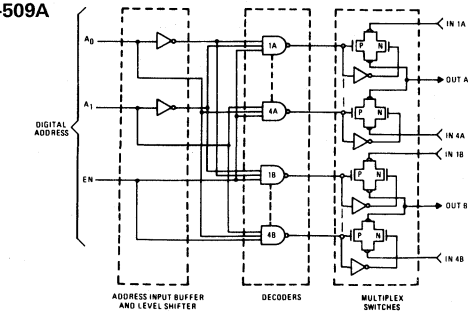


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 44V

V+ to Ground 22V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply}(+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V (unless otherwise specified).

For Test Conditions, consult Performance Characteristics section.

		HI-508A/509A-2 -55°C to +125°C			HI-508A/509A-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
HI-509A	Full			±125			±125	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
HI-509A				±125			±125	nA
I_{DIFF}, Differential OFF Output Leakage Current (HI-509A Only)	Full			±50			±50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5	1.0	μs
t_{OPEN}, Break - Before Make Delay	+25°C	25	80		25	80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	500		300		ns
				1000			1000	ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	500		300		ns
				1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C	50	68		50	68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	2.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	1.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	2.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	1.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 7V, R_L = 1K, C_L = 15pF, V_S = 3V RMS, f = 500kHz. Worst case isolation occurs on channel 4 due to proximity of the output pin(s).
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

* 100% Tested for Dash 8 at +25°C and +125°C only.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

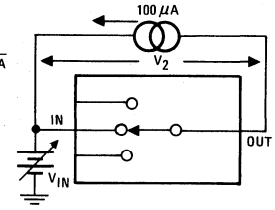
A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

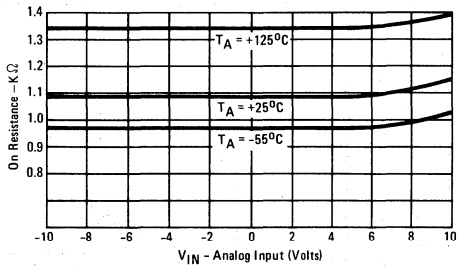
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

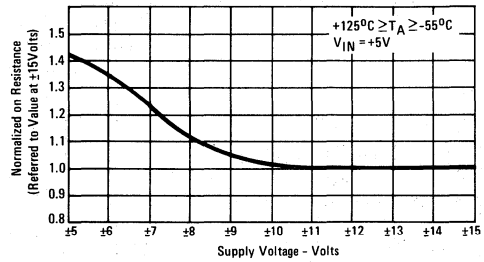


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

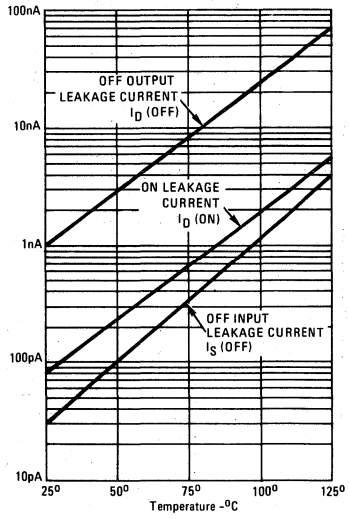
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



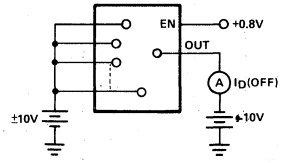
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



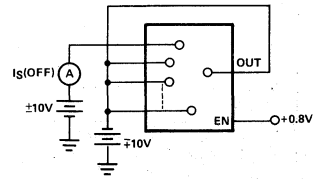
LEAKAGE CURRENT vs. TEMPERATURE



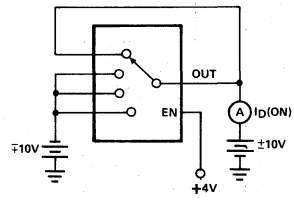
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

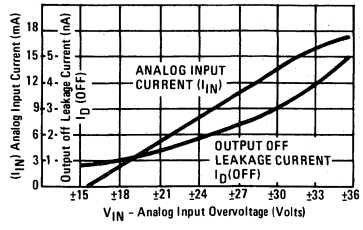


TEST CIRCUIT NO. 4*



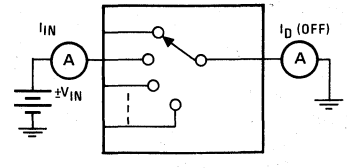
***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



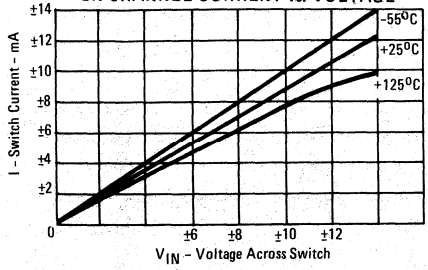
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



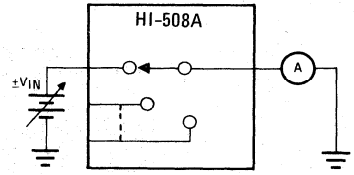
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

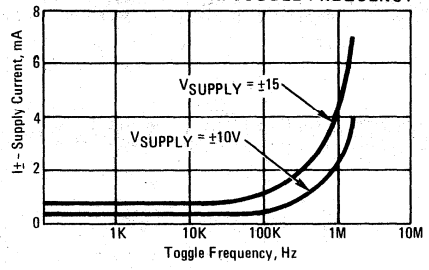


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

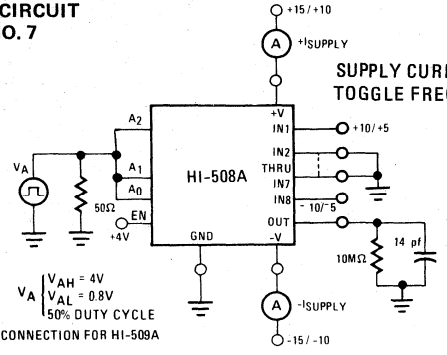


SUPPLY CURRENT vs. TOGGLE FREQUENCY



TEST CIRCUIT NO. 7

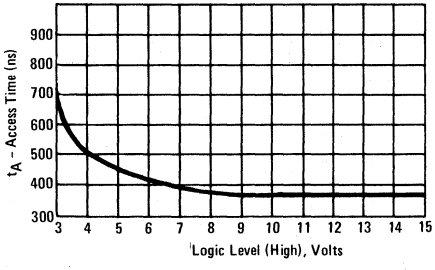
SUPPLY CURRENT vs. TOGGLE FREQUENCY



VA { VAH = 4V, VAL = 0.8V, 50% DUTY CYCLE

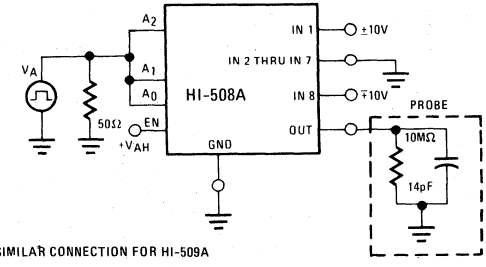
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



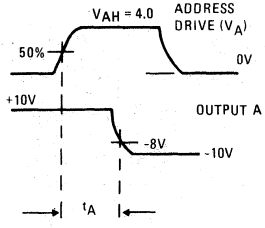
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

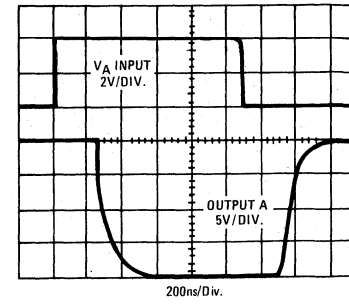


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS

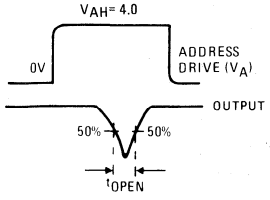


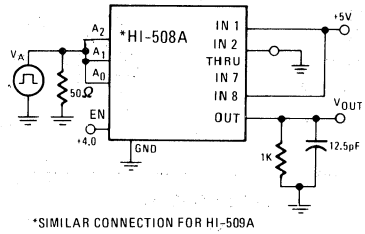
ACCESS TIME



SWITCHING WAVEFORMS (continued)

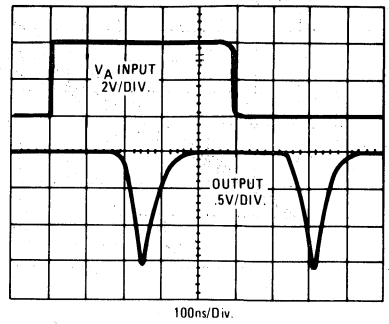
TEST CIRCUIT NO. 9
BREAK BEFORE MAKE DELAY (t_{OPEN})



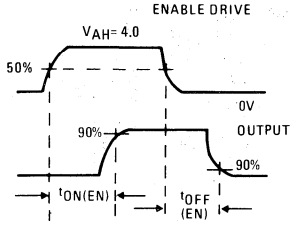


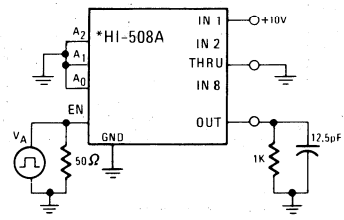
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



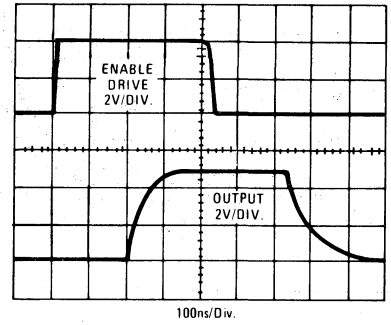
TEST CIRCUIT NO. 10
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



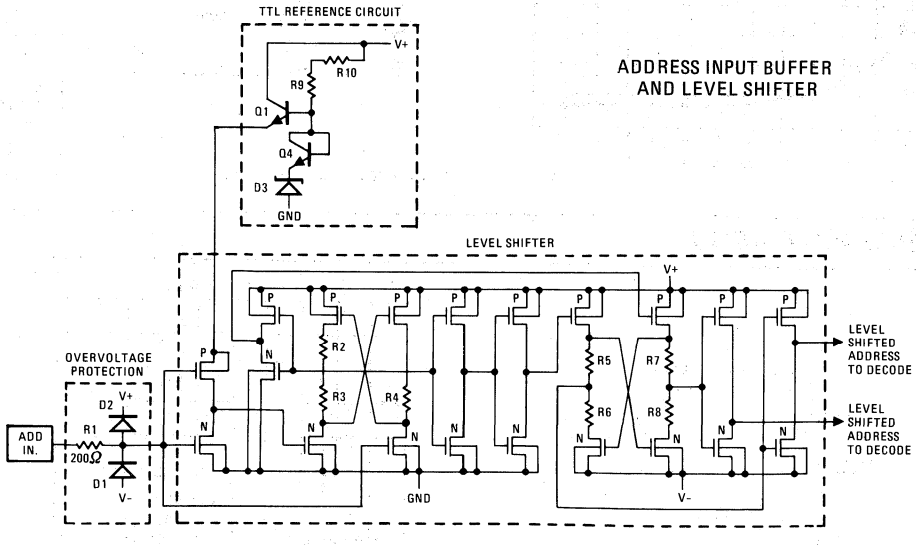


* SIMILAR CONNECTION FOR HI-509A

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

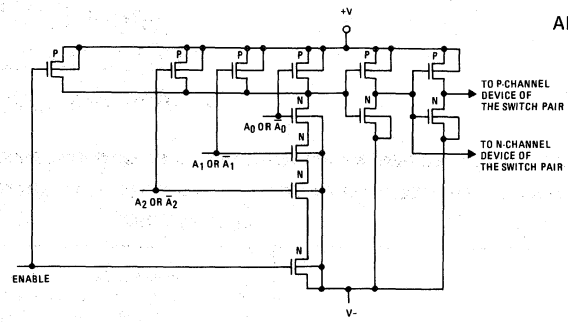


SCHEMATIC DIAGRAMS

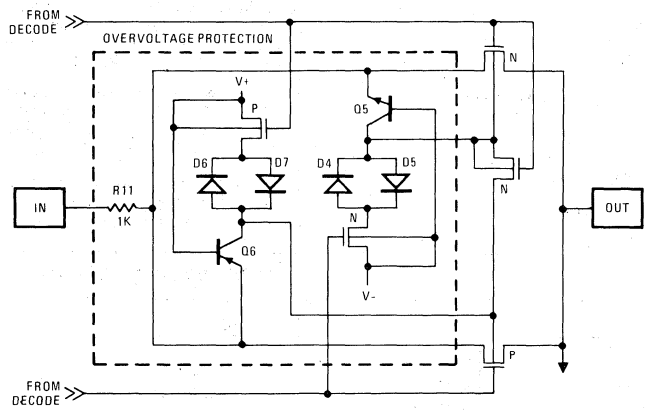


SCHEMATIC DIAGRAMS (continued)

ADDRESS DECODER



MULTIPLEX SWITCH



DIE CHARACTERISTICS

Transistor Count		253
Die Size		116 x 79 mils
Thermal Constants	θ_{ja}	78°C/W
	θ_{jc}	25°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HI-508L/HI-509L

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Latches And Overvoltage Protection

FEATURES

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq 4nA$ (typ) over full temp range
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

DESCRIPTION

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each model includes digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write (WR) and Reset (RS) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output must present a high impedance when power is off. This is achieved by a switch cell with three MOSFET's in series, rather than the conventional transmission gate design.

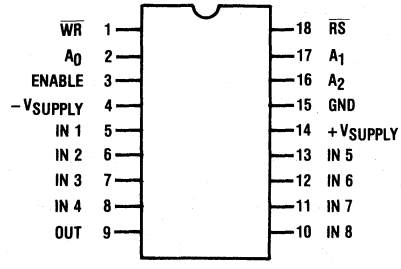
Each channel can withstand overvoltage to +25VDC with respect to ground with power ON or OFF. An OFF channel remains OFF in the presence of overvoltage. If the channel is ON, output voltage is clamped below the supply rail, which protects the load circuit.

The HI-508L offers 8 single-ended channels, and the HI-509L is a 4 channel differential version. The recommended supply voltages are 15V, though operation at reduced levels or with a single supply may also be implemented. The package is a 18 pin ceramic or plastic DIP.

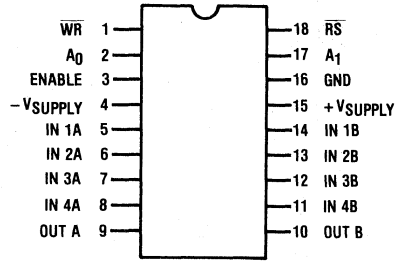
Each product is specified for the commercial temperature range (0°C to 75°C, -5 suffix) and the military range (-55°C to +125°C, -2 suffix). Military high reliability burned-in product is available as a "-8" suffix.

PINOUT

HI-508L

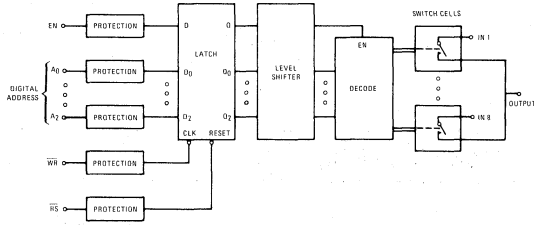


HI-509L

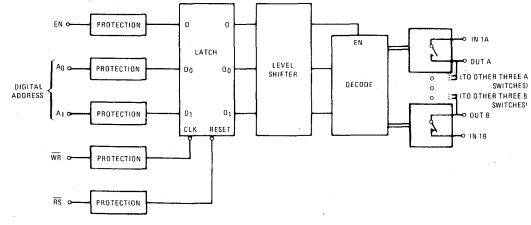


FUNCTIONAL DIAGRAM

HI-508L



HI-509L



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 4 and 14 (15)	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$,			
V supply (+)	+4V	HI-508L/509L-2	−55°C to 125°C
V supply (−)	−4V	HI-508L/509L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

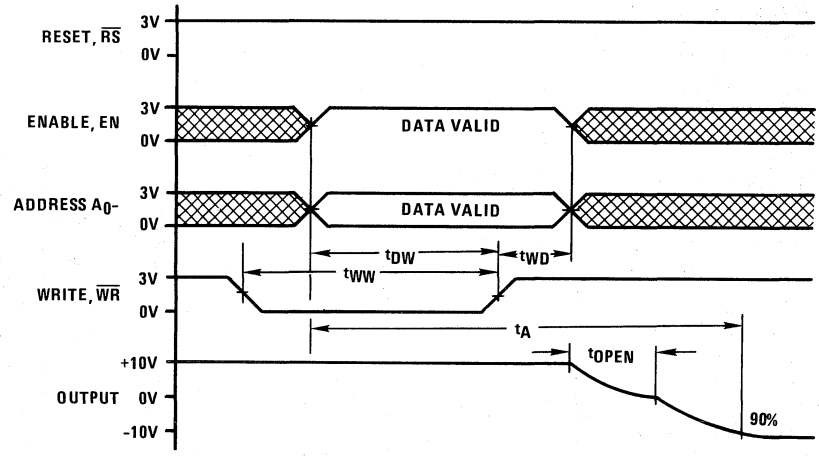
	HI-508L/509L-2 −55°C to +125°C				HI-508L/509L-5 0°C to +75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note 2)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
ΔR_{ON}, Change In R_{ON} (Note 3) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		5	50		5	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-508L	Full		4	100		4	100	nA
HI-509L	Full		2	50		2	50	nA
$I_{D(On)}$, ON Channel leakage current	+25°C			10			10	nA
HI-508L	Full		5	100		5	100	nA
HI-509L	Full		2	50		2	50	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 4)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-voltage applied (Note 4)	+25°C		5			5		nA
	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current (Note 5)	Full		10	40		10	40	μA
I_{AL}, Input Low Current (Note 5)	Full		40	200		40	200	μA
DYNAMIC SWITCHING CHARACTERISTICS (Note 6)								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	μS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		.025	0.1		μS
t_{ON}, (EN), Enable Delay (ON)	+25°C		0.5	1.0		0.5	1.0	μS
t_{OFF}, (EN), Enable Delay (OFF)	+25°C		0.5	1.0		0.5	1.0	μS
Settling Time (±0.1%)	+25°C		1.0			1.0		μS
(±0.01%)	+25°C		1.75			1.75		μS
OFF Isolation (Note 7)	+25°C	50	68		50	68		dB
OFF Isolation POWER OFF (Note 8)	+25°C		56			56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-508L	+25°C		25			25		pF
HI-509L	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 9)	Full		60	100		60	100	mW
I +, Current Pin 14 (Note 9)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 4 (Note 9)	Full		0.3	0.6		0.3	0.6	mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ± 10V, I out = -100μA
3. $\Delta R_{ON} = \frac{R_{ON}(Max) - R_{ON}(Min).}{R_{ON}(Avg.)}$ V_{IN} = ± 10V
4. Analog Overvoltage = ± 25V
5. I_{AH} and I_{AL} tested at 2.4V and 0.4 V respectively
6. For measurements in this section, input logic levels are 3.0V (High) and 0V (Low).
7. V_{EN} = 0.8V, R_L = 1KΩ, C_L = 15pF, V_S = 7Vrms, f = 500kHz
   Off isolation = 20 log $\frac{|V_D|}{|V_S|}$
   Worst case isolation on channel 4 due to proximity of the output pin(s)
8. V+, V- = 0V, R_L = 1KΩ
   C_L = 50pF, V_S = 3Vrms, f = 500 kHz.
9. See Test Circuit #8 for high toggle frequency applications.

MINIMUM TIMING REQUIREMENTS

PARAMETER	MIN LIMITS FULL TEMP RANGE	UNITS
t_{WW}, Write Pulse Width	300	nS
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	225	nS
t_{WD}, A, EN Data Valid After Write (hold Time)	100	nS
t_{RS}, RESET pulse width	400	nS
t_{OFF} ($\overline{RS}$) Reset Delay	1000	nS
t_{ON} ($\overline{WR}$) Write Turn-on Time	1000	nS

TIMING REQUIREMENTS



1. $+V_{SUPPLY}$ = +15V; $-V_{SUPPLY}$ = -15V.
2. Logic Levels: V_{AL} = 0V; V_{AH} = +3.0V.
3. Time intervals are measured between 50% levels unless otherwise noted.
4. Minimum values for $t_{\overline{RS}}$, t_{DW}, t_{WW} and t_{WD} are guaranteed separately but not simultaneously.

Figure 1

SCHEMATIC DIAGRAM

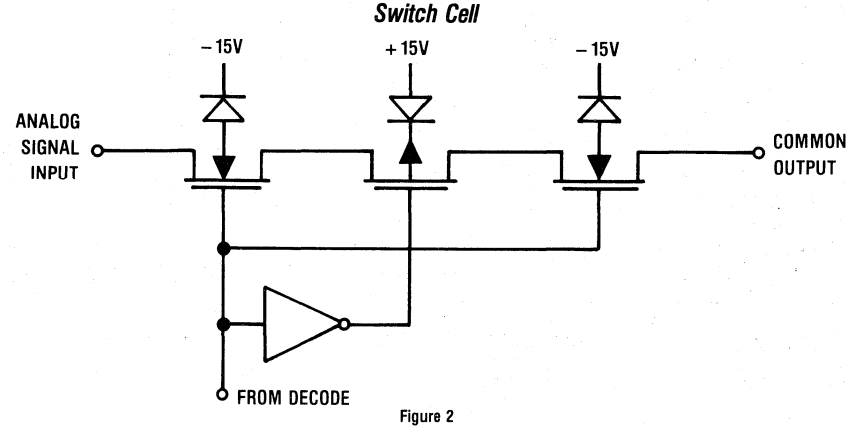


Figure 2

TRUTH TABLES

508L

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL
X	X	X	L	L	H	None
X	X	X	X	↓	H	Previous ON Channel.
X	X	X	X	X	L	None (latches cleared)
L	L	L	H	L	H	Channel 1
L	L	H	H	L	H	Channel 2
L	H	L	H	L	H	Channel 3
L	H	H	H	L	H	Channel 4
H	L	L	H	L	H	Channel 5
H	L	H	H	L	H	Channel 6
H	H	L	H	L	H	Channel 7
H	H	H	H	L	H	Channel 8

509L

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL PAIR
X	X	L	L	H	None
X	X	X	↓	H	Previous ON Channel.
X	X	X	X	L	None (latches cleared)
L	L	H	L	H	Channel 1A and 1B
L	H	H	L	H	Channel 2A and 2B
H	L	H	L	H	Channel 3A and 3B
H	H	H	L	H	Channel 4A and 4B

DESCRIPTION AND APPLICATION

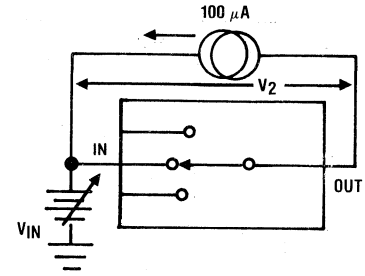
The switch cell of HI-508L/509L has a different structure than earlier Harris designs (HI-508, HI508A). The new switch (Figure 2) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the transmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers higher Off Isolation with power off, and better fault performance. Channel overvoltage protection is inherent since one of the three MOSFETs turn off in the presence of overvoltage. This turn-off process begins well below the supply rail so the V_{IN} range is less than the power supply range. Electrical performance is guaranteed to ±10V for each channel, and the usable range extends above ±11 Volts.

The address inputs A_0, A_1, A_2, and ENABLE are latched into an internal buffer when $\overline{WR}$ goes high. Each latch output is level shifted into the decode section, which activates the appropriate channel. The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system RESET line, to assure that all channels are OFF following a turn-on of power. The reset function overrides all others, just as $\overline{WR}$ overrides the address inputs (A_0-A_2 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e., the latches are "transparent". Refer to Figure 1.

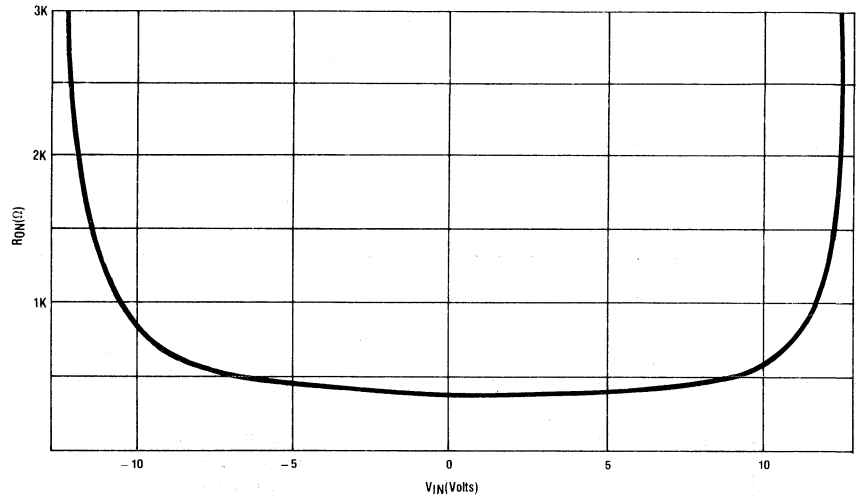
For additional Applications information please see AN 545.

TEST CIRCUIT NO. 1

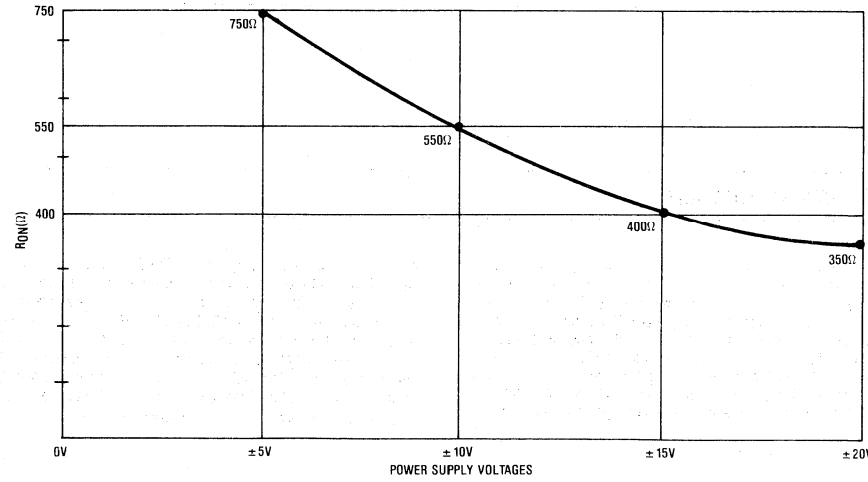
ON RESISTANCE vs.
INPUT SIGNAL LEVEL



VIN vs. RON

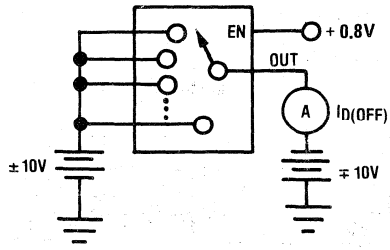


RON vs. POWER SUPPLY VOLTAGES
INPUT = 0V

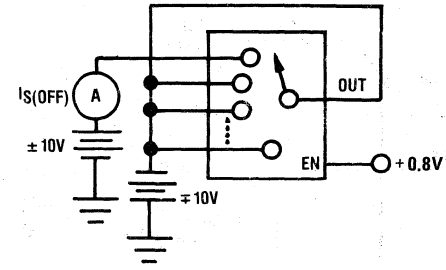


HI-508L TEST CIRCUITS

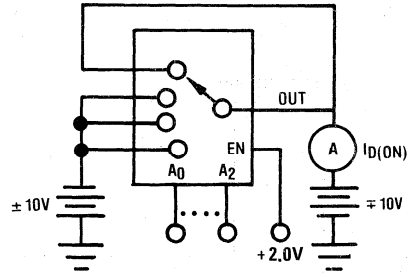
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*



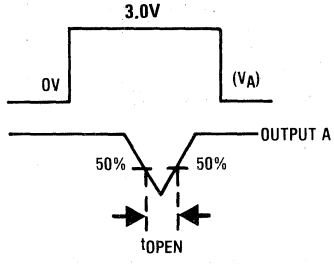
TEST CIRCUIT NO. 4*



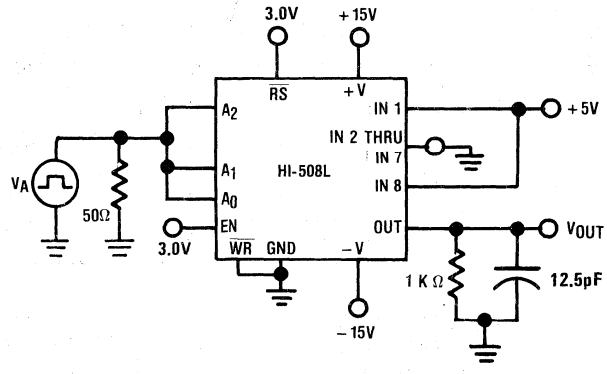
*Two measurements per channel:
+ 10V/ – 10V and – 10V/ + 10V.
(Two measurements per device for $I_{D(OFF)}$:
+ 10V/ – 10V and – 10V/ + 10V.)

TEST CIRCUIT NO. 5

ADDRESS DRIVE

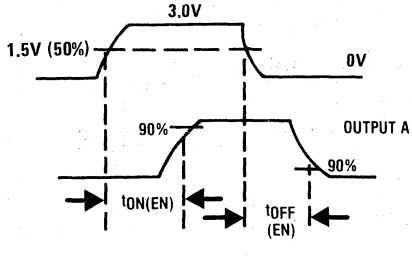


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

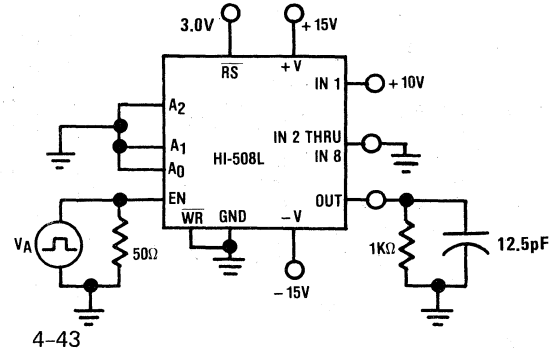


TEST CIRCUIT NO. 6

ENABLE DRIVE

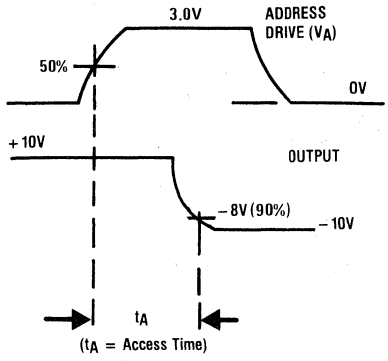


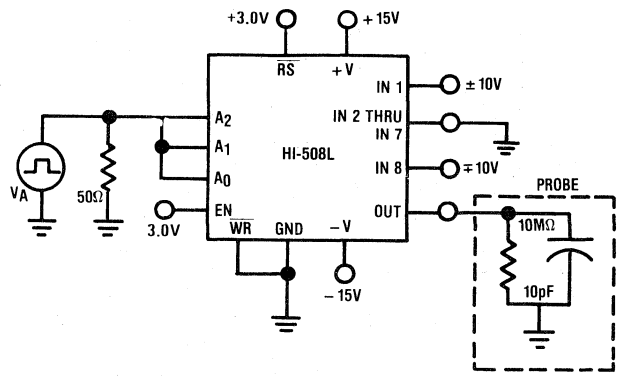
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



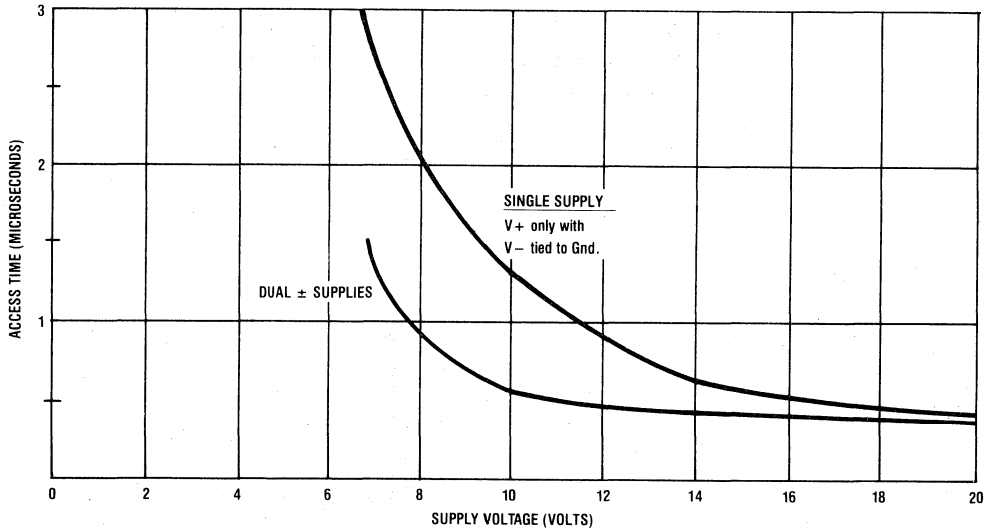
TEST CIRCUIT NO. 7

ACCESS TIME

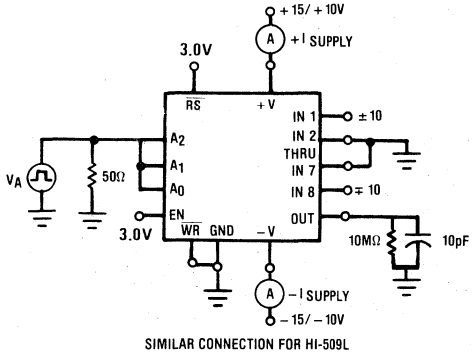




ACCESS TIME vs. SUPPLY VOLTAGE

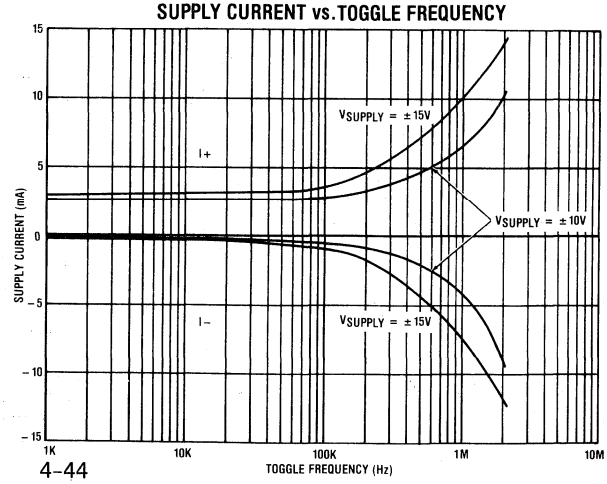


TEST CIRCUIT NO. 8
SUPPLY CURRENTS vs. TOGGLE FREQUENCY

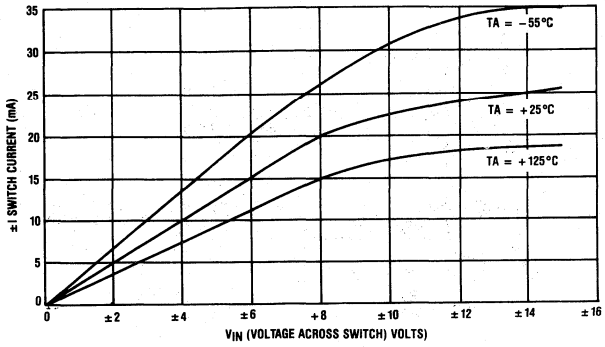


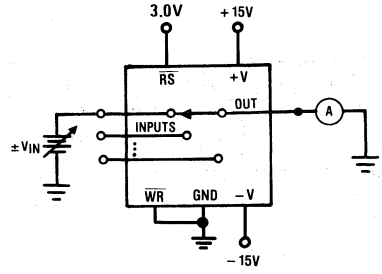
SIMILAR CONNECTION FOR HI-509L

SUPPLY CURRENT vs. TOGGLE FREQUENCY

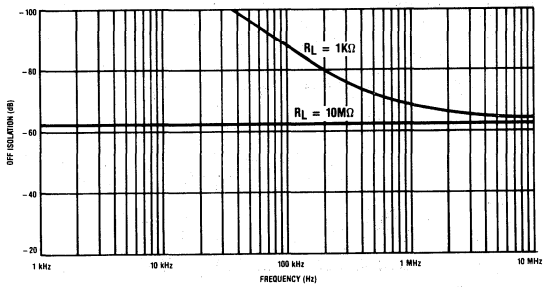


TEST CIRCUIT NO. 9
ON CHANNEL CURRENT vs. INPUT VOLTAGE

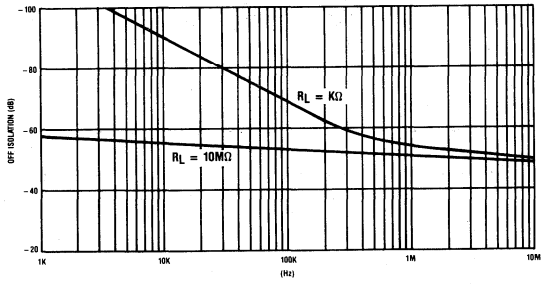




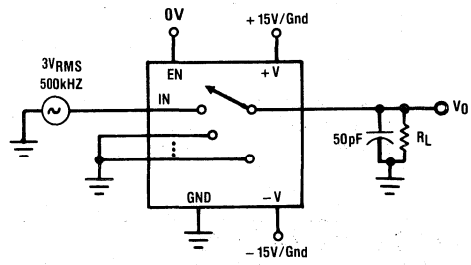
OFF ISOLATION vs. FREQUENCY POWER ON



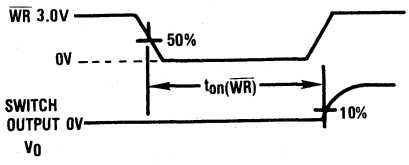
OFF ISOLATION vs. FREQUENCY (POWER OFF)



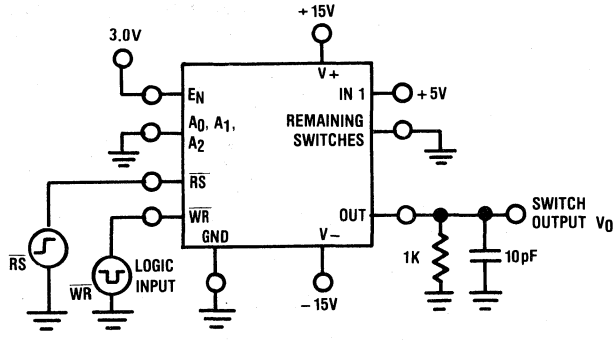
TEST CIRCUIT NO. 10
OFF ISOLATION



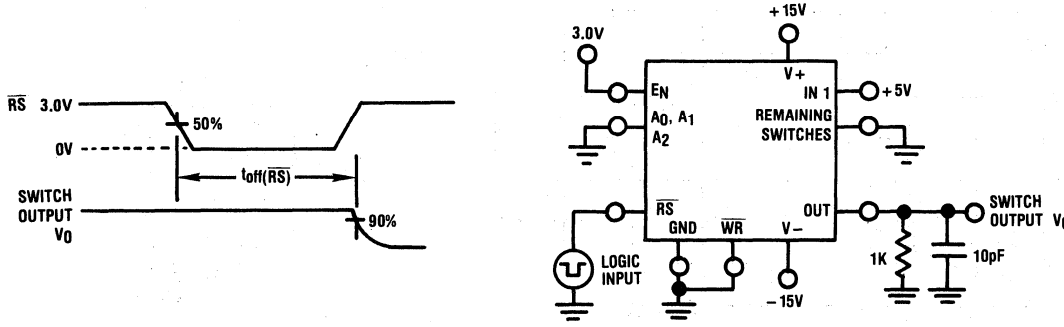
TEST CIRCUIT 11
WRITE TURN-ON TIME $t_{ON(\overline{WR})}$



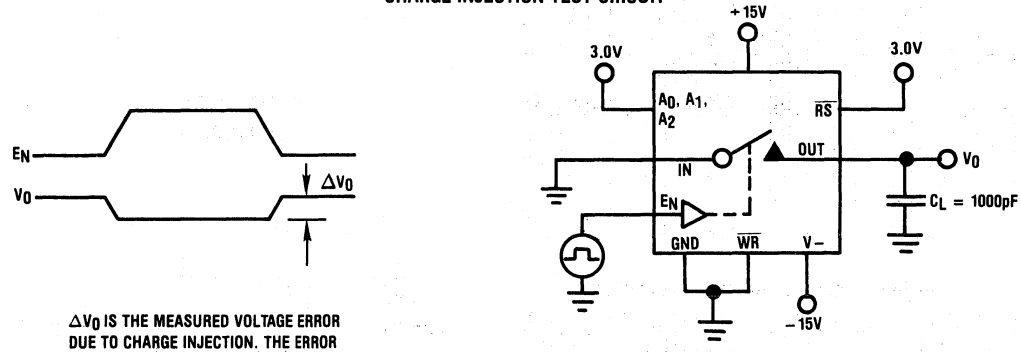
DEVICE MUST BE RESET PRIOR TO APPLYING $\overline{WR}$ PULSE



TEST CIRCUIT 12
RESET TURN-OFF TIME $t_{off(\overline{RS})}$



TEST CIRCUIT 13
CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L X \Delta V_O$.

DIE CHARACTERISTICS

Transistor Count	397
Die Size	124x114mils.
Thermal Impedance	
θJA	80°C/W
θJC	22°C/W
Tie Substrate to:	$-V_{Supply}$
Process	CMOS-DI

HARRIS

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 100ns
- SETTLING TIME (TYP TO 0.01%) 800ns
- LOW LEAKAGE I_S OFF 10pA
  I_D OFF 35pA
- LOW CAPACITANCE C_S OFF 2.5pF
  C_D OFF 18pF
- HIGH OFF ISOLATION AT 1MHz 80dB
- LOW CHARGE INJECTION 0.3pC
- SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

DESCRIPTION

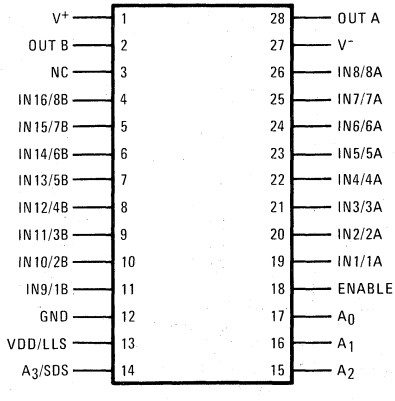
The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_D Off < 100pA @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process controls.

The HI-516 is available in a 28 lead dual-in-line package, and offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

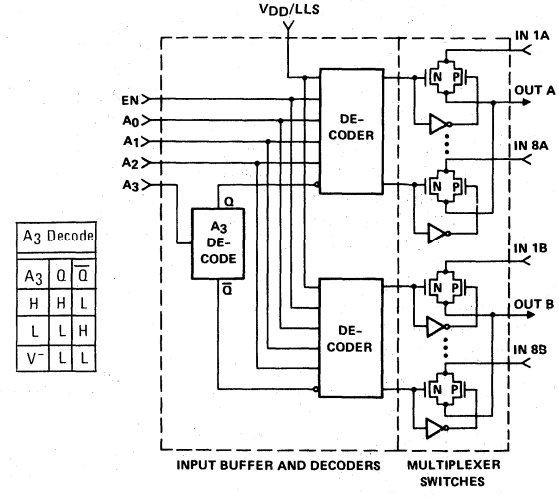
The HI-516 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



A3 Decode

A3	Q	Q̄
H	H	L
L	L	H
V-	L	L

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A3 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation	1200mW
Operating Temperature Ranges:	
HI-516-2	-55°C to +125°C
HI-516-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1)

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range (Note 2)	Full	-14		+14	-15		-15	V
R_{ON}, On Resistance (Note 3)	+25°C		620	750		620	750	Ω
	Full		770	1,000		700	1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full		0.38	50		0.38	50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.035			0.035		nA
	Full		0.48	100		0.48	100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full		0.56	100		0.56	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AL} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full		120	200		120	200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (IN)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	125		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 4)	+25°C		0.33			0.33		pC
Off Isolation (Note 5)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2.5			2.5		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 6)	Full		17.5	25		17.5	30	mA
I^-, Current (Note 6)	Full		17.5	25		17.5	30	mA
I^+, Standby (Note 7)	Full		17.0	25		17.0	30	mA
I^-, Standby (Note 7)	Full		17.0	25		17.0	30	mA

NOTES:
1. V_{DD}/LLS pin = open or grounded for TTL Compatibility
   V_{DD}/LLS pin = V_{DD} for CMOS Compatibility
2. At temperatures above 90°C, care must be taken to assure V_S remains at least 1.0V above the V_{SUPPLY} for proper operation.
3. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
4. V_{IN} = 0V, C_L = 100pF, Enable input pulse = 3V, f = 500kHz.
5. V_{EN} = 0.8V, $V_S = 3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1k, Pin 3 grounded.
6. V_{EN} = +2.4V
7. V_{EN} = 0.8V

TRUTH TABLES

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

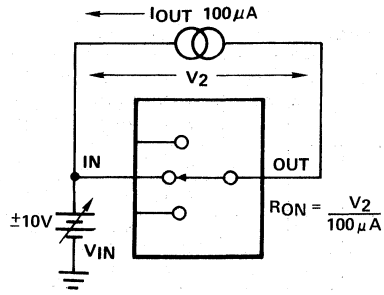
HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

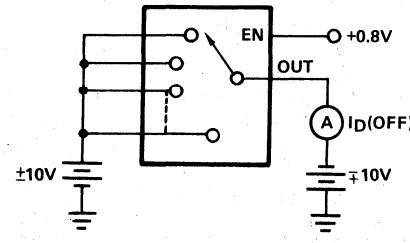
DIE CHARACTERISTICS

Transistor Count		647
Die Size		90 x 147 mils
Thermal Constants	θ_{ja}	50°C/W
	θ_{jc}	18°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

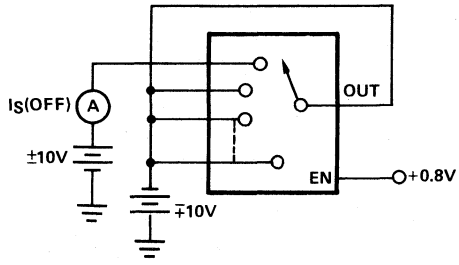
TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL



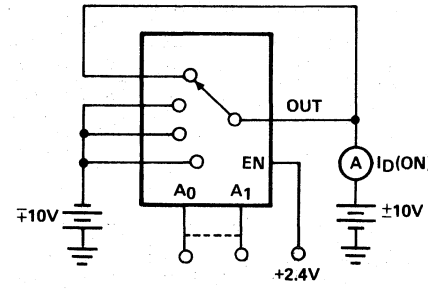
TEST CIRCUIT NO. 2*



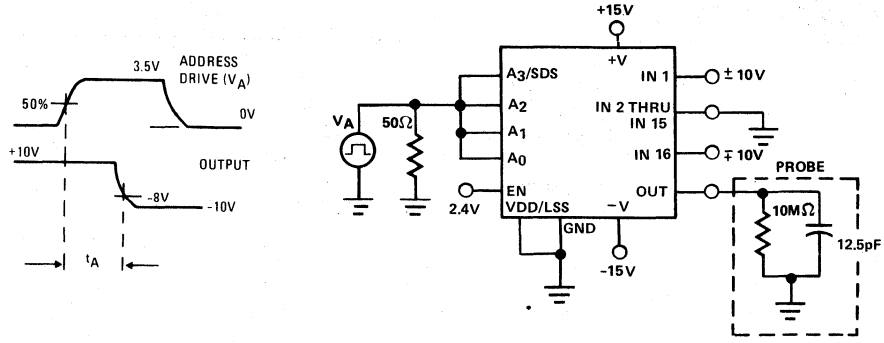
TEST CIRCUIT NO. 3*



TEST CIRCUIT NO. 4*



TEST CIRCUIT NO. 5
ACCESS TIME

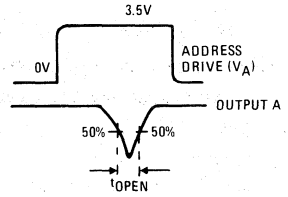


*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

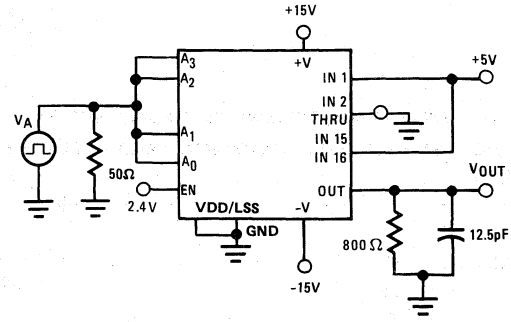
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 6

ENABLE DRIVE

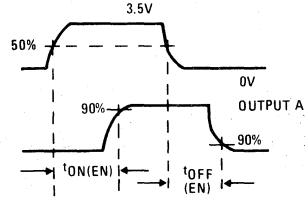


BREAK-BEFORE MAKE DELAY (t_{OPEN})

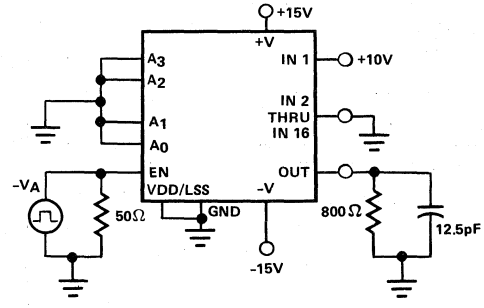


TEST CIRCUIT NO. 7

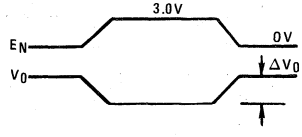
ENABLE DRIVE



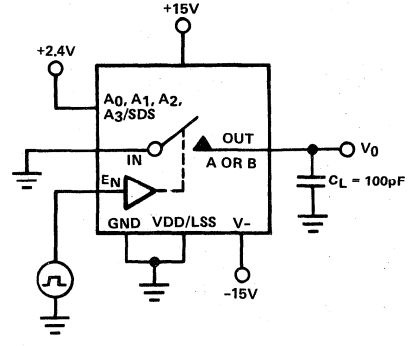
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_O$.



HARRIS

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 80ns
- SETTLING TIME (0.1%) 250ns
- LOW LEAKAGE I_S (OFF) 50pA
  I_D (OFF) 100pA
- LOW CAPACITANCE (TYP) C_S (OFF) 2pF
  C_D (OFF) 10pF
- HIGH OFF ISOLATION @ (1MHz) 75dB
- SINGLE ENDED TO DIFFERENTIAL MODE SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)
- LOW CHARGE INJECTION 0.3pC

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-518 is a monolithic, high performance, high speed Analog Multiplexer, constructed utilizing the Harris Dielectrically isolated CMOS process.

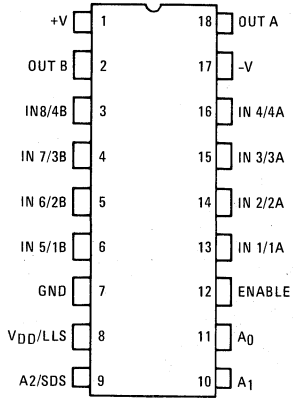
This device has the added feature that it can be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A2 as a digital address input, or as a 4-channel differential multiplexer by connecting A2 to the V^- supply.

TTL or CMOS compatibility is also selectable. Low leakage current, I_D off < 100pA @ 25°C, and fast settling, 250ns to 0.1%, characteristics of this device make it an ideal choice for high speed data acquisition systems, precision instrumentation and industrial process controls.

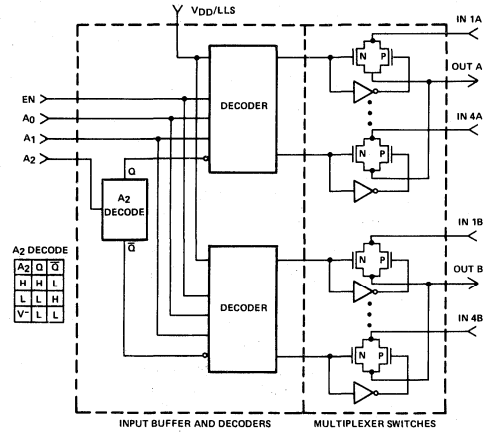
The HI-518 is available in an 18 lead Dual-in-Line package. The HI-518 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	-6V < V_{AH} < +6V	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation	725mW
Operating Temperature Ranges:	
HI-518-2	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Gnd. (Note 1).

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range (Note 2)	Full	-14		+14	-15		+15	V
R_{ON} On Resistance (Note 3)	+25°C		480	750		480	750	Ω
	Full		700	1000		700	1000	Ω
I_S (OFF) Off Input	+25°C		0.05			0.05		nA
Leakage Current	Full		0.60	50		0.60	50	nA
I_D (OFF) Off Output	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
I_D (ON) On Channel	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AH} Input Leakage Current (Low)	Full		4	20		4	20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	
	Full		110	150		110	150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		
Charge Injection (Note 4)	+25°C		0.3			0.3		pC
Off Isolation (Note 5)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		1.9			1.9		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 6)	Full		12	15		12	18	mA
I⁻, Current (Note 6)	Full		12	15		12	18	mA
I+, Standby (Note 7)	Full		11.5	15		11.5	18	mA
I⁻, Standby (Note 7)	Full		11.5	15		11.5	18	mA

1. V_{DD}/LLS Pin = Open or Grounded ed for TTL compatibility. V_{DD}/LLS for CMOS compatibility.
2. At temperatures above 90°C, care must be taken to assure V_S remains at least 1.0V above the V_{SUPPLY}.
3. V_{IN} = ± 10V, I_{OUT} = -100 A.
4. V_{IN} = 0V, C_L = 100pF, Enable Input pulse = 3V, f = 500kHz.
5. C_L = 40pF, R_L = 1k. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
6. V_{EN} = +2.4V.
7. V_{EN} = 0.8V

TRUTH TABLES

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

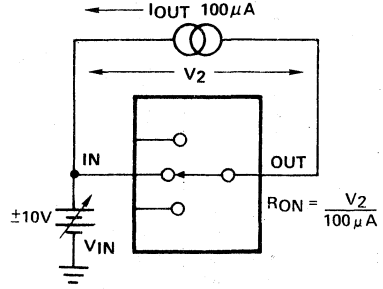
DIE CHARACTERISTICS

Transistor Count		356
Die Size		90 x 93 mils
Thermal Constants	θ_{ja}	84°C/W
	θ_{jc}	25°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

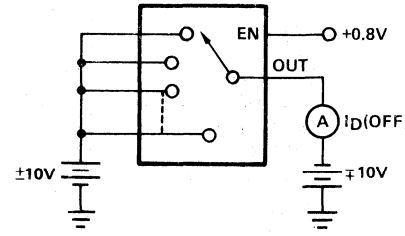
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

TEST CIRCUIT NO. 1

ON RESISTANCE vs.
INPUT SIGNAL LEVEL



TEST CIRCUIT NO. 2*

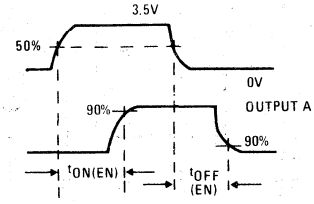


*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

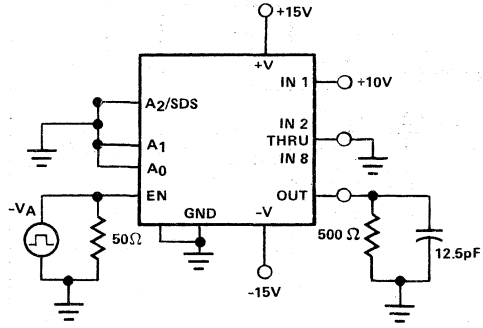
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 7

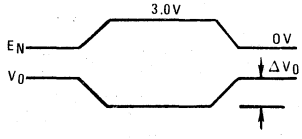
ENABLE DRIVE



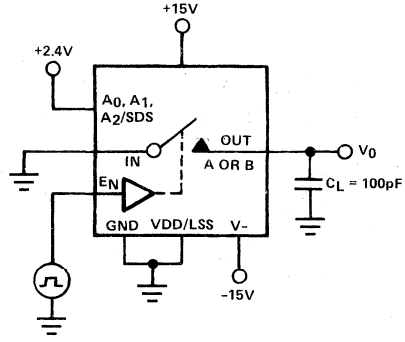
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT

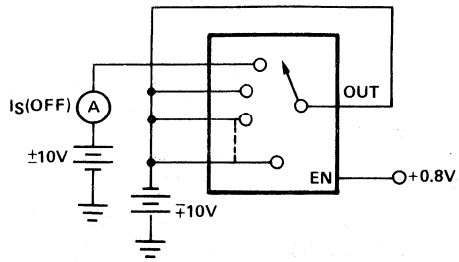


ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L X \Delta V_O$.

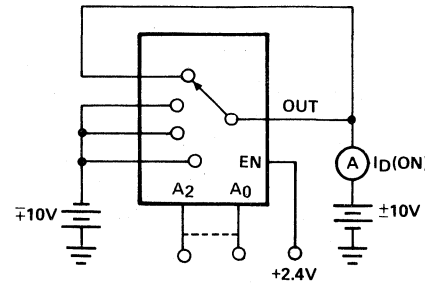


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 3*

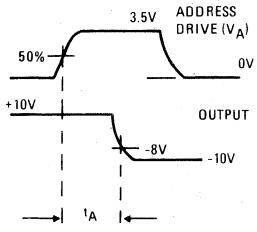


TEST CIRCUIT NO. 4*

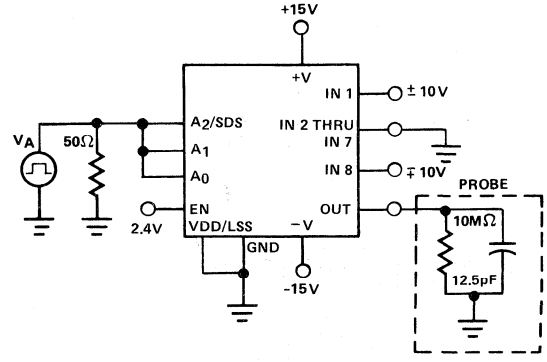


*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

TEST CIRCUIT NO. 5

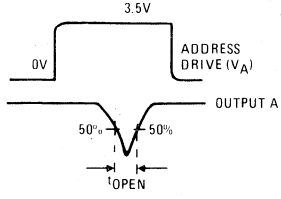


ACCESS TIME

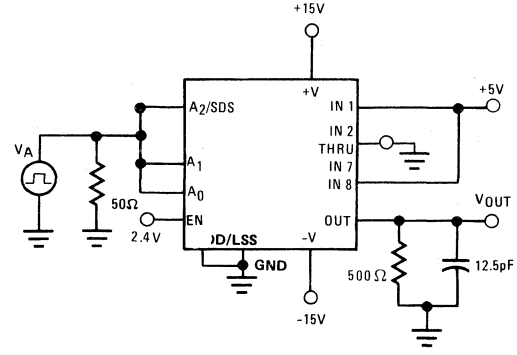


TEST CIRCUIT NO. 6

ENABLE DRIVE



BREAK-BEFORE MAKE DELAY (t_{OPEN})



HARRIS

HI-524

4 Channel Video Multiplexer

FEATURES

- CROSSTALK (10MHz) > 60dB
- FAST ACCESS TIME 150ns
- FAST SETTLING TIME (0.01%) 600ns
- TTL COMPATIBLE

APPLICATIONS

WIDEBAND SWITCHING

- RADAR
- TV VIDEO
- ECM

DESCRIPTION

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended video signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk exceeds 60dB at 10MHz.

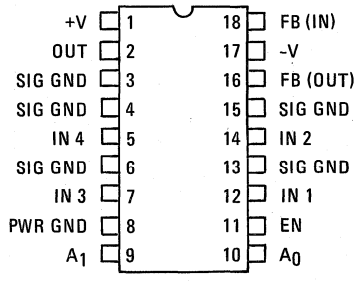
The HI-524 is designed to operate into a wideband buffer amplifier such as the HARRIS HA-5190. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic DIP and operates on ±15V supplies.

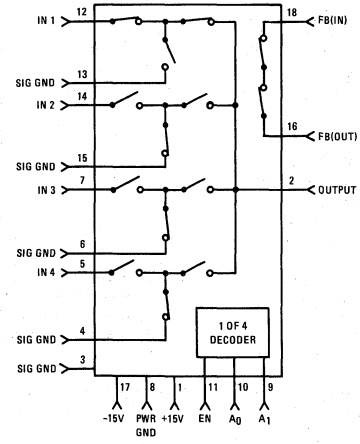
The HI-524 is offered in both commercial and military grades. For Additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

* CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:
$-6V < V_{AH} < +6V$

Analog Input (V_S) or Output (V_O)
$+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V

Voltage Between Supply Pins 33V

Either Supply to Ground 16.5V
Total Power Dissipation* 750mW
Operating Temperature Range:
HI-524-2, -8 -55°C to +125°C
HI-524-5 0°C to 75°C
Storage Temperature Range -65°C to 150°C
*Derate 13.6mW/°C above T_A = 120°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

PARAMETER	TEMP	HI-524-2, -8 -55°C to +125°C MIN	TYP	MAX	HI-524-5 0°C to +75°C MIN	TYP	MAX	UNITS
Analog Channel Characteristics								
V_S, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 1)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 2)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 3)	Full		16			16		MHz
Digital Input Characteristics								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
Switching Characteristics								
t_A, Access Time (Note 4)	+25°C		150	300		150	300	ns
	Full							ns
t_{OPEN}, Break before make delay (Note 4)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 4)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 5)	+25°C		-65			-65		dB
C_S (OFF), Channel Input Capacitance	+25°C			6		6		pF
C_D (OFF), Channel Output Capacitance	+25°C			4		4		pF
C_A, Digital Input Capacitance	+25°C			5		5		pF
Power Requirements								
P_D, Power Dissipation	Full		540			540		mW
I^+, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^-, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^+, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA
I^-, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA

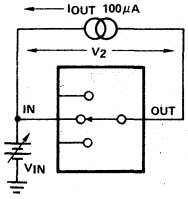
1. V_{IN} = 0V; I_{OUT} = 100μA (See Test Circuit #1)
2. V_O = ±10V; VS = ±10V (See Test Circuits # 2, 3, 4)
3. MUX output is buffered with HA-5033 or other Video performance amplifier properly matched.
4. (See Test Circuit #5)
5. V_{IN} = 10MHz, $3V_{p-p}$ on one channel with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-5033 or other Video amp. Terminate all input channels with 75Ω.
6. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V)

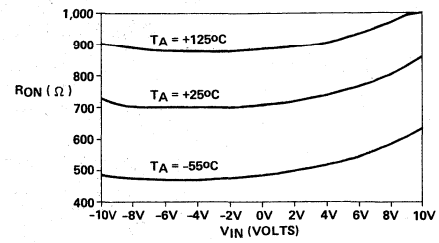
ON RESISTANCE

TEST CIRCUIT NO. 1

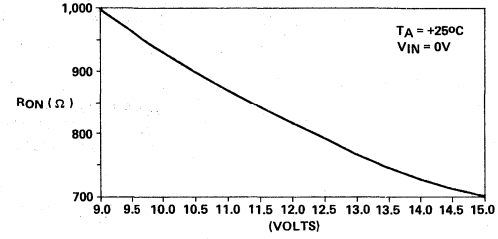


$$R_{ON} = \frac{V_2}{100\mu A}$$

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

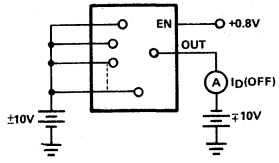


ON RESISTANCE VS. SUPPLY VOLTAGE

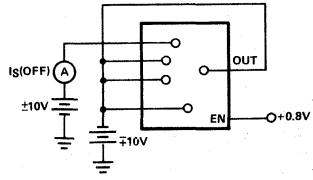


LEAKAGE CURRENT

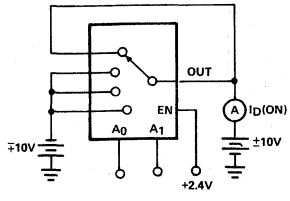
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

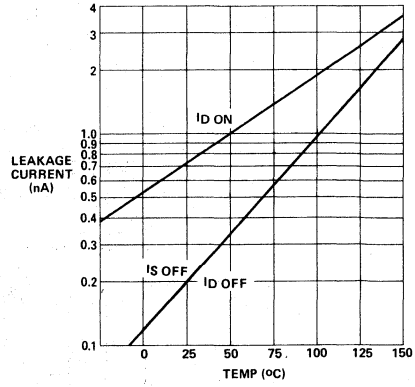


TEST CIRCUIT NO. 4*



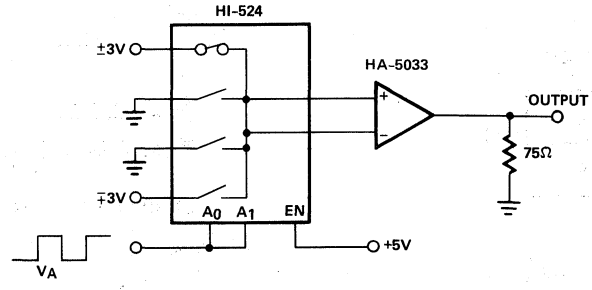
*Two measurements per channel:
+10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$:
+10V/-10V and -10V/+10V.)

LEAKAGE CURRENT VS. TEMPERATURE

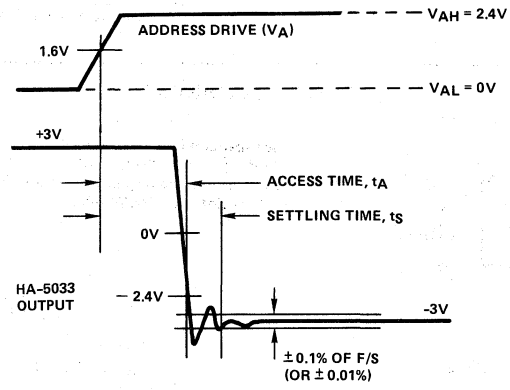


TEST CIRCUIT NO. 5

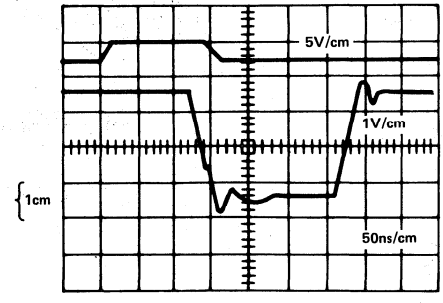
SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY



(USE DIFFERENTIAL COMPARATOR PLUG-IN ON SCOPE FOR SETTLING TIME MEASUREMENT.)

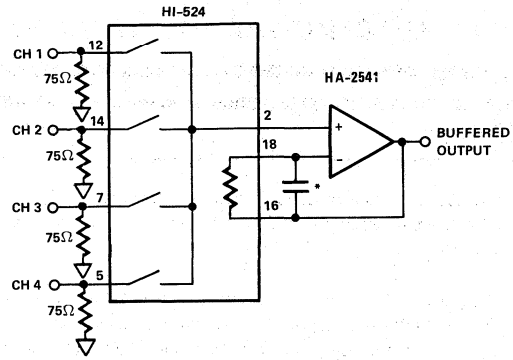


ACCESS TIME



APPLICATIONS

- Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* APPROXIMATELY 10pF SHOULD REMOVE ANY LOW LEVEL INSTABILITY AT THE OUTPUT.

- The main requirement for the buffer amplifier is a full power bandwidth high enough to avoid attenuation of the video signal. The Harris HA-5033 is well suited for this purpose, but where "ON" resistance "tracking" is critical, the differential HA-2541 or HA-5190 may be preferable. The 524/5033 combination offers a 3dB bandwidth per specification, while the 524/2541 comes close to this performance plus makes use of the 524 feedback element (as shown) to match and track the channel "ON" resistance.

- Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

- All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best Crosstalk performance.

- Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

- If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

DIE CHARACTERISTICS

Transistor Count		286
Die Size		146 x 88.6 mils
Thermal Constants	θ_{ja}	80°C/W
	θ_{jc}	22°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HARRIS

HI-539

Monolithic, Four Channel, Low Level, Differential Multiplexer

FEATURES

- DIFFERENTIAL PERFORMANCE, TYP.:
  - LOW ΔR_{ON}, +125°C — 5.5Ω
  - LOW $\Delta I_{D(ON)}$, +125°C — 0.6nA
  - LOW Δ(CHARGE INJECTION) — 0.1pC
  - LOW CROSSTALK — -120dB
- SETTLING TIME, ±0.01% — 900ns
- WIDE SUPPLY RANGE — ±5V TO ±18V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- LOW LEVEL DATA ACQUISITION
- PRECISION INSTRUMENTATION
- TEST SYSTEMS

DESCRIPTION

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

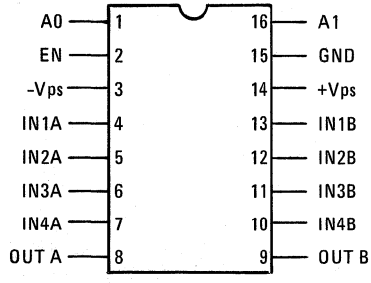
Performance is guaranteed for each channel over the range ± 10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero for zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

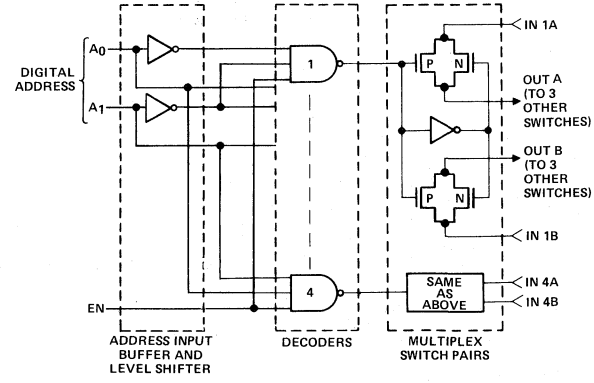
The HI-539 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. Supply voltages are ± 15V and power consumption is only 2.5mW. The package is a 16 pin ceramic DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between Supply Pins (V_{ps+}, V_{ps-})	40V	Internal Power Dissipation*	725mW
Voltage from either Supply to Ground	20V	Operating Temperature Range	
Analog Input Voltage, V_S	$V_{ps-} \leq V_S \leq V_{ps+}$	HI-539-2, -8	-55°C to +125°C
Digital Input Voltage, V_A	$V_{ps-} \leq V_A \leq V_{ps+}$	HI-539-4	-25°C to +85°C
		HI-539-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C	*Derate 9.6mW/°C above T_A = 95°C	

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = ± 15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the Performance Characteristics Section for test circuits and conditions. Selected parameters are defined in the Definitions Section.

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
ANALOG CHANNEL CHARA'S						
V_S, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50	200	50	200	pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10	100	10	100	pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage	+25°C	0.02	0.04	0.02	0.04	μV
	Full	0.70	10	0.08	1.0	μV

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full	450	1,000	450	1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crosstalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.5		2.5		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
± V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES

1. See Test Circuits #2, 3, 4. The condition ±10V means:

   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)

   $I_{D(ON)}$: (+10V, then -10V)

2. ΔV_{OS} (Exclusive of thermocouple effects) = $R_{ON}\ \Delta I_{D(ON)} + I_{D(ON)}\ \Delta R_{ON}$.

   See Applications section for discussion of additional V_{OS} error.

3. V_{IN} = 1kHz, $15V_{p-p}$ on all but the selected channel. See Test Circuit #9.

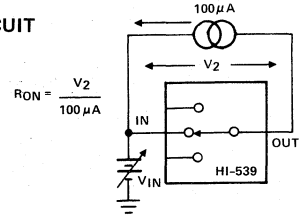
4. Calculated from typical Single-Ended Crosstalk performance.

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

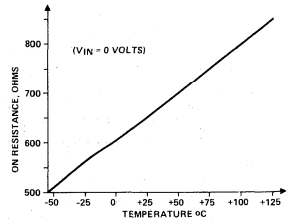
(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ± 15V, V_{AH} = +4V AND V_{AL} = +0.8V)

ON RESISTANCE MEASUREMENT

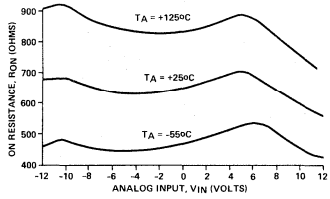
TEST CIRCUIT NO. 1



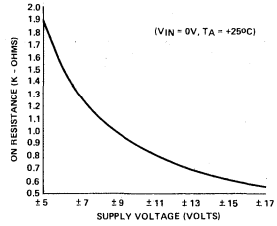
ON RESISTANCE vs. TEMPERATURE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE

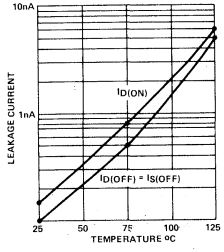


NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

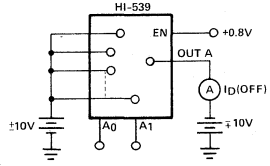


LEAKAGE CURRENT

LEAKAGE CURRENT vs. TEMPERATURE

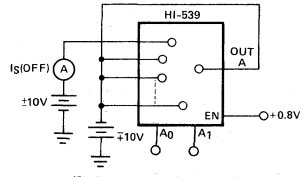


TEST CIRCUIT NO. 2*



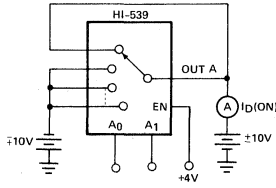
(Similar connections for side "B")

TEST CIRCUIT NO. 3*



(Similar connections for side "B")

TEST CIRCUIT NO. 4*



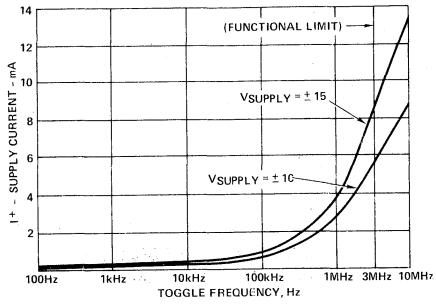
(Similar connections for side "B")

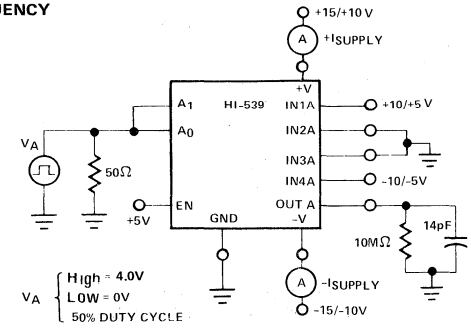
***Three measurements = +10V/-10V, -10V/+10V, and 0V**

TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 5

SUPPLY CURRENT vs. TOGGLE FREQUENCY

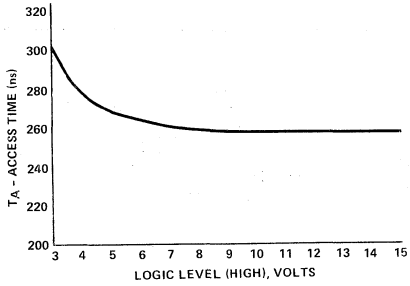


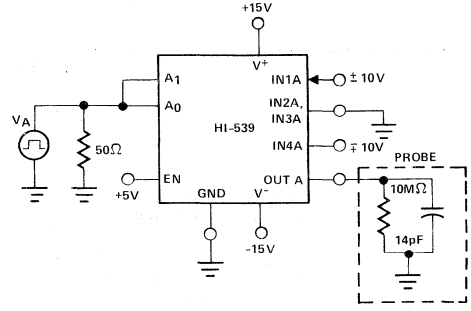


(SIMILAR CONNECTIONS FOR "B" SIDE)

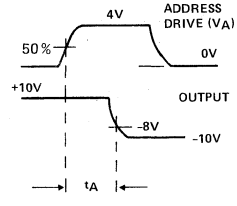
TEST CIRCUIT NO. 6

ACCESS TIME vs. LOGIC LEVEL (HIGH)

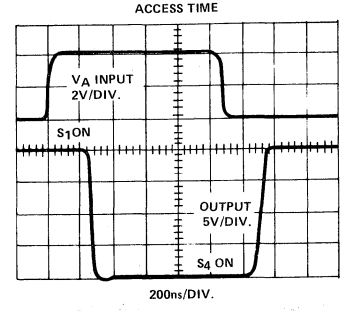




(SIMILAR CONNECTIONS FOR "B" SIDE)



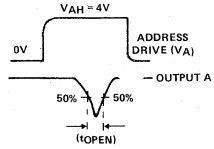
Example: t_A for 4V logic level



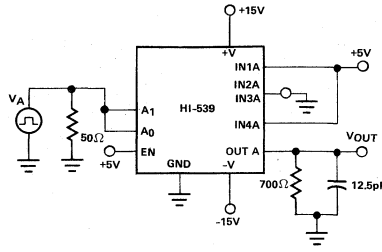
TEST CIRCUITS (Continued)

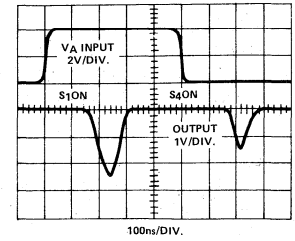
TEST CIRCUIT NO. 7

ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})

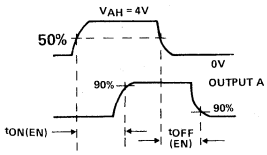




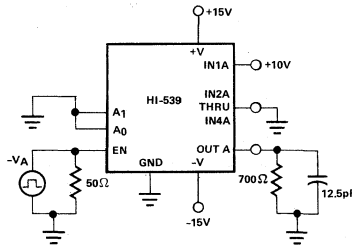
(SIMILAR CONNECTION FOR "B" SIDE)

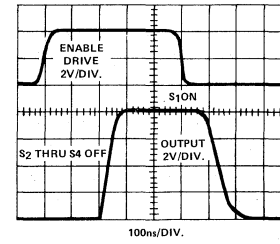
TEST CIRCUIT NO. 8

ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

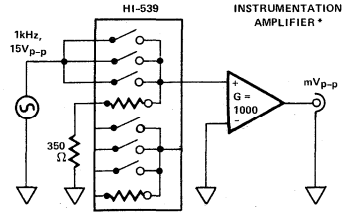




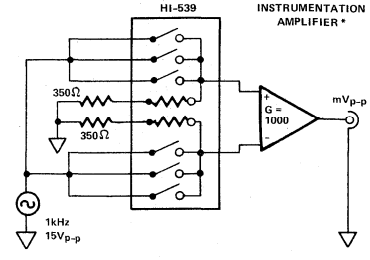
(SIMILAR CONNECTION FOR "B" SIDE)

TEST CIRCUIT NO. 9

SINGLE-ENDED CROSSTALK



DIFFERENTIAL CROSSTALK



* AD606 OR BB3630, FOR EXAMPLE

DEFINITIONS

CHARGE INJECTION – Charge (in pC) transferred, during a transition between channels, through the internal gate-to-channel capacitance. The resulting voltage error varies inversely with the output (or input) capacitance.

CROSSTALK – Signal at the multiplexer output, coupling though the C_{DS} capacitance of an OFF channel. Amplitude is proportional to source resistance for the ON channel. See Test Circuit # 9 for single-ended and differential versions of crosstalk.

DIFFERENTIAL LEAKAGE CURRENT ($\Delta I_{S(OFF)}$, $\Delta I_{D(OFF)}$, $\Delta I_{D(ON)}$) – The absolute difference in leakage for the two sides of a channel.

DIFFERENTIAL OFFSET VOLTAGE (ΔV_{OS}) – Voltage between the multiplexer output terminals with both channel input terminals shorted to ground.

DIFFERENTIAL ON RESISTANCE (ΔR_{ON}) – The absolute difference in On Resistance for the two sides of a channel.

INPUT TO OUTPUT CAPACITANCE (C_{DS}) – Capacitance from one input terminal of a channel to the corresponding output of the multiplexer. This parameter is responsible for Crosstalk.

APPLICATIONS

GENERAL

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential, especially to maintain a noise level below 50 μVrms.

LOW LEVEL SIGNAL TRANSMISSION

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Table 1

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu.)	D.C. RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

WATCH SMALL ΔV ERRORS

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12 bit converter system with an allowable error of ±1/2 LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

PROVIDE PATH FOR I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 1A, and consequently the amplifer output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 1B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

DIFFERENTIAL OFFSET, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part, due to the expression $(R_{ON}\,\Delta I_D(ON) + I_D(ON)\,\Delta R_{ON})$ becomes significant with increasing temperature, as shown in the Electrical Characteristics section. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

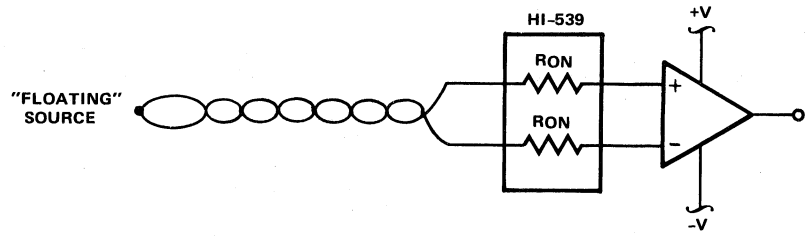


Figure 1A

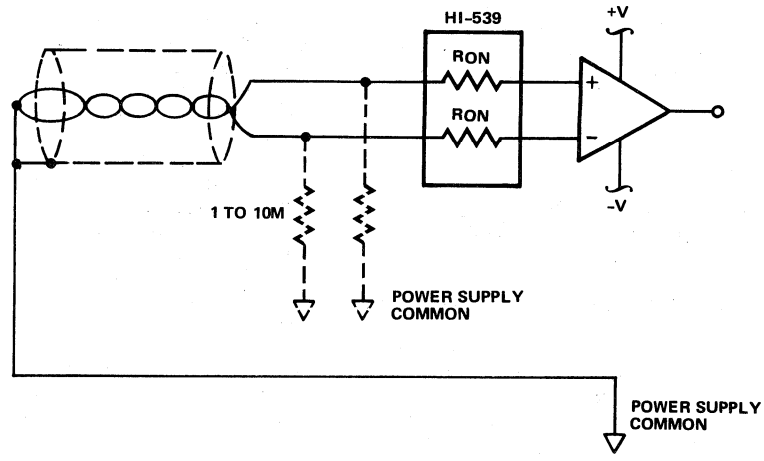


Figure 1B

The amplifier in Figure 1A is unusable because its bias currents cannot return to the power supply. Figure 1B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

DIE CHARACTERISTICS

Transistor Count		236
Die Size		92 x 100 mils
Thermal Constants	θ_{ja}	79°C/W
	θ_{jc}	26°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HI-1818A/1828A

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

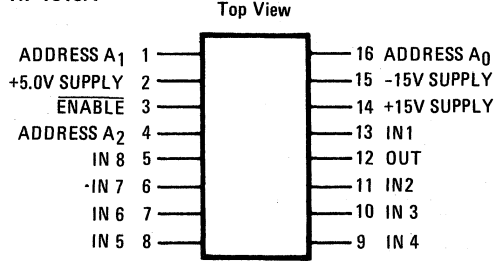
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A/1828A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT

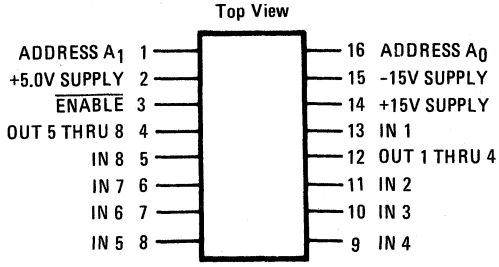
HI-1818A

Top View



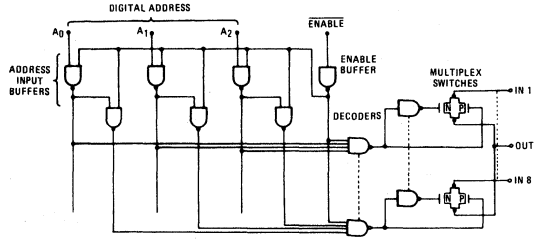
HI-1828A

Top View

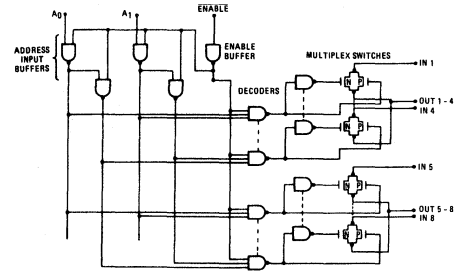


FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15 40.0V
Logic Supply Voltage, Pin 2 30.0V
Analog Input Voltage: V^+_{Supply} +2V
V^-_{Supply} -2V

Digital Input Voltage V-Supply to V+ Supply
Total Power Dissipation (Note 2) 750mW
Storage Temperature Range -65°C to +150°C

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
I_A, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_A, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
*I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
*I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
*I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 12.3mW/°C above 110°C.
3. $V_{OUT} = \pm 10V$, $I_{OUT} = -1mA$.
4. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; $V_{OUT} = -5.0V$ to +5.0V, Digital Inputs = 0V to +4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = +4.0V.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A

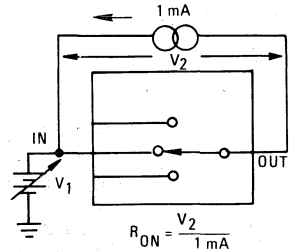
ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

DIE CHARACTERISTICS

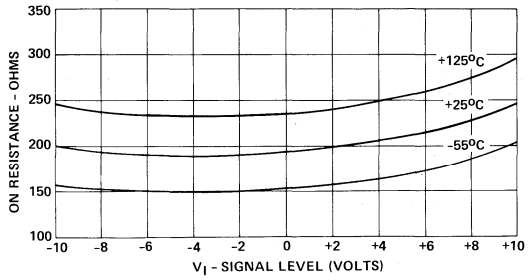
Transistor Count		210
Die Size		68.5 x 104 mils
Thermal Constants	θ_{ja}	90°C/W
	θ_{jc}	36°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

PERFORMANCE CHARACTERISTICS

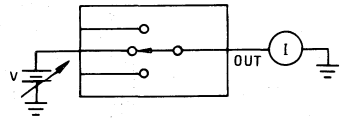
ON RESISTANCE vs. ANALOG SIGNAL LEVEL



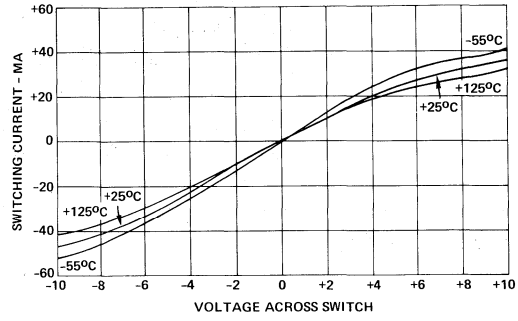
Test Circuit



ON CHANNEL CURRENT vs. VOLTAGE

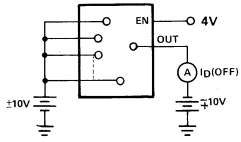


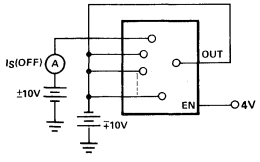
Test Circuit



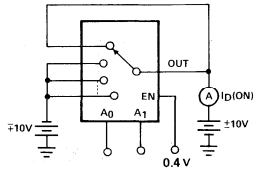
LEAKAGE CURRENTS vs. TEMPERATURE

OFF LEAKAGE

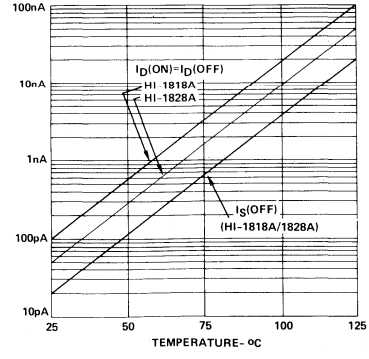




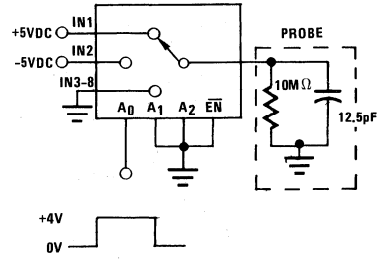
ON LEAKAGE

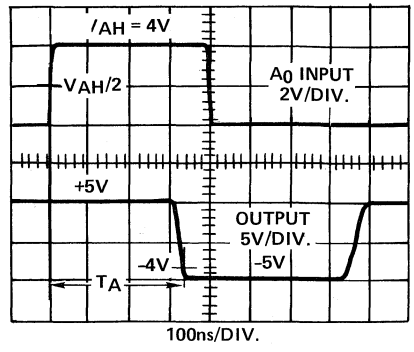


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V).



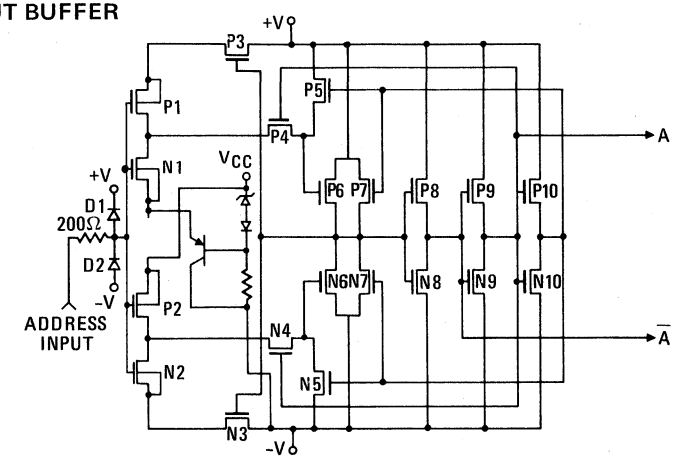
ACCESS TIME





SCHEMATIC DIAGRAM

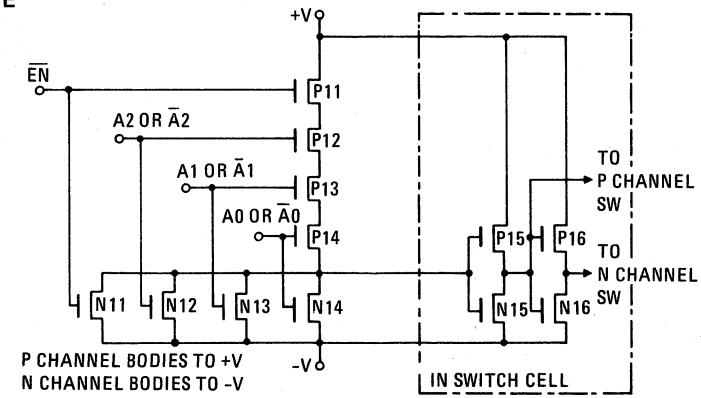
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

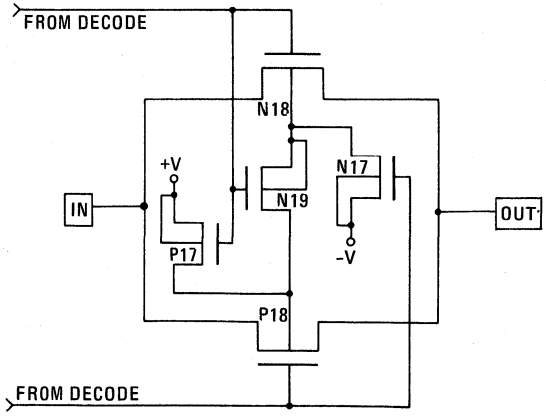
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

DECODER GATE



A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



ANALOG Analog-to-Digital Converters 5

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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Selection Guide

A/D CONVERTERS

	Part Number	Resolution Bits	Temperature Range	Package	Non-linearity, Max. 25°C (LSB)	Differential Non-Linearity Max. 25°C	Gain Drift ppm/°C Max. Full Temp	Conversion Speed (μs) (Internal Clock) Max. 12 Bits	10 Bits	8 Bits	Page
	HI5-5712-2	12	Mil	40 Pin Ceramic	±1	±1 LSB	±20	10.0	8.5	7.0	5-28
	HI5-5712-5		Com		±1	±1 LSB	±20				
	HI5-5712A-2		Mil		±1/2	±1/2 LSB	±10				
	HI5-5712A-5		Com		±1/2	±1/2 LSB	±10				
	HI-574AJD	12	Com	28 Pin Cerdip	±1	11 Bits*	±45	25	N/A	17.0	5-5
	HI-574AKD		Com		±1/2	12 Bits*	±25				
	HI-574ALD		Com		±1/2	12 Bits*	±10				
	HI-574ASD		Mil		±1	11 Bits*	±50				
	HI-574ATD		Mil		±1/2	12 Bits*	±25				
	HI-574AUD		Mil		±1/2	12 Bits*	±12.5				
	HI-674AJD	12	Com	28 Pin Cerdip	±1	11 Bits*	±50	15.0	N/A	10.0	5-16
	HI-674AKD		Com		±1/2	12 Bits*	±27				
	HI-674ALD		Com		±1/2	12 Bits*	±10				
	HI-674ASD		Mil		±1	11 Bits*	±50				
	HI-674ATD		Mil		±1/2	12 Bits*	±25				
	HI-674AUD		Mil		±1/2	12 Bits*	±12.5				
ADVANCE	HI-774AJD	12	Com	28 Pin Cerdip	±1	11 Bits*	±45	7	N/A	4.8	5-27
ADVANCE	HI-774AKD		Com		±1/2	12 Bits*	±25				
ADVANCE	HI-774ALD		Com		±1/2	12 Bits*	±10				
ADVANCE	HI-774ASD		Mil		±1	11 Bits*	±50				
ADVANCE	HI-774ATD		Mil		±1/2	12 Bits*	±25				
ADVANCE	HI-774AUD		Mil		±1/2	12 Bits*	±12.5				

* Maximum resolution with no missing codes guaranteed.

HARRIS

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 25 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
  - GUARANTEES BREAK – BEFORE – MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- IMPROVED SECOND SOURCE FOR AD574A AND HS574
- ±12V TO ±15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

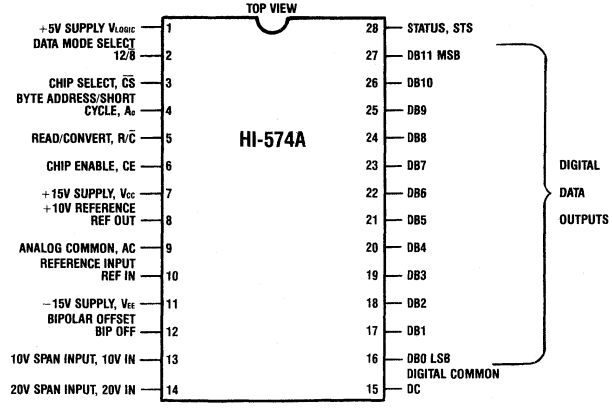
The HI-574A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ± 1 μs.

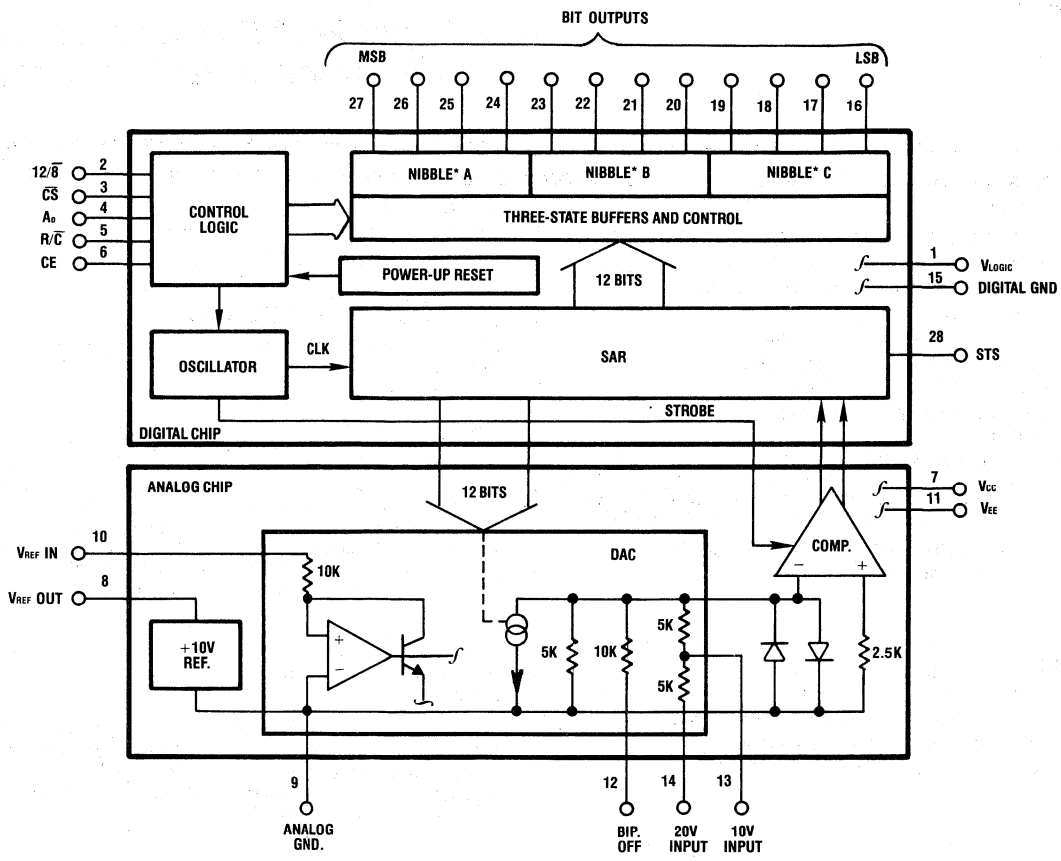
The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ± 12V to ± 15V, with typical dissipation of 515 mW. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix.

PINOUT



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.



("NIBBLE" IS A 4 BIT DIGITAL WORD.)

HI-574A BLOCK DIAGRAM

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5V$ or $-12.6V<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC}	11 TYP, 15 MAX			mA
I_{EE}	21 TYP, 28 MAX			mA
Power Dissipation	515 TYP, 720 MAX			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current,[1]	2.0 MAX			mA
available for external loads (External load should not change during conversion).				

1 When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-574AS	HI-574AT	HI-574AU	UNITS
Temperature Range		−55 TO +125		°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
−55°C to +125°C (max)	±1	±1	±1	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5V$ or $-12.6V<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar		−5 to +5		Volts
		−10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5K Ω, ± 25%		Ohms
20 Volt Span		10K Ω, ± 25%		Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+11.4 to +16.5		Volts
V_{EE}		−11.4 to −16.5		Volts
Operating Current				
I_{LOGIC}		7 TYP, 15 MAX		mA
I_{CC}		11 TYP, 15 MAX		mA
I_{EE}		21 TYP, 28 MAX		mA
Power Dissipation		515 TYP, 720 MAX		mW
Internal Reference Voltage		+10.00 ± 0.1 (MAX)		Volts
Output current,[1]		2.0 MAX		mA
available for external loads (External load				
should not change during conversion).				

1 When supplying an external load and operating on ± 12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to
Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) ..... 100°C
(S, T, U grades) ..... 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C
Thermal Resistance, Θ_{JA} ..... 48°C/W

HI-574A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-574AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-574ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574AUD-2	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-574AUD-8*	−55 to +125°C	±1 LSB	12 Bits	12.5

**Hi-Rel product with burn-in. For additional screening information, refer to Hi-Rel Section of current Analog catalog.*

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Ground) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

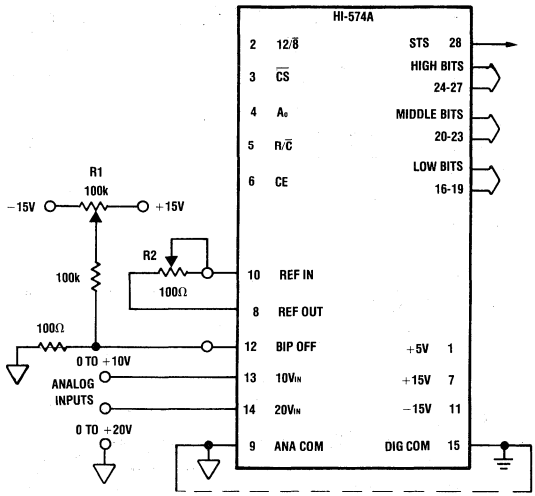


FIGURE 2. UNIPOLAR CONNECTIONS

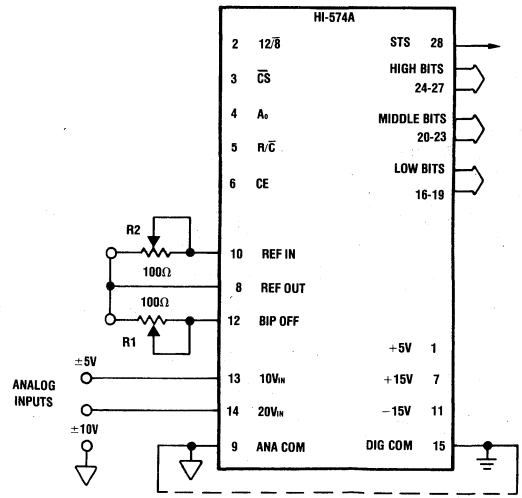


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A_0, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

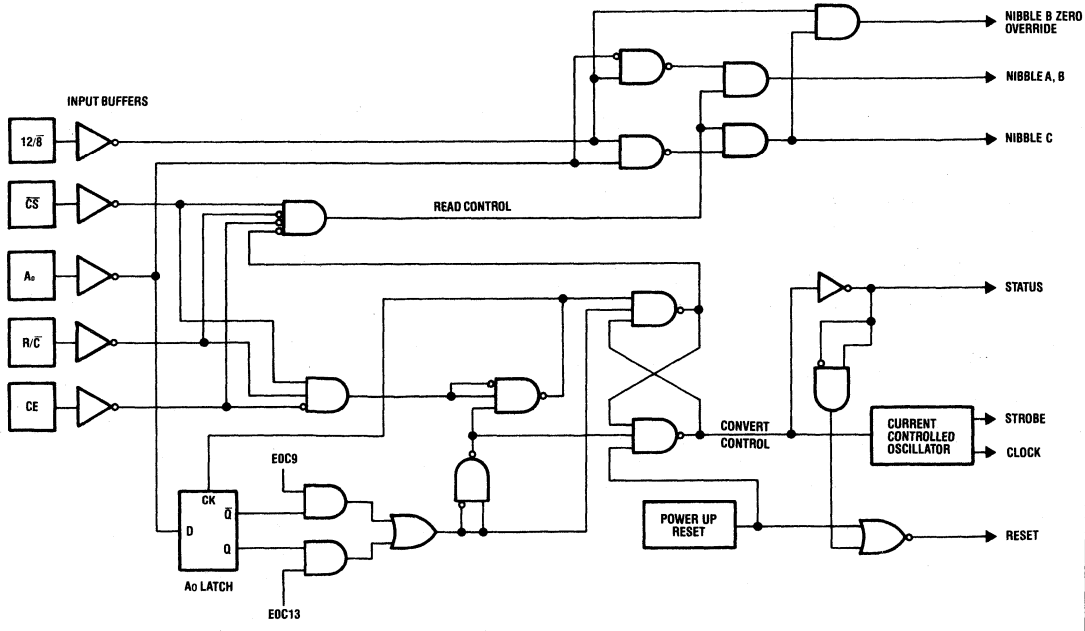


FIGURE 4. HI-574A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

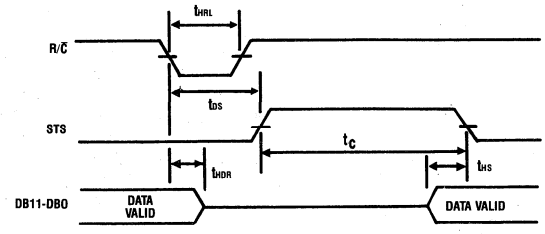


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

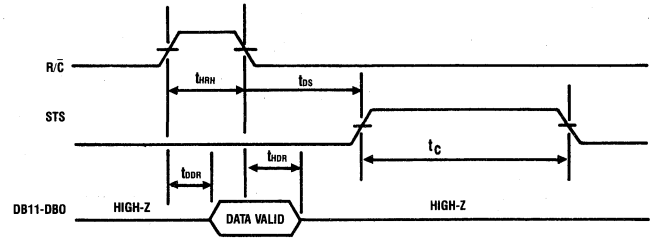


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB8 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-574A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

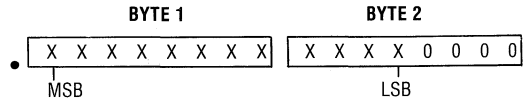
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 5 through 8 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

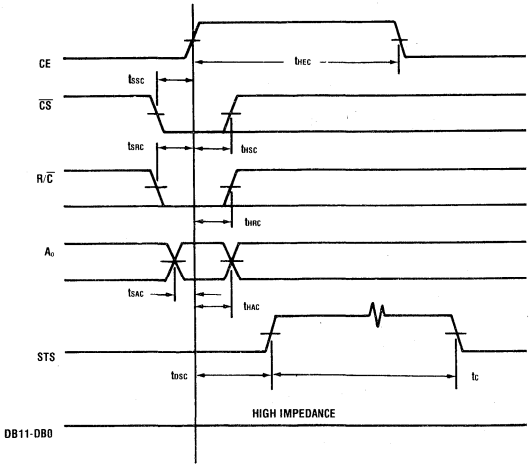


FIGURE 7. CONVERT START TIMING

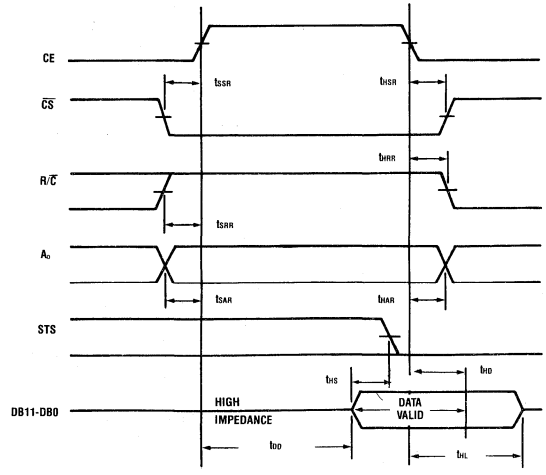


FIGURE 8. READ CYCLE TIMING

HI-574A TIMING SPECIFICATIONS
+25°C

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	nS
t_{HEC}	CE Pulse width	50	30		nS
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		nS
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50	20		nS
t_{SAC}	A_0 to CE Setup	0	0		nS
t_{HAC}	A_0 Valid during CE high	50	20		nS
t_C	Conversion time, 12 bit cycle	15	20	25	μS
	8 bit cycle	10	13	17	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25	35		nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nS
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nS
t_{SAR}	A_0 to CE setup	50	25		nS
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nS
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nS
t_{HAR}	A_0 valid after CE low	50	25		nS
t_{HS}	STS delay after data valid	300	500	1000	nS

Note: Time is measured from 50% level of digital transitions.

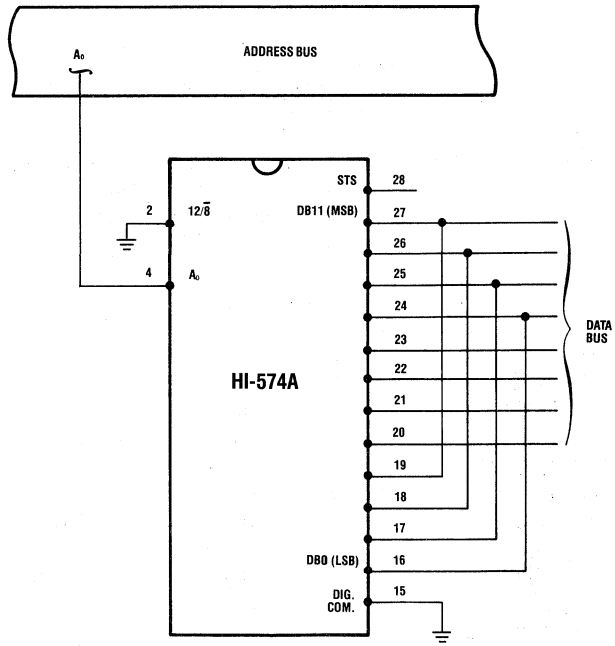


FIGURE 9 INTERFACE TO AN 8 BIT DATA BUS

DIE CHARACTERISTICS

Transistor Count		1117	Thermal Constants;	θja	48°C/W
Die Size:	Analog	204 x 104 mils		θjc	15°C/W
	Digital	158 x 84 mils	Process:		Bipolar – DI and CMOS – JI

HARRIS

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 15 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
  - GUARANTEES BREAK-BEFORE-MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- FASTER VERSION OF THE HI-574A.
- SAME PIN-OUTS AS HI-574A.
- ± 12V TO ± 15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

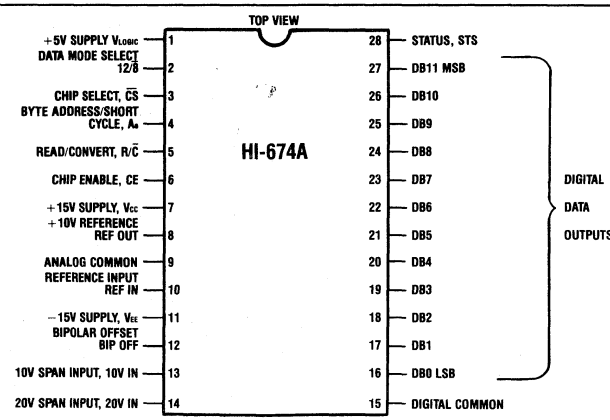
The HI-674A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1 μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

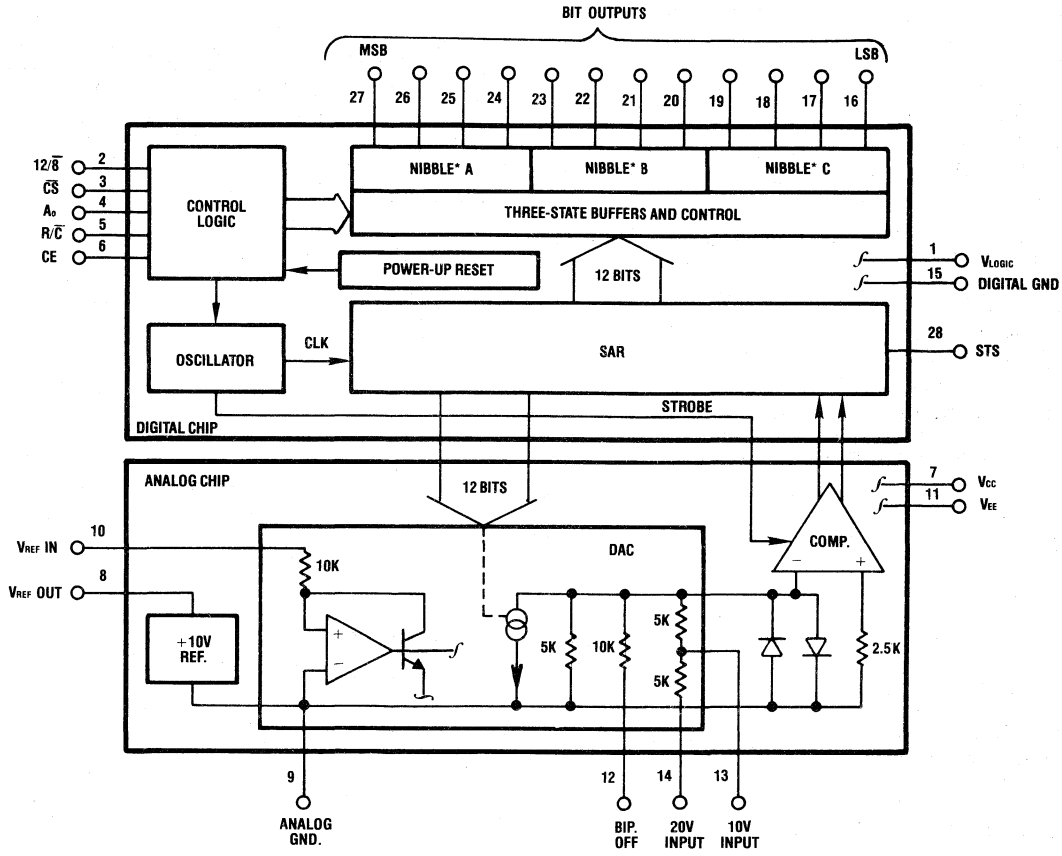
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 515mW. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For additional Hi-Rel screening including 160 hour burn-in, specify the "–8" suffix.

PINOUT



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

HI-674A BLOCK DIAGRAM



("NIBBLE" IS A 4 BIT DIGITAL WORD.)

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-674AJ	HI-674AK	HI-674AL	UNITS
Temperature Range		0 TO +75		°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar		−5 to +5		Volts
		−10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5K, ± 25%		Ohms
20 Volt Span		10K, ± 25%		Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+11.4 to +16.5		Volts
V_{EE}		−11.4 to −16.5		Volts
Operating Current				
I_{LOGIC}		7 TYP, 15 MAX		mA
I_{CC}		11 TYP, 15 MAX		mA
I_{EE}		21 TYP, 28 MAX		mA
Power Dissipation		515 TYP, 720 MAX		mW
Internal Reference Voltage		+10.00 ± 0.1 MAX		Volts
Output current,[1]		2.0 MAX		mA
available for external loads (External load should not change during conversion).				

1 When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-674AS	HI-674AT	HI-674AU	UNITS
Temperature Range	−55 TO +125			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
−55°C to +125°C (max)	±1	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC}	11 TYP, 15 MAX			mA
I_{EE}	21 TYP, 28 MAX			mA
Power Dissipation	515 TYP, 720 MAX			mW
Internal Reference Voltage	+10.00 ± 0.1 (MAX)			Volts
Output current,[1]	2.0 MAX			mA
available for external loads (External load should not change during conversion).				

1 When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to
Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) ..... 100°C
(S, T, U grades) ..... 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C
Thermal Resistance, Θ_{JA} ..... 48°C/W

HI-674A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-674AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-674AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-674ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-674ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-674ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-674AUD-2	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-674AUD-8*	−55 to +125°C	±1 LSB	12 Bits	12.5

*Hi-Rel product with burn-in. For additional screening information, refer to Section 9 of the current Analog data book.

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-674AK, AL, AT, and AU grades, which

DEFINITIONS OF SPECIFICATIONS (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-674A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 5.5mA DC into pin 9 (Analog Ground) and 7mA DC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15. Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA DC of current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-674A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950 nS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 850 nS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

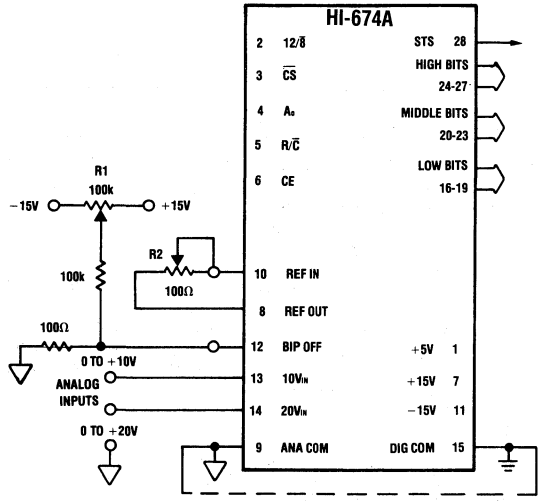


FIGURE 2. UNIPOLAR CONNECTIONS

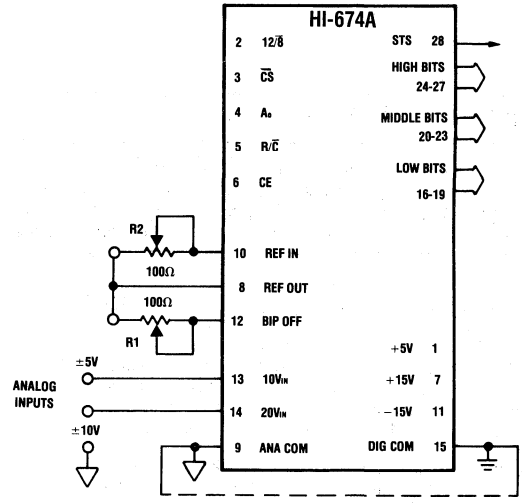


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-674A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A₀, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

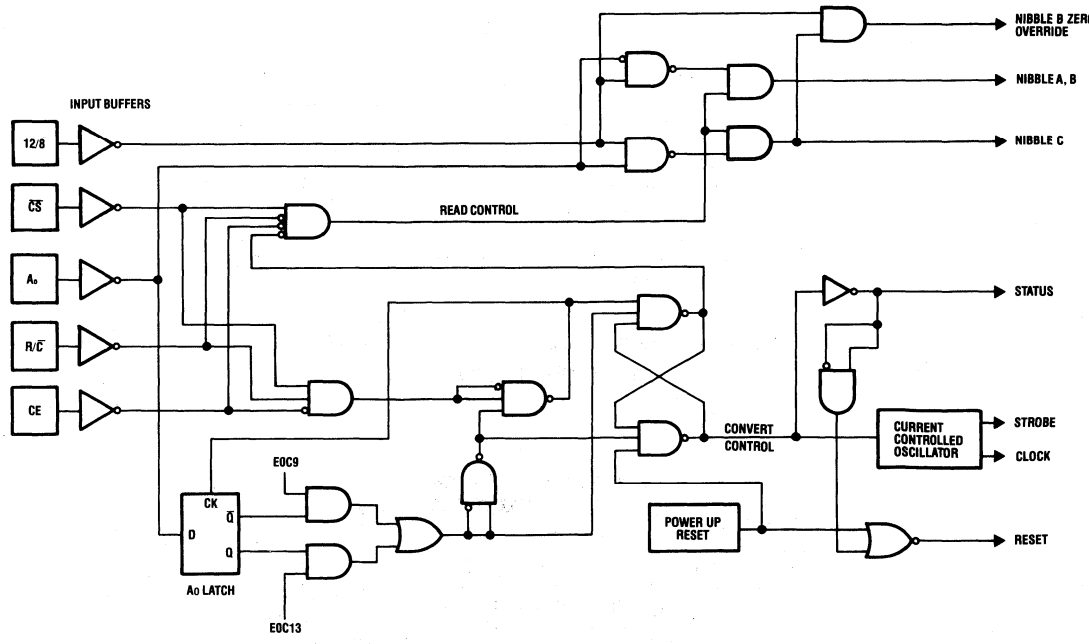


FIGURE 4. HI-674A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

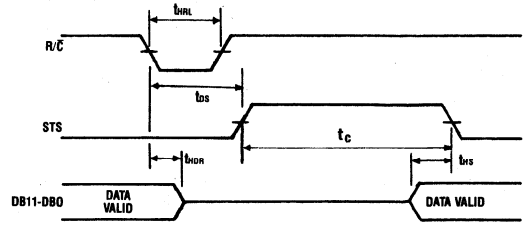


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

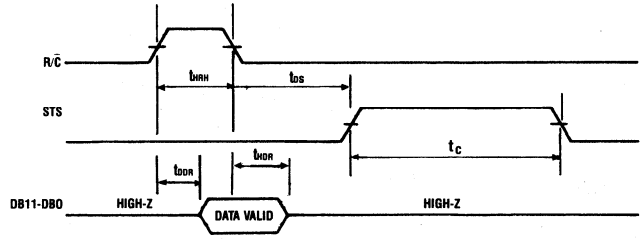


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$–OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB8 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1
Truth Table for HI-674A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-674A Timing Specifications, Convert mode.

This variety of HI-674A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

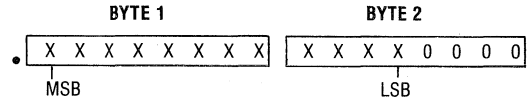
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-674A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 5 through 8 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

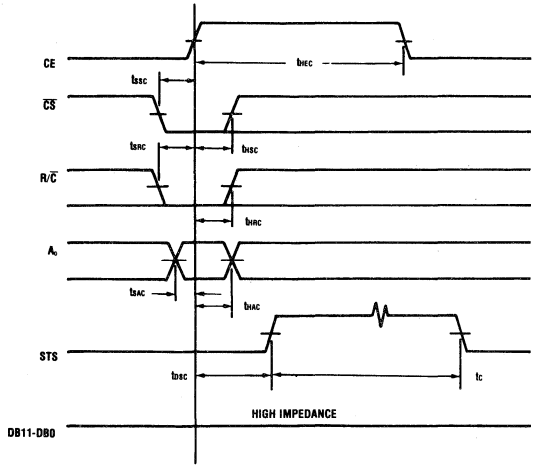


FIGURE 7. CONVERT START TIMING

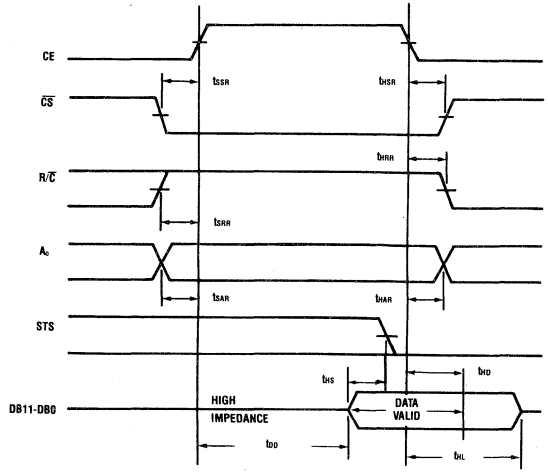


FIGURE 8. READ CYCLE TIMING

HI-674A TIMING SPECIFICATIONS

+25°C

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	nS
t_{HEC}	$\overline{CE}$ Pulse width	50	30		nS
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		nS
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50	20		nS
t_{SAC}	A_0 to CE Setup	0	0		nS
t_{HAC}	A_0 Valid during CE high	50	20		nS
t_C	Conversion time, 12 bit cycle	9	12	15	μS
	8 bit cycle	6	8	10	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25	35		nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nS
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nS
t_{SAR}	A_0 to CE setup	50	25		nS
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nS
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nS
t_{HAR}	A_0 valid after CE low	50	25		nS
t_{HS}	STS delay after data valid	100	300	600	nS

Note: Time is measured from 50% level of digital transitions.

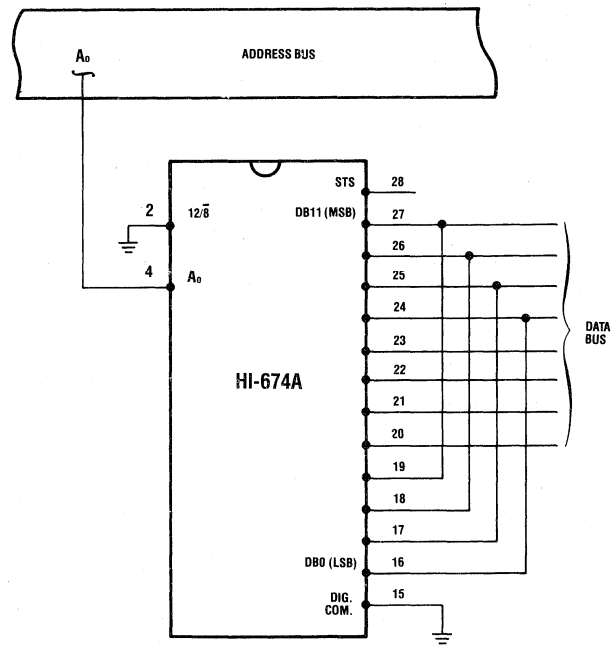


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

Die Characteristics

Transistor Count	1117	Thermal Constants; θ_{ja}	48°C/W
Die Size; Analog	204 x 104 mils	θ_{jc}	15°C/W
Digital	158 x 84 mils	Process	Bipolar-DI
			CMOS-JI

HARRIS

ADVANCE

HI-774A

6μ Sec., Complete 12-Bit Analog to Digital Converter with Microprocessor Interface

FEATURES

- FAST SUCCESSIVE APPROXIMATION CONVERSION 6μs
- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE AND CLOCK
- FULL 8 OR 16-BIT μP INTERFACE
- NO MISSING CODES OVER TEMPERATURE
- LOW GAIN T.C. 10ppm/°C
- PIN COMPATIBLE WITH THE HI-674A AND HI-574A

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- MILITARY AND INDUSTRIAL SYSTEMS

DESCRIPTION

The high speed HI-774A is a 12-bit A/D Converter, pin compatible with "Industry Standard" HI-574A's and the Harris' HI-674A. It includes a low noise +10V reference, stable clock, three-state outputs and a digital interface for microprocessor control, and consists of two monolithic chips housed in a single 28 lead DIP.

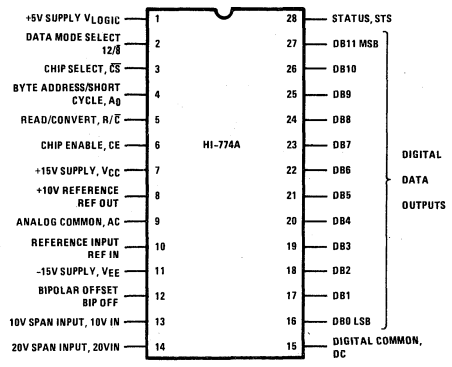
The HI-774A's SAJI CMOS chip includes the Harris SSAR™ which speeds the conversion by avoiding unnecessary settling time between bit decisions. This chip, with its digitally self-correcting successive-approximation register, is supported by analog functions (DAC, reference and comparator) on a bipolar chip utilizing Dielectric Isolation to provide speed and freedom from latch-up.

The HI-774A offers standard unipolar and bipolar input ranges. Twelve-bit accuracy is achieved by laser trimming for linearity, offset and gain. In addition, the internal transition noise is the lowest available, thanks to an improved zener reference and the use of current mode logic for transmission of digital signals between the chips.

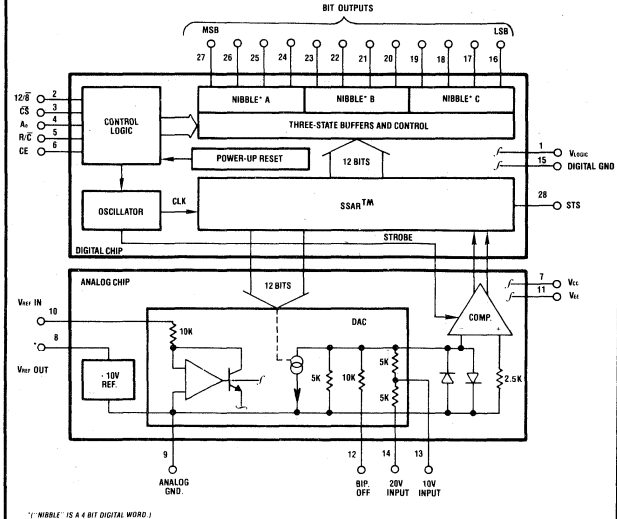
Power requirements are +5V and ±15V with typical dissipation of 565mW. The HI-774A is offered in both commercial and military grades. For additional Hi-Rel screening including a 160 hour burn-in, specify the "-8" suffix.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

HI-774A BLOCK DIAGRAM

HI-5712/5712A

High Performance 12 Bit Analog to Digital Converter

HARRIS

Not Recommended For New Designs See HI-674A, HI-774A, HI-5722

FEATURES

- MICROPROCESSOR COMPATIBLE
- CONVERSION TIME 10μsec MAX
- NO MISSING CODES OVER TEMPERATURE
- INTERNAL +10V REFERENCE
- INTERNAL CLOCK WITH EXTERNAL OVERRIDE CAPABILITY
- SERIAL OUTPUT
- TTL/CMOS COMPATIBLE
- TRISTATE PARALLEL OUTPUTS
- 40 PIN DIP
- MIL-STD-883 PROCESSING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

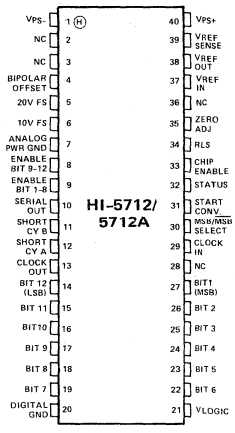
The HI-5712/5712A is a 12-bit successive approximation analog-to-digital converter (ADC) intended for high-speed, high-performance data conversion applications. An 8 μs conversion time for an accurate 12 bit conversion with low gain and offset temperature coefficients are among its many features. Numerous functions can be software controlled to meet a variety of ADC requirements.

The highly flexible input design accepts user programmed unipolar and bipolar inputs of: 0 to +10V, 0 to +20V, ±5V and ±10V full scale signal levels. The internal precision +10V reference delivers up to 10mA of output current with ultra high temperature stability. This reference is intended for biasing the ADC reference input, although other configurations can be implemented. A remote sense line is provided for applications requiring usage of the precision reference elsewhere in the system.

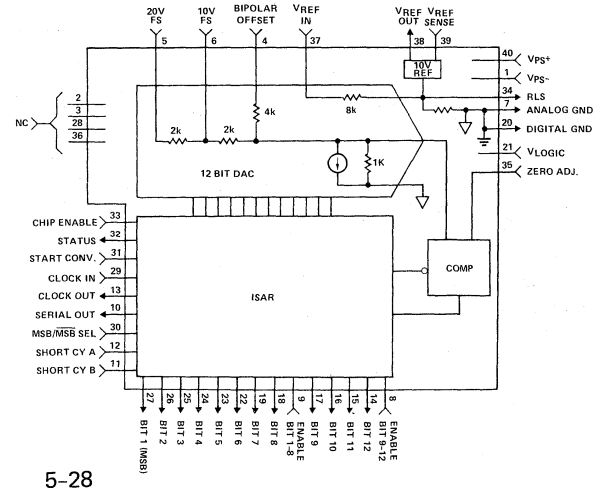
The output code select line and the short cycle control inputs are latched internally for microprocessor compatibility and provide selection of either binary or 2's complement output code, and resolution of 6, 8, 10, or 12 bits, respectively. A flexible interface is provided for 8, 12, and 16 bit systems via the chip select line and the word length control pins. The latter allows independent tri-state enabling of parallel output bits 1-8 and 9-12. A serial data output line is provided for applications requiring remote data transmission.

The HI-5712/5712A is manufactured with hermetically sealed leadless chip carriers (LCC's) mounted to both sides of a multi-layer ceramic substrate which results in a compact 40 pin dual-in-line package. The HI-5712A is intended for military, industrial and instrumentation applications. High reliability, military and commercial grades, are both available as standard products. For further information see Application Notes numbers 524, 528, 529, and 530.

PINOUT



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Power Supply Inputs		Power Dissipation (Pd) 2 Watts	
V_{PS}^+	+20V	Operating Temperature Range	
V_{PS}^-	-20V	HI-5712-2, HI-5712A-2	55°C to +125°C
V_{LOGIC}	+10V	HI-5712-5, HI-5712A-5	0°C to +75°C
V_{REF} IN (Pin 37)	0V, V_{PS}^+		
V_{REF} SENSE (Pin 39)	0V, V_{PS}^+	HI-5712-8, HI-5712A-8	-55°C to +125°C (Hi Rel)
Digital Inputs	-1V, V_{LOGIC}	Storage Temperature Range	65°C to +150°C

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{PS} = +15V, V_{PS}^- = -15V, V_{LOGIC} = +5V, V_{REF} In = Internal V_{REF}, Full Scale = +10V, Conversion Speed = 9 μs TYP (Internal Clock), 12-BIT Conversion, Unless otherwise noted.)

			HI-5712A-2 HI-5712-2 HI-5712A-8 HI-5712-8			HI-5712A-5 HI-5712-5			
PARAMETER		TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		Full			12			12	BITS
NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±3/4		±1/2	±3/4	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
DIFFERENTIAL NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±3/4		±1/2	±3/4	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							
INHERENT QUANTIZATION ERROR		Full			±1/2			±1/2	LSB
UNIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
BIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
GAIN ERROR (note 2) (Adjustable to Zero)		+25°C		.1	.3		.1	.3	%FSR
ADJUSTMENT RANGE									
UNIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
BIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
GAIN		+25°C			.3			.3	%FSR
TEMPERATURE STABILITY (With Internal V_{REF})									
UNIPOLAR OFFSET DRIFT	HI-5712A	Full		±2	±5		±2	±5	ppm FSR/°C
	HI-5712	Full		±4	±15		±4	±15	ppm FSR/°C
BIPOLAR OFFSET DRIFT	HI-5712A	Full		±4	±10		±4	±10	ppm FSR/°C
	HI-5712	Full		±8	±25		±8	±25	ppm FSR/°C
GAIN DRIFT	HI-5712A	Full		±5	±10		±5	±10	ppm FSR/°C
	HI-5712	Full		±10	±20		±10	±20	ppm FSR/°C
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5 HI-5712-5 MIN	TYP	MAX	UNITS
CONVERSION SPEED (Internal Clock)								
12 BIT	+25°C		9.0	10.0		9.0	10.0	μs
10 BIT	"		6.8	8.5		6.8	8.5	μs
8 BIT	"		5.6	7.0		5.6	7.0	μs
6 BIT	"		4.4	5.4		4.4	5.4	μs
MAXIMUM CONVERSION SPEED AT 12 BITS WITH EXTERNAL CLOCK (Note 3)	Full		6.5			6.5		μs
ANALOG INPUT CHARACTERISTICS								
INPUT VOLTAGE RANGE								
UNIPOLAR	Full	10			10			V
	Full	20			20			V
BIPOLAR	Full	±5	±5		±5	±5		V
	Full	±10	±10		±10	±10		V
INPUT IMPEDANCE								
10V FS (PIN 6)	Full	1.6	2	2.4	1.6	2	2.4	KΩ
20V FS (PIN 5)	Full	3.2	4	4.8	3.2	4	4.8	KΩ
V_{REF} IN (PIN 37)	Full	6.4	8	9.6	6.4	8	9.6	KΩ
ANALOG OUTPUT CHARACTERISTICS								
V_{REF} OUTPUT VOLTAGE	+25°C	9.970	10.000	10.030	9.970	10.000	10.030	V
V_{REF} OUTPUT CURRENT	Full	10			10			mA
VREF OUTPUT TC HI-5712A	Full		±10	±15		±10	±15	ppm FSR/°C
VREF OUTPUT TC HI-5712	Full		±10	±15		±10	±15	ppm FSR/°C
DIGITAL INPUT CHARACTERISTICS								
INPUT VOLTAGE (Note 8)								
LOGIC 1	Full	3.3	2.7		3.3	2.7		V
LOGIC 0	Full		1.2	.8		1.2	.8	V
INPUT CURRENT (Note 8)								
LOGIC 1 (VCC)	Full	-25	0	+25	-25	0	+25	μA
LOGIC 0 (GND)	Full		-200	-400		-200	-400	μA
EXTERNAL CLOCK (Note 3)	Full			2.5			2.5	MHz
DIGITAL OUTPUT CHARACTERISTICS								
OUTPUT VOLTAGE								
LOGIC 1 I_{OH} = -800μA	Full	3.5	4.0		3.5	4.0		V
LOGIC 0 I_{OL} = +3.2mA	Full		.2	.4		.2	.4	V
OUTPUT CURRENT								
LOGIC 1 VO = 3.5V	Full	-800	-1000		-800	-1000		μA
LOGIC 0 VO = .4V	Full	3.2	4.0		3.2	4.0		mA
DIGITAL INPUT TIMING CHARACTERISTICS								
CHIP ENABLE TO START CONVERT t_{cd}	Full	50			50			nsec
START CONVERT PULSE LOW t_{scl}	Full	100			100			nsec
START CONVERT PULSE HIGH t_{sch}	Full	50			50			nsec
CONTROL SETUP TIME t_s	Full	100			100			nsec
CONTROL HOLD TIME t_h	Full	100			100			nsec
CLOCK INPUT LOW t_{pwl}	Full	125			125			nsec
CLOCK INPUT HIGH t_{pwh}	Full	150			150			nsec
CLOCK INPUT PERIOD t_{cl}	Full	400			400			nsec
ENABLE 1-8, 9-12 PULSE WIDTH t_{em}	Full	100			100			nsec

SPECIFICATIONS (Continued)

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5 HI-5712-5 MIN	TYP	MAX	UNITS
DIGITAL OUTPUT TIMING CHARACTERISTICS								
THREE STATE ENABLE DELAY t_{oe}	Full		40	50		40	50	nsec
THREE STATE DISABLE DELAY t_{od}	Full		60	100		60	100	nsec
START CONVERT TO STATUS DELAY t_{sd}	Full		70	100		70	100	nsec
START CONVERT TO CLOCK OUT DELAY t_{scd}			200	500		200	500	nsec
CLOCK TO SERIAL OUT DELAY t_{psd}	Full	100	150	200	100	150	200	nsec
LAST CLOCK TO STATUS DELAY t_{scdt}	Full	50	75	100	50	75	100	nsec
PARALLEL DATA TO STATUS DELAY t_{ds}	Full	50	75		50	75		nsec
LAST SERIAL BIT TO STATUS DELAY t_{da}	Full	50	75		50	75		nsec
CLOCK INPUT TO CLOCK OUT DELAY t_{dcl}	Full		25	50		25	50	nsec
PARALLEL DATA OUTPUT CODES								
UNIPOLAR (Note 4)	Positive True Binary							
BIPOLAR (Note 4)	Positive True Offset Binary							
	Positive True Two's Complement Binary							
SERIAL DATA OUTPUT CODE	Positive True NRZ Code							
POWER SUPPLY REQUIREMENTS (Note 5)								
V_{ps+}	Full	+13.5	+15	+16.5	+13.5	+15	+16.5	V
V_{ps-}	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
V_{LOGIC}	Full	+4.5	+5	+5.5	+4.75	+5	+5.25	V
I_{ps+}	Full		27	35		27	35	mA
I_{ps-}	Full		42	50		42	50	mA
I_{LOGIC}	Full		4.5	15		4.5	15	mA
POWER SUPPLY SENSITIVITY (Note 6)								
V_{ps+} = +13.5V to +16.5V, V_{ps-} = -15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	ppm of FSR/ %ΔP.S.
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{ps-} = -13.5V to -16.5V, V_{ps+} = +15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{LOGIC} = +4.5V to +5.5V, V_{ps+} = +15V, V_{ps-} = -15V CONVERSION SPEED (12 Bit with Internal Clock)			±5	±10		±5	±10	%

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Figure 2 for connections. The initial errors are adjustable to zero by using external trim potentiometers as shown in Figure 3, and 4.
3. The HI-5712A will operate at these speeds (for 12 bit conversion), but parametric performance is not guaranteed.
4. See operating instructions for details.
5. After 60 seconds warm-up.
6. See definitions.
7. These terminals will be used in the future for additional functions. Do not make connections to these pins in your system.
8. TTL compatibility guaranteed.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{ps}-	-15V Power Supply Terminal
2	NC	No Connection See Note 7
3	NC	No Connection See Note 7
4	BIPOLAR OFFSET	Connect to V_{REF} for Bipolar Input Mode. See Operating Instructions for Details.
5	20V FS	20V Full Scale Analog Input
6	10V FS	10V Full Scale Analog Input
7	ANALOG GND	Analog Power Supply Return
8	ENABLE BIT 9-12	Output "Three State" Control. An Input "0" Enables Bits 9 through 12, whereas a "1" Switches these Bits to a High Impedance State.
9	ENABLE BIT 1-8	Output "Three State" Control. An Input "0" Enables Bits 1 through 8, whereas a "1" Switches these Bits to a High Impedance State.
10	SERIAL OUT	NRZ Serial Data Output. To be used in Conjunction with Clock Out for Remote Data Transmission
11	SHORT CY B	See Description for Pin 12
12	SHORT CY A	Digital Inputs Applied to short cycle A and B selects a conversion of 6, 8, 10, or 12-bits:

BITS	SHORT CY A	SHORT CY B
6	0	0
8	0	1
10	1	0
12	1	1

PIN	SYMBOL	DESCRIPTION
13	CLOCK OUT	SAR Clock Output. Used for Decoding Serial Out Data
14	BIT 12	Output Data Bit (LSB)
15	BIT 11	Output Data Bit
16	BIT 10	Output Data Bit
17	BIT 9	Output Data Bit
18	BIT 8	Output Data Bit
19	BIT 7	Output Data Bit
20	DIGITAL GND	Digital Power Supply Return
21	V_{LOGIC}	+5V Power Supply Terminal
22	BIT 6	Output Data Bit
23	BIT 5	Output Data Bit
24	BIT 4	Output Data Bit
25	BIT 3	Output Data Bit
26	BIT 2	Output Data Bit
27	BIT 1	Output Data Bit (MSB)
28	NC	No Connection. See Note 7.
29	CLOCK IN	An External Clock Signal Applied to this Input Overrides the Internal Clock.
30	MSB/$\overline{\text{MSB}}$ SEL	Digital Input Pin. A "1" Applied to this Terminal Selects a Straight Binary or Offset Binary Output Code. A "0" Inverts the MSB to Yield a 2's Complement Binary Output Code.
31	START CONV	Digital Input Pin. A High to Low Transition Initiates the ADC Conversion Cycle.
32	STATUS	Digital Output Pin. A "1" Indicates that the ADC is Busy, While a "0" Denotes that Conversion is Completed and Data is Ready for Retrieval.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
33	CHIP ENABLE	Digital Input Pin. A "1" Forces the Output Data, Serial Out and Status Terminals to a High Impedance State and the ADC is Disabled. A "0" Enables these ADC Functions.
34	RLS	Reference Low Sense.
35	ZERO ADJ	External Zero Adjustment Pin, See Operating Instructions for Details.

PIN	SYMBOL	DESCRIPTION
36	NC	No Connection. See Note 7.
37	V_{REF} IN	+10V Reference Input to ADC.
38	V_{REF} OUT	Internal +10V Reference Output, Normally Connected to V_{REF} IN (Pin 37).
39	V_{REF} SENSE	Internal +10V Reference Sensing Terminal, Normally connected to V_{REF} Out (Pin 38). See Operating Instructions for Details.
40	V_{ps+}	+15V Power Supply Terminal.

APPLYING THE HI-5712/5712A

OPERATING INSTRUCTIONS

Conventional ADC systems provide maximum performance when the analog and digital ground lines are tied together at the ADC terminals. This minimizes analog interference due to digital switching noise. For optimum performance, this external grounding procedure should be followed in HI-5712/5712A installations to reinforce the unit's internal analog-to-digital ground connections. Under no circumstances should the Reference Low Sense (RLS) terminal (Pin 34) be connected to system ground.

In practice, the Reference Low Sense (RLS) terminal (Pin 34) normally is connected to zero adjust (or error amplifier) input terminal (Pin 35), either directly or through an appropriate resistor network. See figures 3 and 4.

On the HI-5712/5712A substrate, the power supply lines to each active component are bypassed to ground with 0.01 μF chip capacitors for high frequency noise rejection. For best accuracy, the grounding and decoupling schemes shown in Figures 3 and 4 are recommended. The 10μF bypass capacitors shown should be connected as close as possible to the HI-5712/5712A, preferably at the device pin.

For applications where usage of potentiometers is highly undesirable, the trim pots shown in Figures 3 and 4 can either be deleted or replaced by precision fixed resistors. (Delete R_3 and R_4; replace R_1 with 25 ohms). When precision fixed resistors are used, the initial offset error and gain error contributions are as specified in page 2.

NOTE: The HI-5712/5712A may latch up if the device is enabled before applying power. Disabling the device following power turn on will remedy this situation. Care supplies do not excessively overshoot their final value during turn on.

CONTROL AND INTERFACE

The HI-5712/5712A features a versatile set of controlling functions which allows a wide variety of applications, including microprocessor bus interfacing.

When the chip enable is set to low, the internal registers are enabled, and the output data lines can be enabled via the output enable control lines. The conversion cycle is initiated at the falling edge of the start conversion pulse. At this time, the MSB/$\overline{\text{MSB}}$ Select, Short Cycle A, and Short Cycle B control information is latched into the internal registers. The status line is also forced into an active high state indicating that a conversion is taking place. At the end of the conversion cycle the status line will be set to low to signify that the data is ready at the tri-state buffers. The various timing relationships are shown in Figure 1.

There are two distinct modes of operation, namely, continuous conversion and single step conversion. Continuous conversion can be easily achieved by connecting the Status line to the Start Convert pin. In this application, an indecision state may occur during the initial power-on conditions. Normal operation is restored by pulsing the chip enable pin to logic high for a period greater than 100 ns.

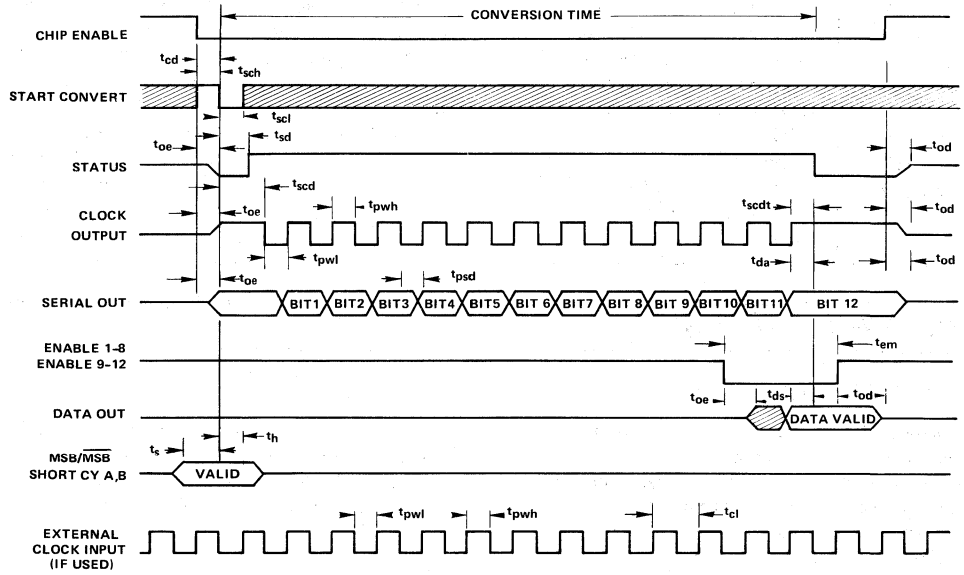


FIGURE 1. HI-5712/5712A TIMING DIAGRAM

REMOTE DATA TRANSMISSION

The Serial Data Out is mainly used for remote data transmission, where only a limited number of wires are available.

Serial Output is bit by bit (MSB first, LSB last) in a NRZ (nonreturn-to-zero) format. It changes state only at the positive going edges of the Clock Out, and remains valid during the whole clock period. Parallel data can be constructed by clocking the serial data into a receiving shift register.

In order to minimize transmission error, the negative-going edge of the clock should be used to clock data into the remote shift register. The parallel data will be valid once the status line returns to low. The clocking scheme is shown in Figure 1.

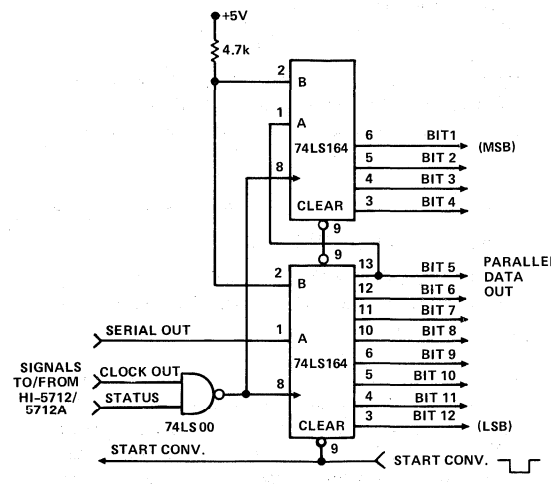


FIGURE 2. DECODING SERIAL DATA OUT

HI-5712/5712A CALIBRATION CHART

OPERATING MODE	ANALOG INPUT CONNECTION	R2 BIAS RESISTOR	MSB/$\overline{\text{MSB}}$ SELECT PIN 30	OFFSET ADJUST ANALOG INPUT VOLTAGE	ADJUST R3 FOR DITHER BETWEEN CODES	GAIN ADJUST ANALOG INPUT VOLTAGE	ADJUST R1 FOR DITHER BETWEEN CODES	LSB WEIGHT
UNIPOLAR STRAIGHT BINARY 0V to +10V	10VFS PIN 6	667Ω	HIGH	+1.22mV	0000 0000 0000 0000 0000 0001	+9.9963V	1111 1111 1110 1111 1111 1111	2.44mV
UNIPOLAR STRAIGHT BINARY 0V to +20V	20VFS PIN 5	800Ω	HIGH	+2.44mV	0000 0000 0000 0000 0000 0001	+19.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR OFFSET BINARY -5V to +5V	10VFS PIN 6	580Ω	HIGH	-4.9988V	0000 0000 0000 0000 0000 0001	+4.9963V	1111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR OFFSET BINARY -10V to +10V	20V FS PIN 5	667Ω	HIGH	-9.9976V	0000 0000 0000 0000 0000 0001	+9.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR 2's COMPLEMENT -5V to +5V	10V FS PIN 5	580Ω	LOW	-4.9988V	1000 0000 0000 1000 0000 0001	+4.9963V	0111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR 2's COMPLEMENT 10V to +10V	20V FS PIN 6	667Ω	LOW	-9.9976V	1000 0000 0000 1000 0000 0001	+9.9927V	0111 1111 1110 0111 1111 1111	4.88mV

CALIBRATION PROCEDURE- Refer to Calibration Chart and to Figures 3 and 4 for appropriate analog input connections, value of bias resistor, and MSB/$\overline{\text{MSB}}$ select.

STEP 1 OFFSET ADJUSTMENT

- Set analog input to the appropriate value for offset adjustment.
- Adjust R3 for dither between codes shown in calibration chart.

STEP 2 GAIN ADJUSTMENT

- Set analog input to the appropriate value for gain adjustment.
- Adjust R1 for dither between codes shown in calibration chart.

NOTE: This calibration procedure insures that the transfer characteristic produced by connecting the midpoints of all quantization intervals passes through the origin.

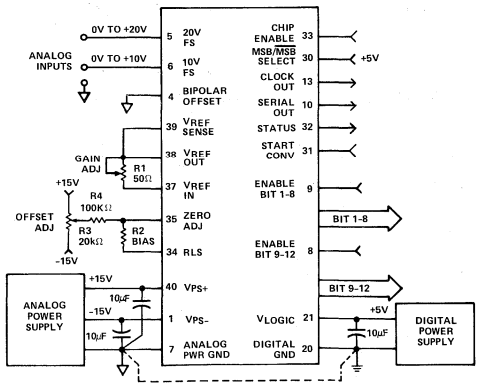


FIGURE 3. UNIPOLAR INPUT CONNECTIONS - STRAIGHT BINARY OUTPUT CODE

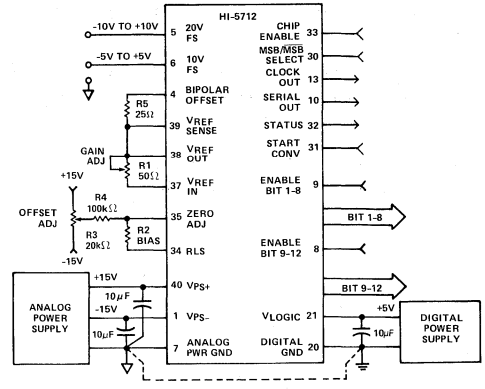


FIGURE 4. BIPOLAR INPUT CONNECTIONS

DEFINITIONS

Least Significant Bit (LSB) - The LSB of an Analog-to-Digital Converter (ADC) is defined to be the digital output bit carrying the lowest numerical weight ($\frac{1}{2}^n$); or the Analog input shift associated with this bit (FSR/2^n) which is the smallest possible Analog input step that can be resolved.

Most Significant Bit (MSB) - The Digital output bit carrying the highest numerical weight (½); or the Analog input shift associated with this bit. In a Binary ADC the MSB indicates the Analog input reaches its ½ FSR.

Resolution - An indication of the number of possible analog input levels an ADC will resolve. Usually it is expressed as the number of output bits. For example, a 12 bit Binary ADC can have 2^{12} = 4096 possible output codes and it has a resolution of 12 bits.

Nonlinearity (Linearity Error) - A measure of the deviation of each individual code from an ideal straight line transfer curve drawn between zero and full scale. The deviation of a code from the ideal straight line is measured from the middle of each particular code.

Code Width - A fundamental quantity for ADC specifications, it is defined as the range of Analog input values which produce a given digital output code. The ideal value of a code width is equivalent to FSR/2^n, where n is the number of bits.

Differential Nonlinearity - A measure of the deviation between the actual code width of an ADC from the ideal code width. A specification which guarantees no missing codes requires that every code must have a non-zero width.

Quantizing Error (or uncertainty) - The uncertainty introduced by partitioning the Analog continuum into 2^n discrete ranges for n-BIT conversion. The Analog values within a given quantum are normally assigned to the nominal midrange value, represented by the same digital code and therefore, a quantization uncertainty of $\pm$½ LSB is inherently associated with a given resolution.

Unipolar Offset Error - A measure of the difference between the ideal (+½LSB) and the actual analog input level required to produce the first output digital code transition (00- - -0 to 00- - -01). It is usually expressed in percent of full scale range (%FSR).

Bipolar Offset Error - A measure of the difference between the ideal (½FSR -½LSB) and the actual analog input level required to produce the major carry output digital code transition (from 011- - -0 to100- - -0). It is usually expressed in percent of full scale range (%FSR).

Gain Error - The gain of an ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2LSB. It is usually expressed in percent of full scale range (%FSR).

Unipolar Offset Drift - A measure of the change in unipolar offset over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Gain Drift - A measure of the change in gain (with offset error removed) over the specified termperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Bipolar Offset Drift - A measure of the change in bipolar offset over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Power Supply Sensitivity - A measure of the change in gain, offset, and conversion speed of the ADC resulting from a change in supply voltages. It is expressed in parts per million of full scale range per percent of change in power supply voltages (PPM of FSR/%).

Conversion Speed - The measure of how long it takes an ADC to arrive at the proper output code. It is the time between the edge of the digital command that starts conversion and the edge of the status line signal which signifies that the conversion is completed.

Throughput Rate - For SAR-Types, ADC's throughput rate is defined as the total number of conversions in a given time period. Usually, it is expressed in conversions per second although, the term Hertz is generally accepted.

HARRIS

HI-5722

High Performance 12 Bit Analog to Digital Converter

Preview Information This Product May be Discontinued or Changed Without Notice.

FEATURES

- MICROPROCESSOR COMPATIBLE
- CONVERSION TIME 10μsec MAX
- NO MISSING CODES OVER TEMPERATURE
- INTERNAL +10V REFERENCE
- INTERNAL CLOCK WITH EXTERNAL OVERRIDE CAPABILITY
- SERIAL OUTPUT
- TTL/COMS COMPATIBLE
- TRISTATE PARALLEL OUTPUTS
- 40 PIN DIP
- REPLACES THE HI-5712/5712A

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

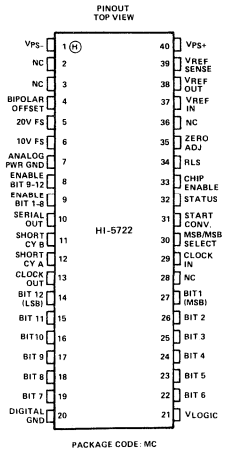
The HI-5722 is a 12-bit successive approximation analog-to-digital converter (ADC) intended for high-speed, high-performance data conversion applications. An 8μs conversion time with low gain and offset temperature coefficients are among its many features. Numerous functions can be software controlled to meet a variety of ADC requirements.

The highly flexible input design accepts user programmed unipolar and bipolar inputs of : 0 to +10V, 0 to +20V, ±5V and ±10V full scale signal levels. The internal precision +10V reference delivers up to 10mA of output current with ultra high temperature stability. This reference is intended for biasing the ADC reference input, although other configurations can be implemented. A remote sense line is provided for applications requiring use of the precision reference elsewhere in the system.

The output code select line and the short cycle control inputs are latched internally and provide selection of either binary or 2's complement output code, and resolution of 6, 8, 10 or 12 bits, respectively. A flexible interface is provided ifor 8, 12 and 16 bit systems via the chip select line and the word length control pins. The latter allows independent tri-state enabling of parallel output bits 1-8 and 9-12. A serial data output line is provided for applications requiring remote data transmission.

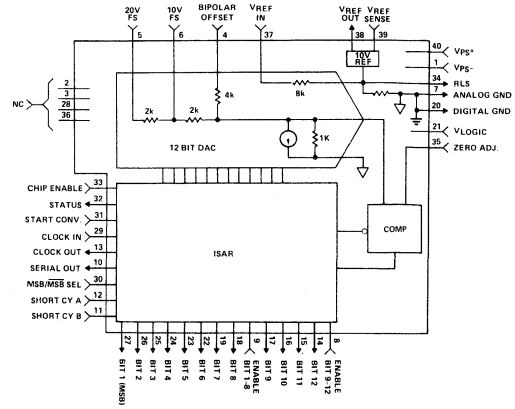
The HI-5722 is pin compatible and functionally equivalent to Harris' HI-5712, but replaces that multi-chip hybrid device with two custom IC's in a 40 pin DIP. The HI-5722 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT



PACKAGE CODE: MC

FUNCTIONAL DIAGRAM



ANALOG Digital-to-Analog Converters 6

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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Digital-to-Analog Converter Selection Guide

Part Number	Features	Resolution (Bits)	Output Range	Settling Time to ±1/2 LSB (Typ.)	Gain Error (% FSR)	Differential Non-Linearity (Max @ 25°C, LSB)	Intergral Non-Linearity (Max @ 25°C, LSB)	Ref. Reqmts. VIN/RIN (V/Ω)	Supply Voltage Power Dissipation (V/mW, Typ.)	Package Pin Count	Page
						-5/-2	-5/-2				
HI-562A	Industry Std.	12	-2mA	300ns	±0.024	±1/2 ±1/4	±1/2 ±1/4	+10/20K	+5,-15/280	24	6-5
HI-565A	+10V Ref. On-Chip	12	-2mA	350ns	±0.1	±1/2 to ±3/4	±1/4 to ±1/2	±10/20K (Internal)	±15/320	24	6-10
HI-5610	High Speed	10	-5mA	85ns	±0.05	±1/2	±1/2	+10/8K	+5,-15/420	24	6-17
HI-5618A	High Speed	8	-5mA	65ns	±0.78	±1/4	±1/4	+10/8K	+5, -15/330	18	6-23
HI-5618B	High Speed	8	-5mA	65ns	±0.78	1/2	1/2	+10/8K	+5, -15/330	18	6-23
HI-5660	Low Glitch	12	-2mA	250ns	±0.1	±3/4	±1/2	+10/20K	±15/230	24	6-30
HI-5660A	Low Glitch	12	-2mA	250ns	±0.1	±1/2	±1/4	+10/20K	±15/230	24	6-30
HI-5680V/I	Voltage/Current DAC 80, 0° to +75°C	12	10V -2mA	1.5μs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5,±15/320	24	6-39
HI-5685V/I	Voltage/Current DAC 80, -25° to+85°C	12	±10V -2mA	1.5μs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±15/320	24	6-45
HI-5685AV/I	Voltage/Current Low Drift, -25° to +85°C	12	±10V -2mA	1.5μs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±15/320	24	6-45
HI-5687V/I	Voltage/Current DAC 80, -55°C to +125°C	12	±10V -2mA	1.5μs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5,±15/320	24	6-51
HI-5690V	Fast Settling V_O; DAC 80 0°C to +75°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	± 15/555	24	6-57
HI-5695V	Fast Settling V_O; DAC 80 -25°C to +85°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	± 15/555	24	6-58
HI-5697V	Fast Settling V_O; DAC 80 -55°C to +125°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	± 15/555	24	6-59
HI-7541	Multiplying; Low Power ; CMOS	12	1mA	1.0μs Max	±0.1	±.4 to ±.8	±.4 to ±.8	±10/9K	±15/30Max	18	6-60
HI-DAC16B	16 Bit Monolithic	16	-2mA	1.0μs (14 Bits)	±0.1	±1 Typ.	±1.5 Typ.	±10/10K	±15/465	40	6-67
HI-DAC16C	16 Bit Monolithic	16	-2mA	1.0μs	±0.1	2 Typ.	3Typ.	±10/10K	±15/465	40	6-67

HARRIS

HI-562A

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- OUTPUT CURRENT 2mA, F.S.
- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING 300ns TO 0.01% (TYP.)
- LOW GAIN DRIFT ±10ppm/°C (MAX.)
- EXCELLENT LINEARITY ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE
- NOTE: HI-562A IS RECOMMENDED FOR NEW DESIGNS

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

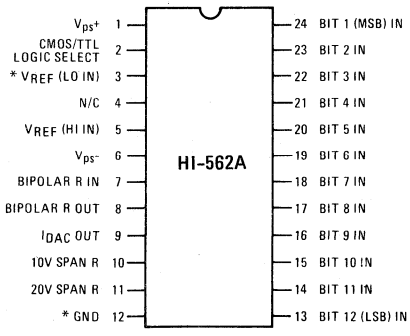
DESCRIPTION

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed true 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts, and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as a high as 3.3 MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A is offered in commercial, industrial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. All are available in a hermetically sealed 24-lead dual-in-line package.

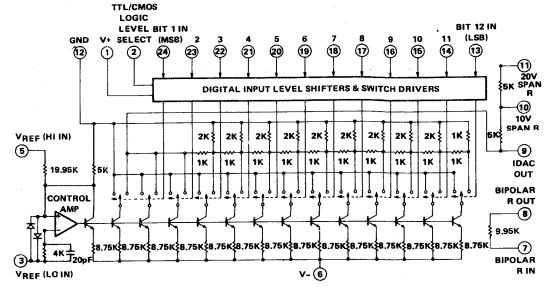
PINOUT

TOP VIEW



*Pin 3 connected to bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{PS}$
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{PS}$
	Pin 9	$+V_{PS}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-562A-2	-55°C to +125°C
HI-562A-4	-25°C to +85°C
HI-562A-5	0°C to +75°C
HI-562A-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{PS}+$, = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"	Over full temp. range			0.8			0.8	V
TTL Input Current (2) Logic "1"	Pin 2 tied to Pin 12		20	±500		20	±500	nA
TTL Logic "0"	Pin 2 tied to Pin 12		-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Connect pin 2 to pin 1 for $V_{PS}+ \geq 9.5V$. Otherwise (for CMOS levels below 9.5V) connect pin 2 to pin 12.	$0.7V_{PS}+$			$0.7V_{PS}+$			V
CMOS Logic "0"				$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Input Current Logic "1"			20	±500		20	±500	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input Input Resistance			19.95K			19.95K		Ω
Reference Input Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C		±1/2	±1/4		±1/4	±1/2	LSB
Nonlinearity (3)	Over full temp. range			±1			±1	LSB
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
Differential Nonlinearity (3)	Over full temp. range			MONOTONICITY GUARANTEED				LSB
Relative Accuracy (6)	With 50Ω (1%) Trim Resistors							
Gain Error	All Bits ON		±.024	±0.25		±.024	±0.25	
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	% FSR (4)
Unipolar Offset Error	All Bits OFF		±.012	±0.05		±.012	±0.05	% FSR (4)
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim		±0.25			±0.25		% FSR
Bipolar Offset	Potentiometers		±0.5			±0.5		% FSR
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range		±6	±10			±10	ppm of FSR/°C
Offset Drift (3)	Over full temp. range							ppm of FSR/°C
Unipolar Offset	All Bits OFF			±2			±2	ppm of FSR/°C
Bipolar Offset	All Bits OFF			±4			±4	ppm of FSR/°C
Differential Nonlinearity	Over full temp. range		±1	±2		±1	±2	ppm of FSR/°C
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
Major Carry Transient Peak Amplitude Settling Time to 90% Complete	From 011...1 to 100...0 or 100...0 to 011...1		0.7 35			0.7 35		mA ns
Power Supply Sensitivity (3) Unipolar Offset V_{ps}+ @ +5V V_{ps}- @ -15V Bipolar Offset V_{ps}+ @ 5V V_{ps}- @ -15V Gain V_{ps}+ @ +5V V_{ps}- @ -15V	All Bits OFF All Bits OFF, Bipolar mode All Bits ON		 ±0.5 ±0.5 ±1.5 ±1.5	 ±3.5 ±7.5		 ±0.5 ±0.5 ±1.5 ±1.5	 ±3.5 ±7.5	ppm of FSR/% V_{ps}

OUTPUT CHARACTERISTICS

Output Current Unipolar Bipolar		-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	mA
Resistance			2K			2K		ohms
Capacitance			20			20		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10 ±2.5 ±5 ±10			0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)

POWER REQUIREMENTS

V_{ps}+ (7) V_{ps}-	Over full temp. range	4.5 -13.5	5 -15	16.5 -16.5	4.75 -13.5	5 -15	16.5 -16.5	V
I_{ps}+ (5) I_{ps}- (5)	All Bits ON or OFF in either TTL or CMOS mode (25°C)		8 16	15 23		8 16	15 23	mA
I_{ps}+ (5) I_{ps}- (5)	Same as above except over full temp. range		11 20	20 30		11 20	20 30	mA
Power Dissipation	+25°C V_{ps}+ = +5V V_{ps}- = -15V		280	420				mW

DIE CHARACTERISTICS

Transistor Count	150
Die Size	209 x 109 mils
Thermal Constants; θ_{ja}	50°C/W
θ_{jc}	15°C/W
Tie Substrate to:	Ground
Process:	Bipolar - DI

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. $V_{PS}+$ tolerance is ±10% for HI-562A-2, -8. and ±5% for HI-562A-4,-5.

3. See Definitions.

4. FSR is "full scale range" = 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.

5. After 30 seconds warm-up.

6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

7. The HI-562A is designed for $V_{PS}+ = 5V$, but $+4.5V \leq V_{PS}+ \leq +16V$ may be connected if convenient. (For $V_{PS}+$ above +5V, there is an increase in power dissipation but little change in performance.)

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero –1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the converter resulting from a change in the -15V or +5V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

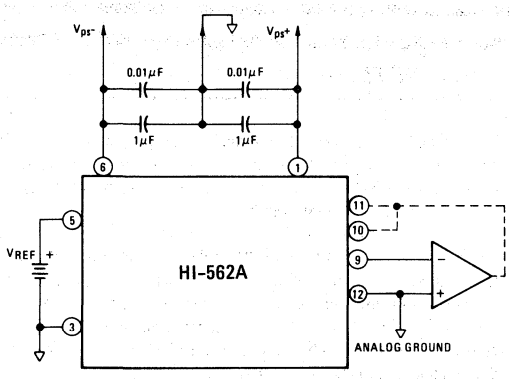
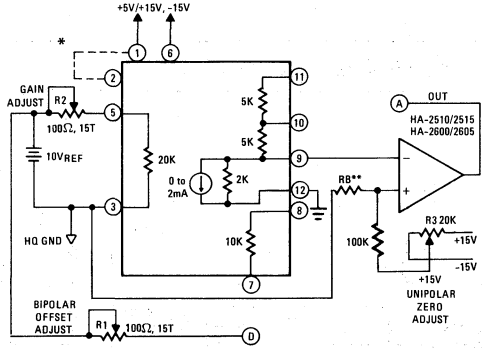


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output voltage should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility: if $V_{PS}+ < 9.5V$, connect pin 2 to pin 12. $V_{PS}+ \geq 9.5V$, connect pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar	0 to +10V	N.C.	N.C.	A	N.C.	1.43K
Mode	0 to +5V	N.C.	N.C.	A	9	1.11K
Bipolar Mode	±10V	D	9	N.C.	A	1.43K
	±5V	D	9	A	N.C.	1.25K
	±2.5V	D	9	A	9	1.0K

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5 μ V/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5 μ s settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12LSB and ±25 LSB respectivelv. If desired, the potentiometers can be replaced with fixed 50Ω(1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2LSB.

UNIPOLAR CALIBRATION
Step 1: Unipolar Offset • Turn all bits OFF • Adjust R3 for zero volts output
Step 2: Gain • Turn all bits ON • Adjust R2 for an output of FS -1 LSB That is, adjust for: 9.9976V for 0V to +10V range 4.9988V for 0V to +5V range
BIPOLAR CALIBRATION
Step 1: Bipolar Offset • Turn all bits OFF • Adjust R1 for an output of: -10V for ±10V range -5V for ±5V range -2.5V for ±2.5V range
Step 2: Gain • Turn bit 1 (MSB) ON; all other bits OFF • Adjust R2 for zero volts output

HARRIS

HI-565A

High Speed Monolithic Digital to Analog Converter with Reference

FEATURES

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX. FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

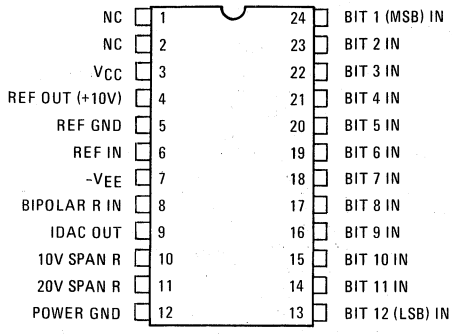
HI-565A dice are laser trimmed for a maximum integral nonlinearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

The HI-565A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. See Ordering Information.

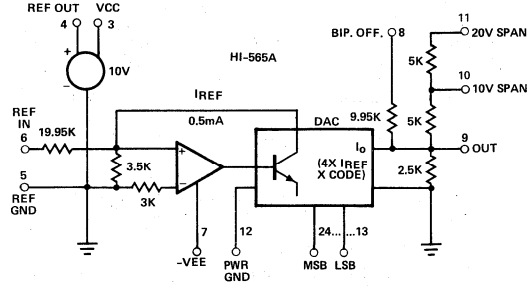
Package is a 24 pin side-brazed ceramic or plastic DIP. Power requirement is 250mW typical, with ±15V supplies.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Package Power Dissipation	
Ref In to Reference Ground	±12V	Ceramic (D)	1000mW
Bipolar Offset to Reference Ground	±12V	Plastic (N)	750mW

**Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.*

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	µA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 2, R_3 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

SPECIFICATIONS (Continued)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V DC		9.0	11.8		9.0	11.8	mA
V_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:
1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

APPLYING THE HI-565A

OP AMP SELECTION

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

NO-TRIM OPERATION

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω ; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Table 1 — Operating Modes and Calibration

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

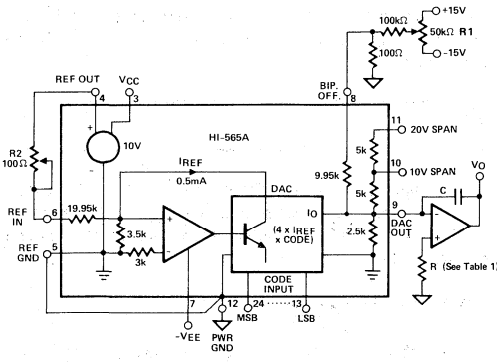


Figure 1 — Unipolar Voltage Output

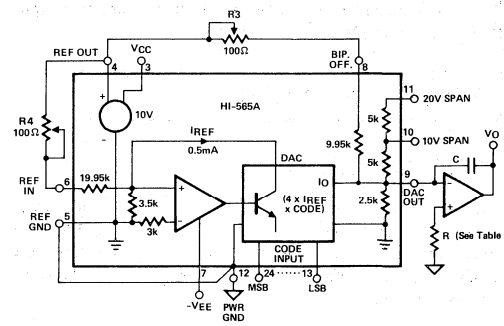


Figure 2 — Bipolar Voltage Output

SETTLING TIME

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-565A), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

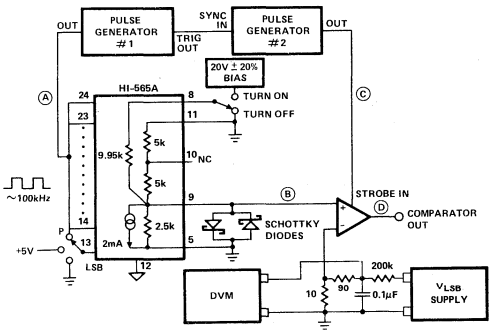


Figure 3A

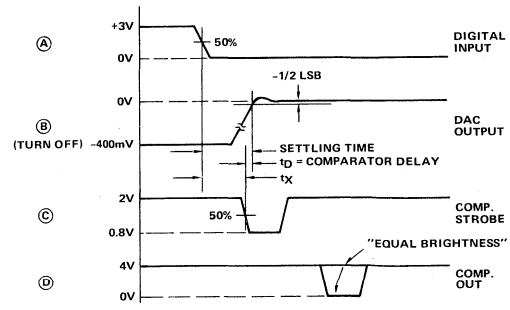


Figure 3B

OTHER CONSIDERATIONS

GROUNDS

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code – dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DAC's input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

DIE CHARACTERISTICS

Transistor Count	192
Die Size	192 x 98 mils
Thermal Constants; θ_{ja}	51°C/W
θ_{jc}	16°C/W
Tie Substrate to:	Ground
Process:	Bipolar - DI

HARRIS

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . ± ½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

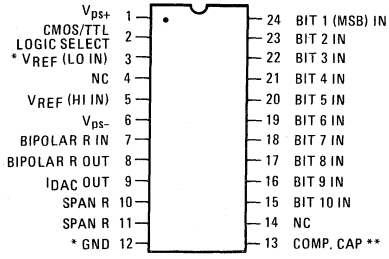
The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±1LSB for both unipolar and bipolar operation.

The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12MHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. All are available in a hermetically sealed 24 lead dual-in-line package.

PINOUT

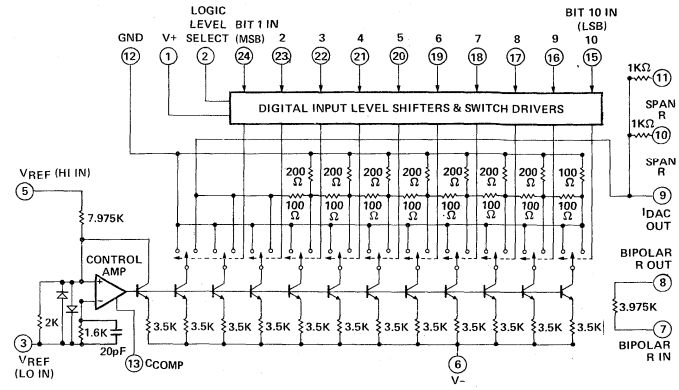
TOP VIEW



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01μF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5610-2	-55°C to +125°C
HI-5610-5	0°C to +75°C
HI-5610-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

PARAMETER	TEMP	HI-5610-2 HI-5610-8 MIN	HI-5610-2 HI-5610-8 TYP	HI-5610-2 HI-5610-8 MAX	HI-5610-5 MIN	HI-5610-5 TYP	HI-5610-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V_{ps+}
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V_{ps+}
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								Ω
Input Resistance			8K			8K		
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			± ½			± ½	LSB
	25°C			± ½			± ½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			± 0.05	± 0.25		± 0.05	± 0.25	% FSR
Unipolar Offset Error								
(Input Code 00....0)			± 0.05	± 0.10		± 0.05	± 0.10	% FSR
Bipolar Offset Error								
(Input Code 00....0)			± 0.05	± 0.15		± 0.05	± 0.15	% FSR
(Adjustable to zero, see Fig. 4, 5)								
Adjustment Range								
Gain			± 0.25			± 0.25		% FSR
Bipolar Offset			± 0.25			± 0.25		% FSR
Temperature Stability								
Gain Drift	Full		± 5			± 5		ppm/°C
Unipolar Offset Drift	Full		± 3			± 3		ppm/°C
Bipolar Offset Drift	Full		± 3			± 3		ppm/°C
Differential Nonlinearity	Full		± 2			± 2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's			85			85		ns
From all 1's to all 0's			85			85		ns
Major Carry Switching to 90% Complete			40			40		ns

SPECIFICATIONS (continued)

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								
V_{ps}+ = +5V, V_{ps}- = -13.5V to -16.5V								
Gain								
(Input Code 11....1)				±3.5			±3.5	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		ppm of FSR/%V_{ps}
Bipolar Offset								
(Input Code 00....0)			±1.5			±1.5		
V_{ps}- = -15V, V_{ps}+ = 4.5V to 5.5V								
Gain								
(Input Code 11....1)				±7.5			±7.5	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								
(Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-4.0	-5.0	-6.0	-4.0	-5.0	-6.0	mA
Bipolar		±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+5			+5		V
			+2.5			+2.5		V
Bipolar			±2.5			±2.5		V
			±1.25			±1.25		V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		μV_{p-p}
0.1Hz to 1MHz			100			100		μV_{p-p}
POWER REQUIREMENTS								
V_{ps}+ (4)	Full	4.5	5	16.5	4.75	5	16.5	V
V_{ps}-	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{ps}+ (All 1's or all 0's in	25°C		9	15		9	15	mA
(10) either TTL or CMOS Mode)	Full		15	20		15	20	mA
I_{ps}- (Same as above)	25°C		25	30		25	30	mA
(10)	Full		30	35		30	35	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions).
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{ps}+ tolerance is ±10% for HI-5610-2,-8. And ±5% for HI-5610-5.
4. For CMOS compatibility based on V_{ps}+ ≥ 9.5V, (switching thresholds equal V_{ps}+/2), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ±1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions.)
7. Using an external op amp and internal span resistors. (See operating instructions for connections.)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ±2.5V range, 2.5V for ±1.25V range, etc., or 5mA (±20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle within the specified error band for any input code transition. It is usually specified for a full scale transition (11...1 to 00...0 or vice versa).

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (TL) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5610 (preferably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

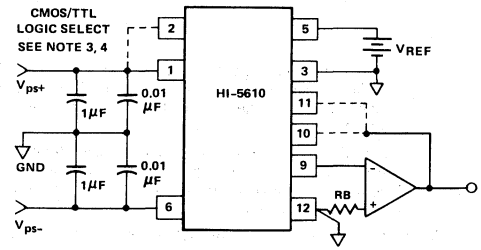


FIGURE 1

OPERATING INSTRUCTIONS (continued)

HIGH PRECISION PERFORMANCE

The output accuracy of the HI-5610 depends mainly on the accuracy of voltage applied to the V_{REF} input, since full scale output current is approximately $4V_{REF}/8K\Omega$. For precision performance a +10V voltage reference with reasonably low temperature coefficient such as HA-1608 is recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5610 internal scaling resistors as feedback elements. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of $5\mu V/^oC$ and $1nA/^oC$, respectively. The input reference resistor ($7.975K\Omega$) and bipolar offset resistor ($3.975K\Omega$) are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than $1\mu s$ settling to 1/2 LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +5V and +2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS-1LSB
  That is, adjust for:
  4.99512V for 0V to +5V range
  2.49756V for 0V to +2.5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 4.99512V
10 0	½FS	= 2.50000V
01 1	½FS -1LSB	= 2.49512V
00 0	Zero	= 0.00000V

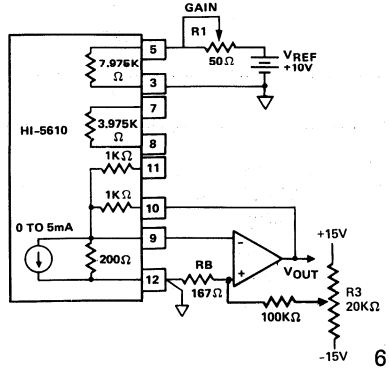


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +2.5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 2.49756V
10 0	½FS	= 1.25000V
01 1	½FS -1LSB	= 1.24756V
00 0	Zero	= 0.00000V

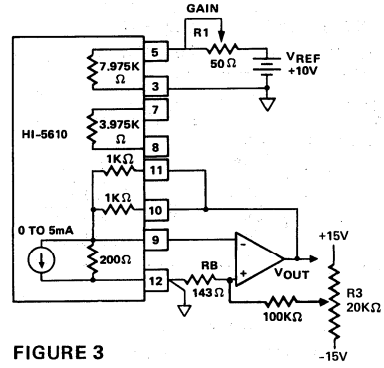


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 2.5V and ± 1.25V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1, Offset:
- Turn all bits off (all 0's)
- Adjust R2 for output voltage as follows:
  -2.5V, ±2.5V range
  -1.25V, ±1.25V range

Step 2, Gain:
- Turn all bits on (all 1's)
- Adjust R1 for an output voltage of (+FS -1LSB).
  That is:
  +2.49512V, ±2.5V range
  +1.24756V, ±1.25V range

OPERATING INSTRUCTIONS (continued)

BIPOLAR - OFFSET BINARY
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1 LSB	= +2.49512V
10 0	ZERO	= +0.00000V
01 1	Zero - 1 LSB	= -0.00488V
00 0	-FS	= -2.50000V

BIPOLAR TWO'S COMPLEMENT **
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49512V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00488V
10 0	-FS	= -2.50000V

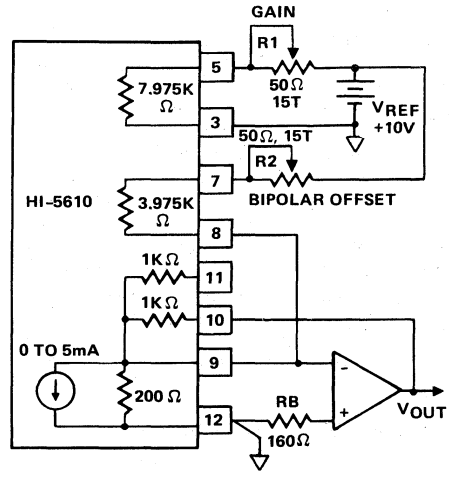


FIGURE 4

BIPOLAR - OFFSET BINARY
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +1.24756V
10 0	Zero	= +0.00000V
01 1	Zero - 1LSB	= -0.00244V
00 0	-FS	= -1.25000V

BIPOLAR - TWO'S COMPLEMENT **
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +1.24756V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00244V
10	-FS	= -1.25000V

** Invert MSB with external inverter
to obtain two's complement coding.

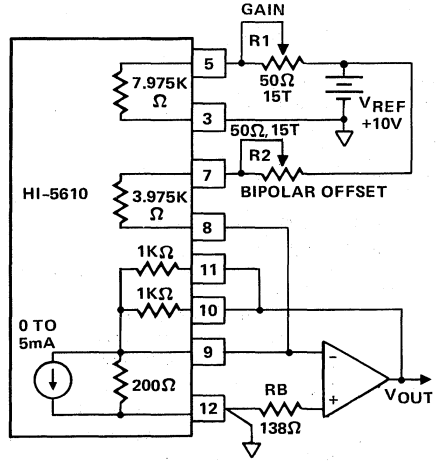


FIGURE 5

DIE CHARACTERISTICS

Transistor Count		138
Die Size:		103 x 209 mils
Thermal Constants;	θ ja	50°C/W
	θ jc	15°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

HI-5618A/5618B

8 Bit High Speed Digital-to-Analog Converters

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 65ns
- MINIMUM NONLINEARITY ERROR
  - HI-5618A ±1/4 LSB MAX
  - HI-5618B ±1/2 LSB MAX
- LOW POWER OPERATION 340mW TYP
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CMOS, TTL, OR DTL COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERSION
- WAVEFORM SYNTHESIS
- HIGH RELIABILITY APPLICATIONS
- VIDEO SIGNAL RECONSTRUCTION

DESCRIPTION

The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 65ns to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy without trimming. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

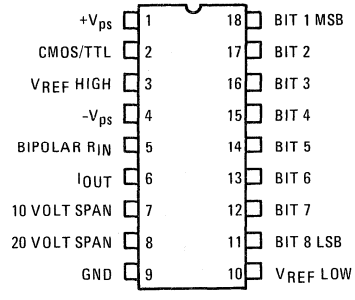
The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. The HI-5618A/B is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

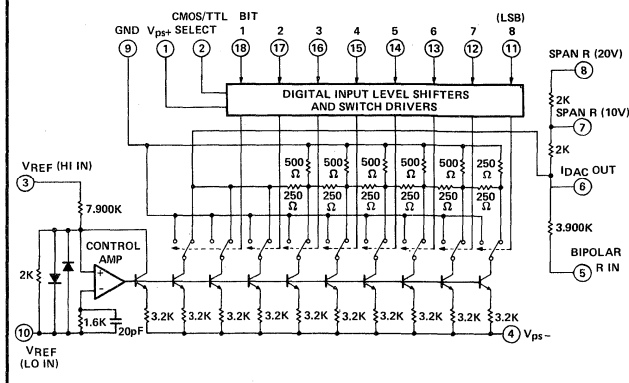
Power requirements are +5V and -15V. Package is an 18 pin DIP, in plastic or ceramic.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (1)

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1 - 8	-1V, +12V
CMOS/TTL Logic Select		-1V, +12V
Outputs	Pins 5, 7, 8	$\pm V_{ps}$
	Pin 6	$+V_{ps}$, -2.5V

Power Dissipation Pd, Package	700mW
Operating Temperature Range	
HI-5618A/B-2	-55°C to +125°C
HI-5618A/B-5	0°C to +75°C
HI-5618A/B-8	-55°C to +125°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS ($V_{ps}+ = +5V$; $V_{ps}- = -15V$; $V_{REF} = +10V$; Pin 2 to GND, unless otherwise noted)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL logic Input Voltage (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
TTL Logic Input Current	Logic "1"	Full		20	500		20	500	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
	Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Logic Input Current	Logic "1"	Full		20	500		20	500	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input									
Input Resistance		+25°C		8k			8k		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity, Integral and Differential	HI-5618A	25°C			±1/4			±1/4	LSB
		Full			±3/8			±3/8	LSB
	HI-5618B	25°C			±1/2			±1/2	LSB
		Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference)									
Gain		25°C			±2			±2	LSB
Unipolar Zero		25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)		25°C			±2			±2	LSB
Temperature Stability									
Gain Drift		Full			±1/4			±1/4	LSB
Unipolar Zero Drift		Full			±1/16			±1/16	LSB
Bipolar Zero Drift		Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB									
High Impedance (11)	(from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		65	75		65	75	ns

SPECIFICATIONS (Continued)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS (Continued)									
Glitch (5) - Major Carry Transition									
Duration		+25°C		20			20		ns
Amplitude (See Fig. 4)		+25°C		350			350		mV
Area		+25°C		3500			3500		mV–ns
Power Supply Sensitivity (5)									
V_{ps+} = +5V, V_{ps-} = -13V to -16.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		FSR/% Vps (9)
V_{ps-} = -15V, V_{ps+} = 4.5V to 5.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS									
Output Current	Unipolar	+25°C	-4	-5	-6	-4	-5	-6	mA
	Bipolar	+25°C	±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance		+25°C		500			500		Ω
Output Capacitance		+25°C		20			20		pF
Output Voltage Range (7)	Unipolar	+25°C		+10			+10		V
		+25°C		+5			+5		V
	Bipolar	+25°C		±10			±10		V
		+25°C		±5			±5		V
		+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)		+25°C		±1.5			±1.5		V
Output Noise Voltage (8)	0.1Hz to 100Hz	+25°C		30			30		μV_{p-p}
	0.1Hz to 1Mhz	+25°C		100			100		μV_{p-p}
POWER REQUIREMENTS (4)									
V_{ps+}		Full	4.5	5	16.5	4.5	5	16.5	V
V_{ps-}		Full	−13.5	−15	−16.5	−13.5	−15	−16.5	V
I_{ps+} (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)		+25°C		9			9		mA
		Full			12			12	mA
I_{ps-} (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)		+25°C		19			19		mA
		Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{ps+} tolerance is ± 10% for HI-5618A/B -2, -8; and ± 5% for HI-5618A/B-5.
4. For CMOS compatibility based on $V_{ps+} \geq 9.5V$, (switching thresholds equal $V_{ps+}/2$), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100 Ω ± 1% resistors, in place of R_1 and R_2.
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit , Figure 4.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in fractional LSB's, or parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

ZERO DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Zero error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Zero Drift is calculated for high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two representing worst case drift.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale transition. D/A settling time may vary depending upon the impedance level being driven. A comparator presents a high impedance, while an op amp connected for current to voltage conversion presents a low impedance. Figure 3a shows the test circuit used for testing the HI-5618A/B for T_S (OFF) into a high impedance.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011. . .1 to 100. . .0 or vice versa. For example, if turn ON is greater than turn OFF for 100. . .1 to 100. . .0, an intermediate state of 000. . .0 exists, such that, the output momentarily glitches toward zero output. In general, when a D/A is driven by a set of external logic gates, the unmatched turn on – turn off times at the gates will add to the glitch problem. See Figure 4.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in the +5V or -15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE VOLTAGE

When the D/A converter is used without an op amp, it may be configured for various ranges of voltage at its output. However, Compliance Voltage is the maximum full scale voltage for which the converter will comply with its specifications.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5618A/B; preferably to the device pin. A solid tantalum or electrolytic capacitor in parallel with a smaller ceramic type is recommended.

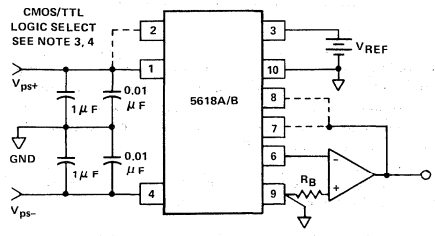


FIGURE 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

Make connections as shown in the table and Figure 2, for five standard output ranges:

	OUTPUT RANGE	CONNECTIONS PIN 5 TO	CONNECTIONS PIN 7 TO	CONNECTIONS PIN 8 TO	BIAS RESISTOR R_B
Unipolar Mode	0 to +10V	NC	A	NC	400Ω
	0 to +5V	NC	A	6	330Ω
Bipolar Mode	± 10V	D	NC	A	400Ω
	± 5V	D	A	NC	360Ω
	± 2.5V	D	A	6	310Ω

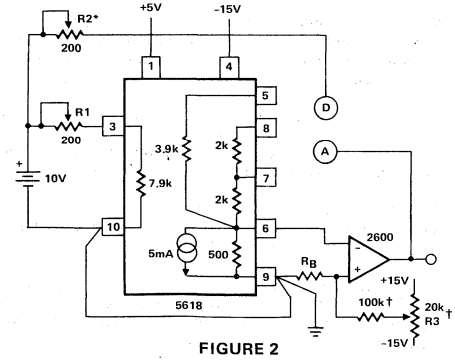


FIGURE 2

*Used in Bipolar Mode only.
†Used in Unipolar Mode only.

OPERATING INSTRUCTIONS (continued)

The HI-5618A/B accepts an 8 bit digital word in Straight Binary code. In the bipolar mode this code becomes Offset Binary. Also in bipolar mode, the MSB may be complemented using an external inverter to obtain 2's complement code. Here are the correct outputs for some key input codes:

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 9.96094V
10 0	½FS	= 5.00000V
01 1	½FS - 1 LSB	= 4.96094V
00 0	Zero	= 0.00000V

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 4.98047V
10 0	½FS	= 2.50000V
01 1	½FS - 1 LSB	= 2.48047V
00 0	Zero	= 0.00000V

BIPOLAR - OFFSET BINARY
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +9.92188V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.07813V
00 0	-FS	= -10.0000V

BIPOLAR - TWO'S COMPLEMENT **
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +9.92188V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.07813V
10 0	-FS	= -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

Output Accuracy of the HI-5618A/B is affected directly by the reference voltage, since $I_0(F/S) \simeq 4\ (V_{REF}/8k\Omega)$. For precision performance, a stable +10V reference with low temperature coefficient is recommended, such as HARRIS HA-1608.

The output current may be converted to voltage using an external op amp with the internal span and offset resistors, as shown above in the table. The op amp should have good front end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.9kΩ) and bipolar offset resistor (3.9kΩ) are both intentionally set low by 100Ω to allow the user to externally trim out initial errors to a high degree of precision.

For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns. (See Applications).

CALIBRATION (See Figure 2)

UNIPOLAR MODE -

1. Apply zero (all 0's) input, and adjust R_3 for 0V output.
2. Apply full scale (all 1's) input, and adjust R_1 for:
   +9.96094 Volts, +10 Volt range
   +4.98047 Volts, +5 Volt range
   -5 Volts, ± 5 Volt Range
   -2.5 Volts, ±2.5 Volt Range

BIPOLAR MODE -

1. Apply negative full scale (also called bipolar offset): All 0's for offset binary; 1000 . . . . for 2's complement. Adjust R_2 for output voltages as follows:
   -10 Volts, ±10 Volt Range
2. Apply positive full scale (all 1's for offset Binary; 0111. . . . for 2's complement) Adjust R_1 for output voltages as follows:
   +9.92188 Volts, ± 10 Volt Range
   +4.96094 Volts, ±5 Volt Range
   +2.48047 Volts, ±2.5 Volt Range
3. Apply zero input (1000. . . . for offset Binary; 0000. . . . for 2's complement). Output should be zero volts. Any error is due to nonlinearity in the DAC, and cannot be nulled without disrupting the calibration in steps 2 and 3.

SETTLING TIME

Turn-off settling time ($T_{S(OFF)}$) is somewhat longer than $T_{S(ON)}$ for the HI-5618. Typical $T_{S(OFF)}$ performance is shown in Figure 3C, using the circuit of Figure 3A.

Refer to Figure 3B; Settling time following turn-off equals T_X plus T_D. The comparator delay T_D may be measured at 1mV/cm, using a Tektronix 7A13 differential comparator or equivalent. Then, T_X is easily measured in a short procedure:

- Adjust delay on generator # 2 for T_X approximately 1μs
- Switch the LSB to +5V (ON).
- Adjust the V_{LSB} supply for 50 percent triggering at COMP. OUT (equal brightness).
- DVM reads -1 LSB. Adjust V_{LSB} supply so DVM reads -1/2 LSB.
- Switch the LSB to P (pulse); COMP. OUT pulse disappears.
- Reduce generator # 2 delay until COMP. OUT pulse reappears; adjust delay for "equal brightness".
- Measure T_X from scope. (Any overshoot will be less than 1/2 LSB, so it is not necessary to examine the other side of the envelope, i.e. final value plus 1/2 LSB.)

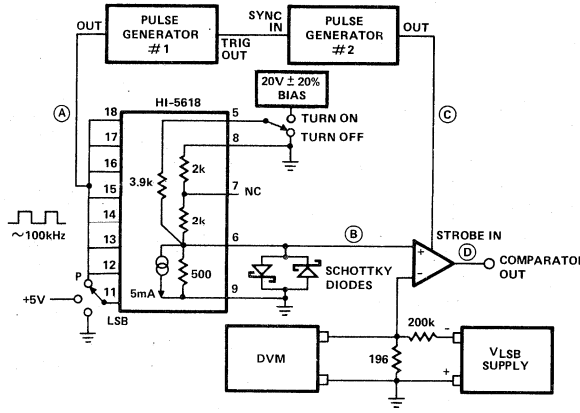


Figure 3A

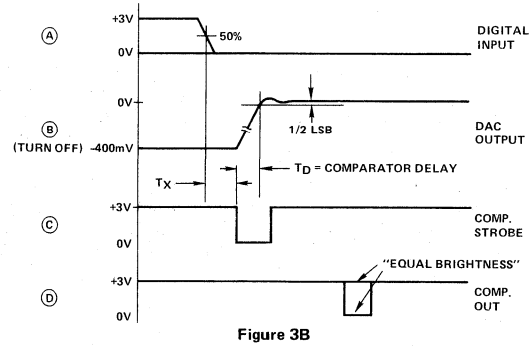


Figure 3B

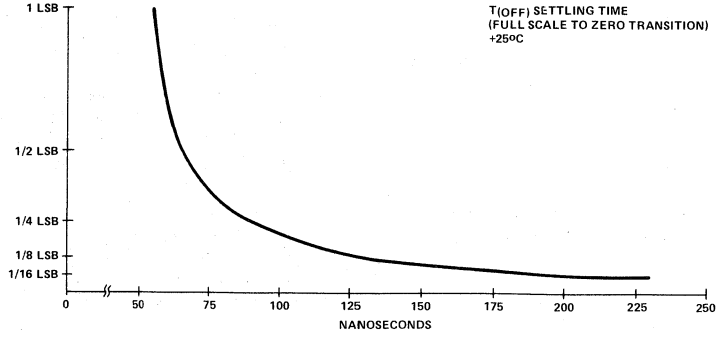
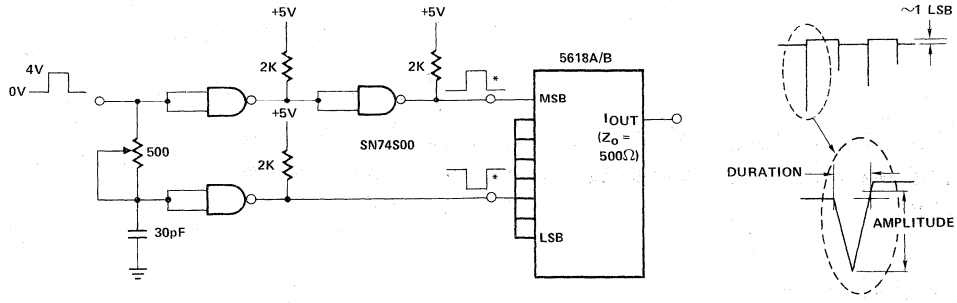


Figure 3C

TEST CIRCUIT (Continued)

OUTPUT GLITCH MEASUREMENT

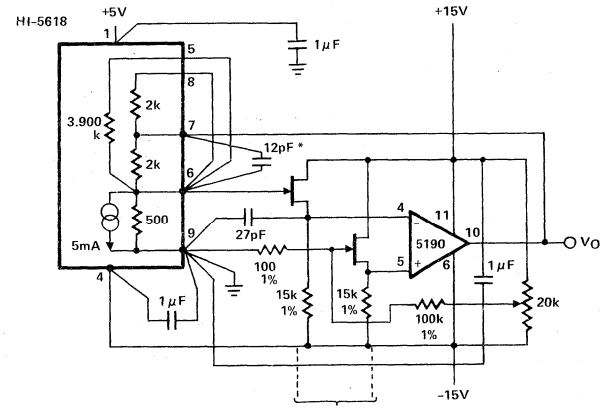


* ADJUST 500Ω TRIMMER SO THAT INPUT SIGNALS CROSS THEIR RESPECTIVE SWITCHING THRESHOLDS AT THE SAME TIME.

Figure 4

APPLICATIONS

HIGH SPEED VOLTAGE OUTPUT



MATCHED DUAL N-FET,
MICRO POWER SYSTEMS MP-835
OR EQUIVALENT

* NOMINAL VALUE, SELECTED FOR OPTIMUM STEP RESPONSE.

DIE CHARACTERISTICS

Transistor Count		122
Die Size:		103 x 209 mils
Thermal Constants;	θ_{ja}	75°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

HARRIS

HI-5660/5660A

High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- FAST SETTLING (TO ±1/2 LSB) 350ns
- ±1/2 LSB MAX. NONLINEARITY GUARANTEED OVER TEMPERATURE
- INTERNAL CANCELLATION OF GROUND CURRENT
- EXCELLENT POWER SUPPLY REJECTION 1ppm/%PS
- LOW COST

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- CRT DISPLAYS
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-5660 is a current output, 12 bit monolithic digital-to-analog converter. It offers high speed plus enhanced accuracy, through internal cancellation of ground currents.

Electrical performance is similar to that of the AD566A. Pinouts are identical except for pin 1, which requires a +5V supply (versus no connection on the AD566A).

Fabrication of the HI-5660 features the Harris bipolar dielectric isolation process, which eliminates latchup and minimizes parasitic capacitance and leakage currents. The chip includes nichrome thin-film resistors, laser trimmed at the wafer level to a maximum linearity error of ±1/4 LSB at +25°C.

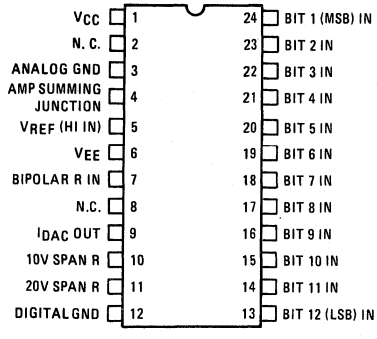
Near zero current in the Analog Ground terminal simplifies use of the HI-5660 by minimizing noise and offsets between the package and the system analog ground. This is accomplished by adding a complement current to the internal ground from an auxiliary R-2R ladder, and then supplying the resultant DC current from the positive power supply.

The Harris HA-1608 +10V precision reference is recommended for use with the HI-5660 in non-multiplying applications.

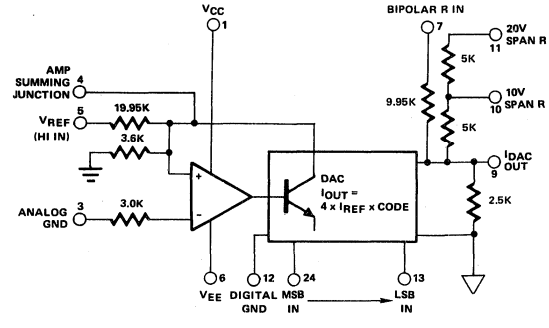
The HI-5660 is offered in two accuracy grades each for the commercial and military temperature ranges. Package is a 24 pin plastic or ceramic DIP, and power requirements are +15V, -15V.

PINOUT

TOP VIEW
24 LEAD DIP



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Package Power Dissipation	
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Ceramic	1000mW
Ref In to Reference Ground	±12V	Plastic	750mW
Bipolar Offset to Reference Ground	±12V		

**Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.*

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-5660-5 MIN	HI-5660-5 TYP	HI-5660-5 MAX	HI-5660A-5 MIN	HI-5660A-5 TYP	HI-5660A-5 MAX	UNITS
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	0.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of FS
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		500			500		ns
With 75Ω External Load		250			250		ns

MODEL	HI-5660-5 MIN	HI-5660-5 TYP	HI-5660-5 MAX	HI-5660A-5 MIN	HI-5660A-5 TYP	HI-5660A-5 MAX	UNITS
TEMPERATURE RANGE							
Operating	0		+75	0		+75	°C
Storage	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2): Bipolar Operation at Digital Input Only.						
Reference Voltage	Unipolar: +10V Max, +2V Min.						
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.						
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical						
Output Slew Rate 10%-90%	1.3mA/µs						
90%-10%	1.3mA/µs						
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5µs to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:
1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-5660-2, HI-5660-8 MIN	HI-5660-2, HI-5660-8 TYP	HI-5660-2, HI-5660-8 MAX	HI-5660A-2, HI-5660A-8 MIN	HI-5660A-2, HI-5660A-8 TYP	HI-5660A-2, HI-5660A-8 MAX	UNITS
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of FS
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		500			500		ns
With 75Ω External Load		250			250		ns

MODEL	HI-5660-2, HI-5660-8 MIN	HI-5660-2, HI-5660-8 TYP	HI-5660-2, HI-5660-8 MAX	HI-5660A-2, HI-5660A-8 MIN	HI-5660A-2, HI-5660A-8 TYP	HI-5660A-2, HI-5660A-8 MAX	UNITS
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2): Bipolar Operation at Digital Input Only.						
Reference Voltage	Unipolar: +10V Max, +2V Min.						
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.						
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical						
Output Slew Rate 10%-90%	1.3mA/µs						
90%-10%	1.3mA/µs						
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5µs to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:
1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-5660 accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement*, or Offset Binary (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i. e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

APPLYING THE HI-5660

OP AMP SELECTION

The HI-5660's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

Table 1 – Operating Modes and Calibration

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)*	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

*Many op amps do not require this resistor, since a bias current of 60nA produces a worst case output error of only 100μV. For a low bias current amplifier, connect its non-inverting input directly to ground.

NO-TRIM OPERATION

The HI-5660 will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100 Ω trimming potentiometers: In Figure 1 replace R2 with 50 Ω ; also remove the network on pin 7 and connect 50 Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50 Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

When using wide bandwidth op amps, the feedback capacitor C may be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-5660 these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

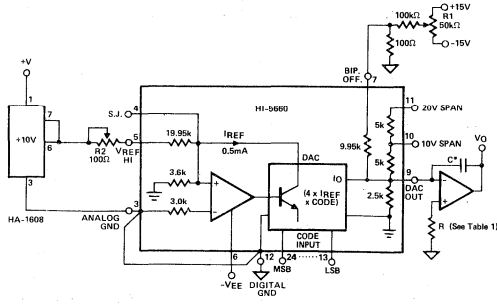


Figure 1 – Unipolar Voltage Output

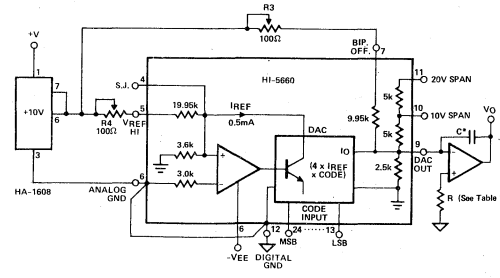


Figure 2 – Bipolar Voltage Output

SETTLING TIME

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-5660), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals t_X + t_D, i.e. t_X +15ns.

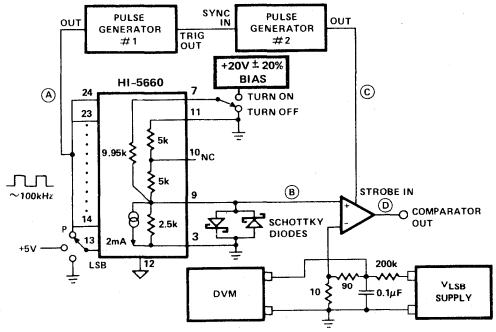


Figure 3A

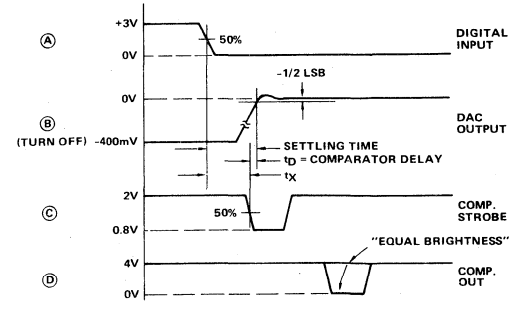


Figure 3B

OTHER CONSIDERATIONS

GROUNDS

The HI-5660 has two ground terminals, pin 3 (ANALOG GND) and pin 12 (DIGITAL GND). The current through pin 3 is near-zero DC, but pin 12 carries up to 1.75mA of code-dependent current from bits 1, 2 and 3. The general rule is to connect pin 3 to the system analog ground and pin 12 to the power or digital ground. If the system has a single ground point, provide separate paths to pins 3 and 12.

Current cancellation in pin 3 is accomplished as follows: An auxiliary 9 bit R-2R ladder is driven by the complement of the HI-5660 input code. Together, the main and auxiliary ladders draw a constant 2.25mA from the internal analog ground, regardless of input code. This current is then sourced from the positive supply via a current mirror, yielding near-zero current through pin 3.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-5660 are very critical for high speed performance. Output capacitance of the DAC is only 25pF, so a small change or additional capacitance may alter the output op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C).

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-5660 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient.

DIE CHARACTERISTICS

Transistor Count		158
Die Size:		104 x 172 mils
Thermal Constants;	θ_{ja}	52°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

HARRIS

HI-5680

12 Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5680 is a monolithic, direct replacement for the popular DAC80-CBI, DAC80Z-CBI, and DAC85C-CBI, incorporating the best features of each. Single chip construction, along with several design innovations, make the HI-5680 the optimum choice for low cost, high reliability applications.

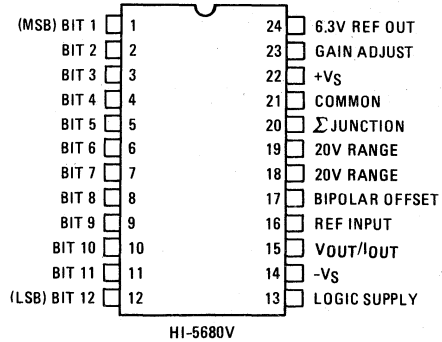
Harris' unique Dielectric Isolation(DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5680V), or with a user supplied external amplifier (HI-5680I).

Internally, the HI-5680 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to +75°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

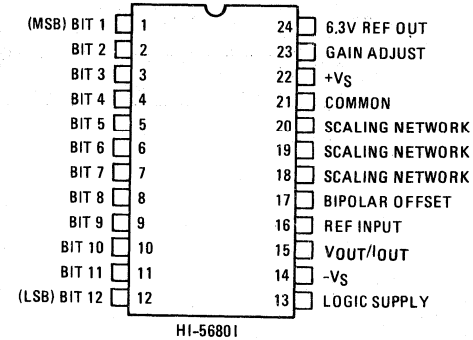
PINOUTS

TOP VIEW



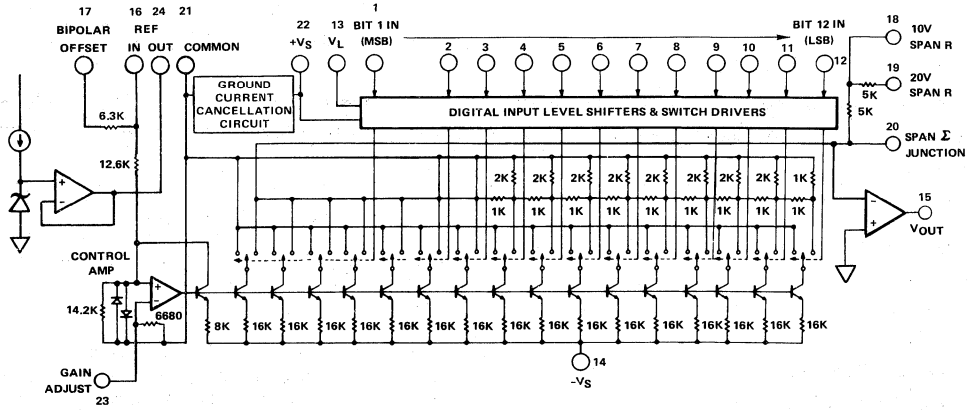
HI-5680V
VOLTAGE OUTPUT

TOP VIEW



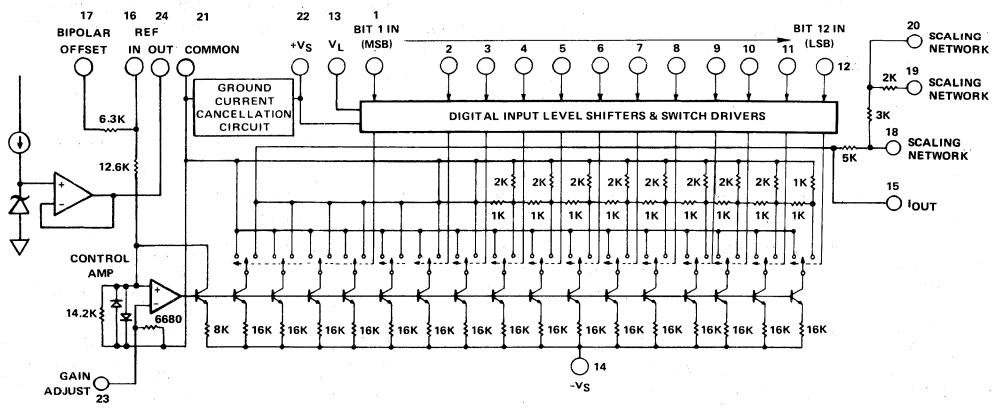
HI-5680I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5680 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5680 I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation	Pd, Package	1000mW
	$-V_S$	−20V			
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
				HI-5680I/V-5	0°C to +75°C
Reference	Input (pin 16)	$+V_S$			
	Output drain	2.5mA	Storage Temperature Range		−65°C to +150°C
Digital Inputs	Bits 1 to 12	−1V to +12V			

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_S = ±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5680X MIN	HI-5680X TYP	HI-5680X MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	Volts
Logic "0"	at -100 μA	0		+0.8	Volts
ACCURACY (3)					
Linearity Error	0°C to +75°C		±¼	±½	LSB
Differential Lin. Error	0°C to +75°C		±½	±¾	LSB
Gain Error (2)			±0.1	±0.3	%FSR
Offset Error (2)			±.05	±0.15	%FSR
Monotonicity	0°C to +75°C		Guaranteed		
DRIFT (3)	0°C to +75°C				
Total Bipolar Drift (Includes gain, offset and linearity drifts.)				±20	ppm/°C
Total Error	0°C to +75°C				
Unipolar (Note 6)			± 0.08	±0.15	%FSR
Bipolar (Note 6)			± 0.06	±.1	%FSR
Gain	Including internal reference		±15	±30	ppm/°C
	Exclusive of internal reference		±5	±7	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED (3)					
Voltage Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB change			1.5		μs
Slew Rate		10	15		V/μs
Current Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1000		ns
ANALOG OUTPUT					
Voltage Models					
Output current		±5			mA
Output Resistance			.05		Ω
Short Circuit Duration	to common		continuous		

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5680X MIN	HI-5680X TYP	HI-5680X MAX	UNITS
ANALOG OUTPUT					
Current Models					
Output Current					
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			20		ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V supply				.002	$\frac{\%FSR}{\Delta V_s}$
−15V supply				.002	
+5V supply				.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		-11.4	-15	-16.5	V
+5V		+ 4.5	+ 5	+16.5	V
Current					
+15V			8	11	mA
- 15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "Full Scale Range" and is 20V for ± 10V range, 10V for ± 5V range, etc., or 2mA (± 20%) for current output.
5. The HI-5680 will operate with supply voltages as low as ± 11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ± 12V.
6. With gain and offset errors adjusted to zero at 25°C.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ_{ja}	49°C/W
	θ_{jc}	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

DIGITAL INPUTS

The HI-5680 accepts digital input codes in complementary, binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale
* Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H –25°C) and low ranges (+25°C–T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H –25°C) and low (+25°C –T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5680 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

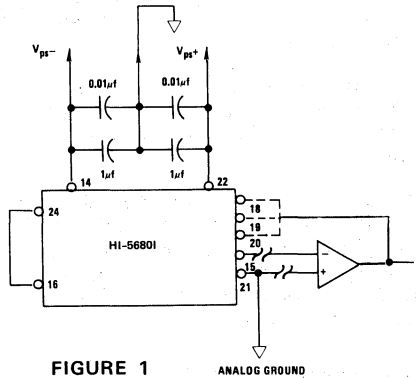


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5680 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5680. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5680V

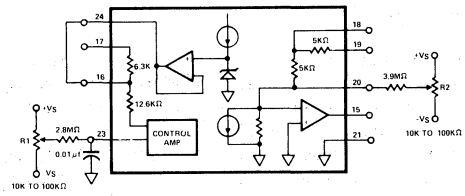


FIGURE 2

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5680I

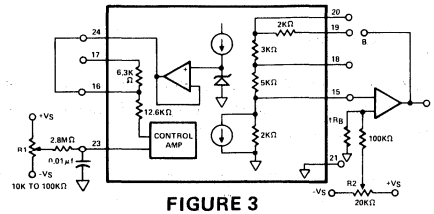


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5680I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HARRIS

HI-5685/5685A

High Performance Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 85 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC –25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5685 is a monolithic direct replacement for the popular DAC85-CBI and the ADDAC85LD-CBI. Single chip construction along with several design innovations make the HI-5685 the optimum choice for low cost, high reliability applications.

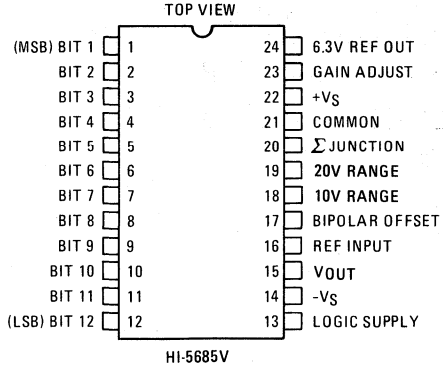
Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5685V), or with a user supplied external amplifier (HI-5685I).

Internally, the HI-5685 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

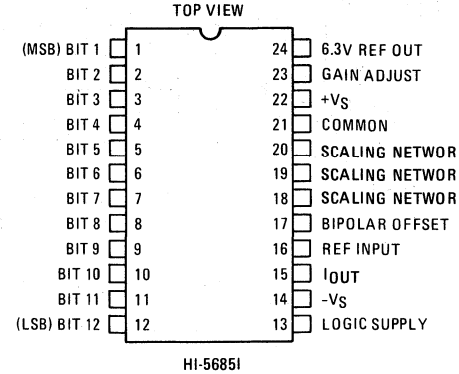
The HI-5685 and HI-5685A are available in both current and voltage output models which are guaranteed over the –25°C to +85°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

The HI-5685A offers exceptionally low drift over temperature. Gain drift is a maximum ±10ppm/°C, over –25°C to +85°C.

PINOUTS

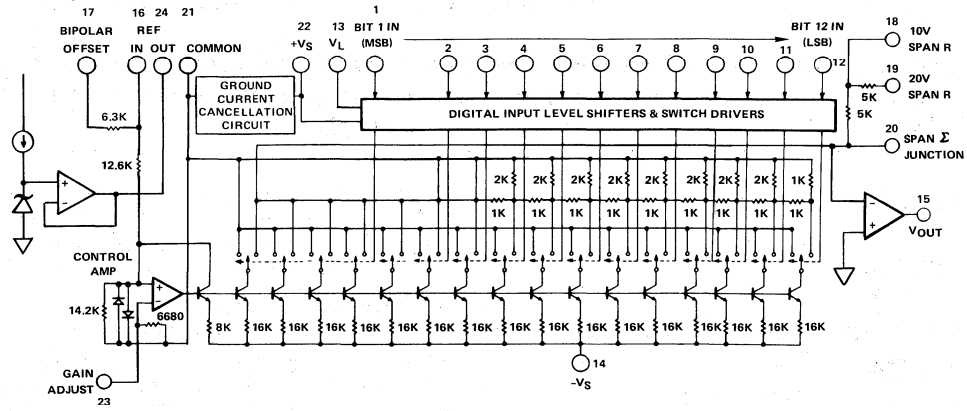


HI-5685V
VOLTAGE OUTPUT



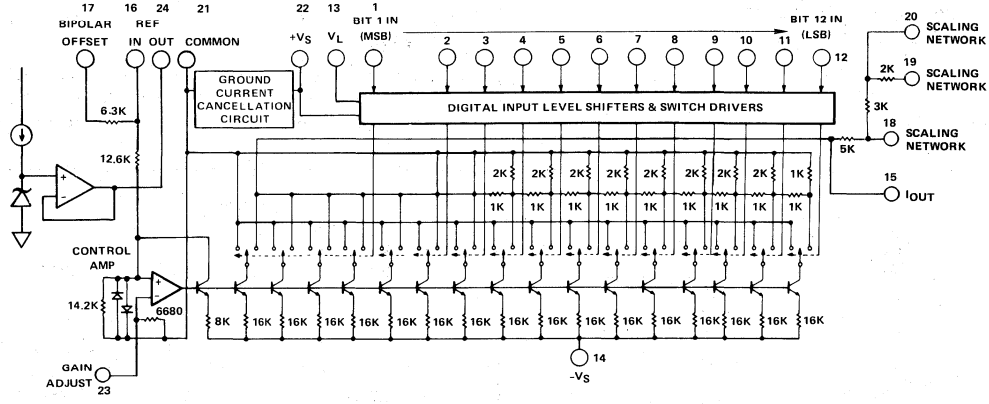
HI-5685I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5685 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5685 I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation		
	$-V_S$	−20V		Pd, Package	1000mW
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
Reference	Input (pin 16)	$\pm V_S$		HI-5685I/V−4	−25°C to +85°C
	Output drain	2.5mA		HI-5685AI/V−4	−25°C to +85°C
Digital Inputs	Bits 1 to 12	−1V to +12V	Storage Temperature Range		−65° to +150°C

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_S = ±15V , V_{LOGIC} = 5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	HI-5685 MIN	HI-5685 TYP	HI-5685 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 µA	+2		+5.5	V
Logic "0"	at −100 µA	0		+0.8	V
Accuracy (3)					
Linearity Error	at +25°C			±½	LSB
	−25°C to +85°C			±½	LSB
Differential Lin. Error				±½	LSB
Gain Error (2)			±0.1	±0.15	%FSR (4)
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-25°C to +85°C		GUARANTEED		
DRIFT (3) HI-5685	−25°C to +85°C				
Gain				±20	
Offset					
Unipolar			±1	±3	PPM/°C
Bipolar			±5	±10	
DRIFT (3) HI-5685A (Low Drift)	−25°C to +85°C				
Gain				±10	
Offset					PPM/°C
Unipolar			±1		
Bipolar				±5	
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩFeedback			3		µs
With 5KΩFeedback			1.5		µs
For 1 LSB Change			1.5		µs
Slew Rate			15		V/µs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		µs

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5685 MIN	HI-5685 TYP	HI-5685 MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		±5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		−2.5		+10	V
INTERNAL REFERENCE					
Output voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±10	±20	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				.002	$\frac{\%FSR}{\Delta V_S}$
−15V				.002	
+5V				.002	
POWER SUPPLY REQUIREMENTS(5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5685 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

DIGITAL INPUTS

The HI-5685 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale
* Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C – T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C – T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5685 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

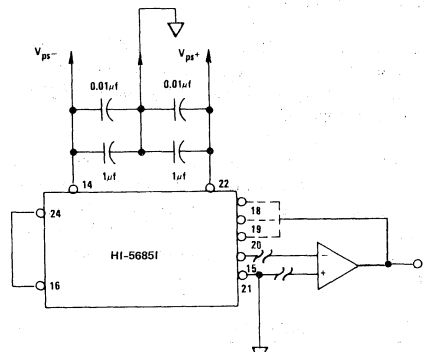


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5685 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5685. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5685V

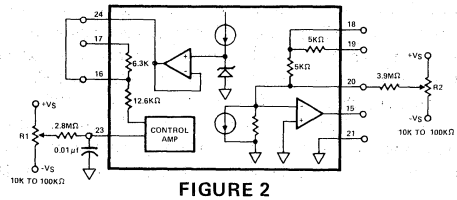


FIGURE 2

RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5685I

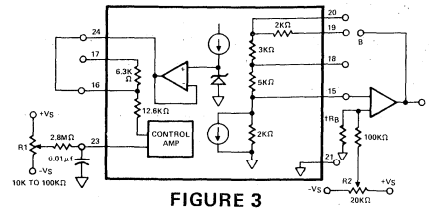


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5685I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HARRIS

HI-5687

Wide Temperature Range Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 87 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION
- MIL STD 883 PROCESSING AVAILABLE

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5687 is a monolithic direct replacement for the popular DAC87-CBI wide temperature range d-to-a converter. Single chip construction, along with several design innovations make the HI-5687 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5687V), or with a user supplied external amplifier (HI-5687I).

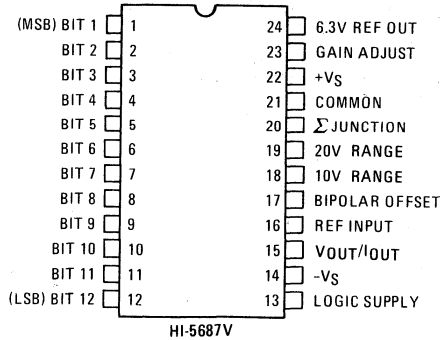
Internally, the HI-5687 eliminates code dependent ground currents by routing current from the positive supply to the internal ground mode, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5687 is available in both current and voltage output models which are 100% tested over the -55°C to +125°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

For additional Hi-Rel screening including a 160 hour burn-in, specify the "-8" suffix.

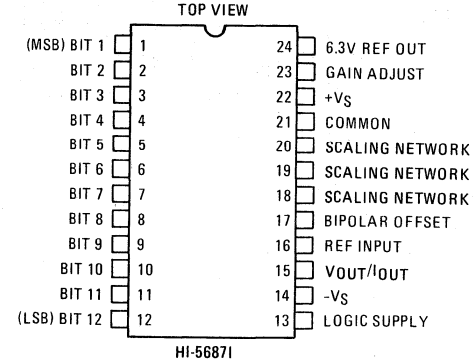
PINOUT

TOP VIEW



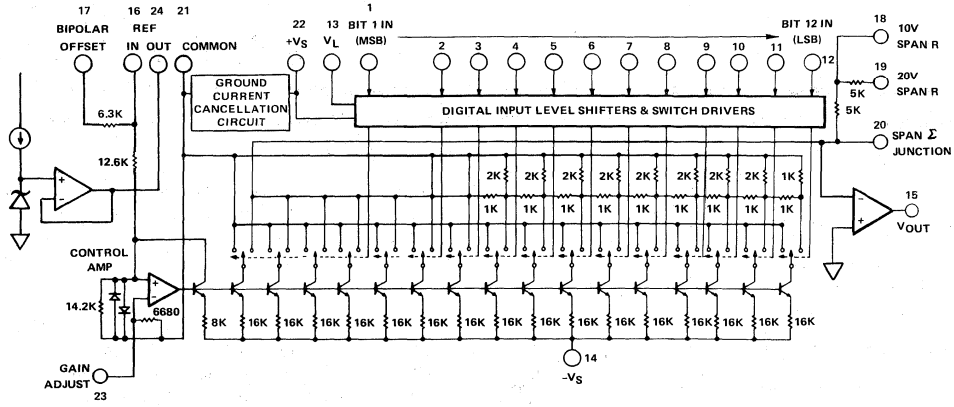
HI-5687V
VOLTAGE OUTPUT

TOP VIEW



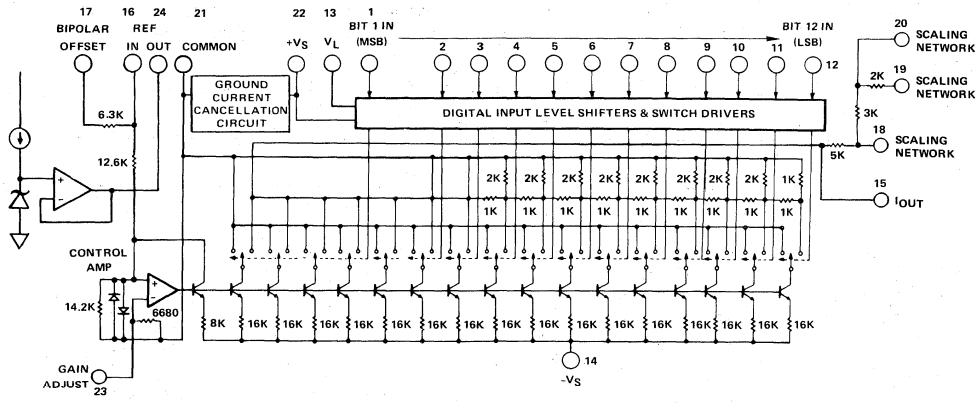
HI-5687I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5687 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5687 I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation	Pd, Package	1000mW
	$-V_S$	−20V			
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
				HI-5687I/V-2	−55°C to +125°C
Reference	Input (pin 16)	$\pm V_S$		HI-5687I/V-8	−55°C to +125°C
	Output drain	2.5mA			
			Storage Temperature Range		−65°C to +150°C
Digital Inputs	Bits 1 to 12	−1V to +12V			

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_S=±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5687 MIN	HI-5687 TYP	HI-5687 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1μA	+2		+5.5	V
Logic "0"	at −100μA	0		+0.8	V
ACCURACY (3)					
Linearity Error	At +25°C		±¼	±½	LSB
	−55°C to +125°C			+¾	LSB
Differential Lin. Error	at +25°C			±¾	LSB
	−55°C to +125°C		±½	±1	LSB (4)
Gain Error (2)			±0.1	±0.2	%FSR
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-55°C to +125°C		GUARANTEED		
DRIFT (3)	−55°C to +125°C				
Total Bipolar Drift (includes gain, offset and linearity drifts)			±15	±30	ppm/°C
Total Error (NOTE 6)					
Unipolar			±0.13	±0.3	%FSR
Bipolar			±0.12	±0.24	%FSR
Gain					
including internal reference			±10	±25	ppm/°C
excluding internal reference			±5	±10	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		μs

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5687 MIN	HI-5687 TYP	HI-5687 MAX	HI-5687 UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		+5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	–2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±5	±10	ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				±.002	$\frac{\%FSR}{\Delta V_S}$
–15V				±.002	
+5V				±.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
–15V		–11.4	–15	–16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
–15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5687 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and not be used if the supply voltages are less than ±12.5V.
6. With gain and offset errors adjusted to zero at 25°C.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

DIGITAL INPUTS

The HI-5687 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale
* Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C – T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C – T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5687 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

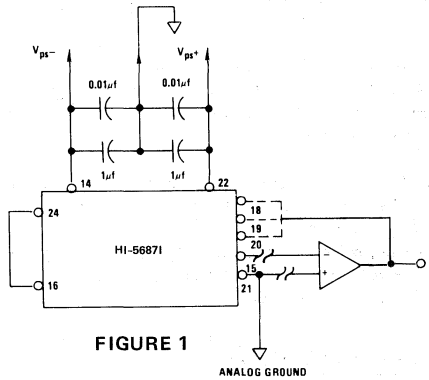


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5687 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5687. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5687V

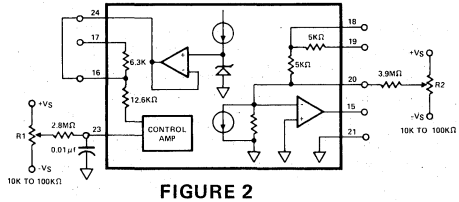


FIGURE 2

RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5687I

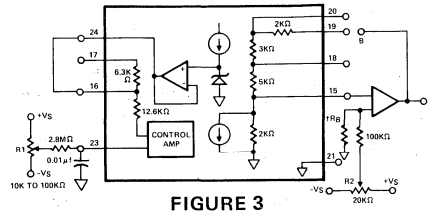


FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5687I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the, output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HARRIS

ADVANCE

HI-5690V

High Speed, 12 Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

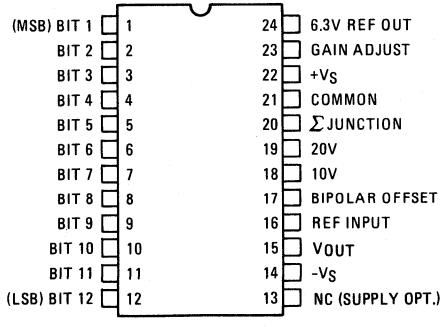
- IMPROVED REPLACEMENT FOR DAC 80
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING VOLTAGE OUTPUT 750ns
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5690 is a fast settling voltage output 12 bit digital to analog converter. Single chip construction makes this converter the optimum choice for low cost, high reliability applications. Also, the Harris unique Dielectric Isolation (DI) processing reduces internal parasitics to provide fast switching time and minimum glitch. Wafer level laser trimming of ladder and span resistors ensure high accuracy and exceptional tracking over temperature. All models include a low noise buried zener reference with low temperature coefficient, and a high speed on-board output amplifier.

Power requirements include $\pm V_S$, each with a range of 11.4V to 16.5V. Connection of a logic supply is optional, with TTL logic levels derived from the $\pm V_S$ supplies. The package is a 24 pin side brazed DIP.

MODEL	TEMP RANGE	INPUT CODE
HI-5690	0°C to +75°C	Complementary Binary
HI-5695	-25°C to +85°C	Complementary Binary
HI-5697	-55°C to +125°C	Complementary Binary

HARRIS

ADVANCE

HI-5695V

High Speed Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

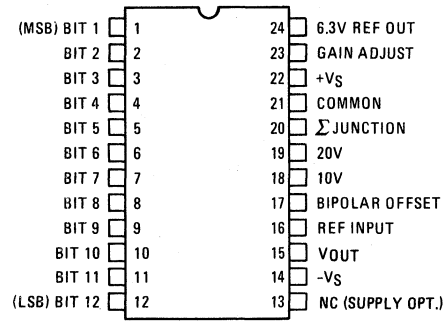
- IMPROVED REPLACEMENT FOR DAC 85
- PLUG COMPATIBLE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING VOLTAGE OUTPUT 600ns
- GUARANTEED MONOTONIC -25°C to +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5695 is a fast settling voltage output 12 bit digital to analog converter. Single chip construction makes this converter the optimum choice for low cost, high reliability applications. Also, the Harris unique Dielectric Isolation (DI) processing reduces internal parasitics to provide fast switching time and minimum glitch. Wafer level laser trimming of ladder and span resistors ensure high accuracy and exceptional tracking over temperature. All models include a low noise buried zener reference with low temperature coefficient, and a high speed on-board output amplifier.

Power requirements include $\pm V_S$, each with a range of 11.4V to 16.5V. Connection of a logic supply is optional, with TTL logic levels derived from the $\pm V_S$ supplies. The package is a 24 pin side brazed DIP.

MODEL	TEMP RANGE	INPUT CODE
HI-5690	0°C to +75°C	Complementary Binary
HI-5695	-25°C to +85°C	Complementary Binary
HI-5697	-55°C to +125°C	Complementary Binary

HARRIS

ADVANCE

HI-5697V

Wide Temperature Range High Speed Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

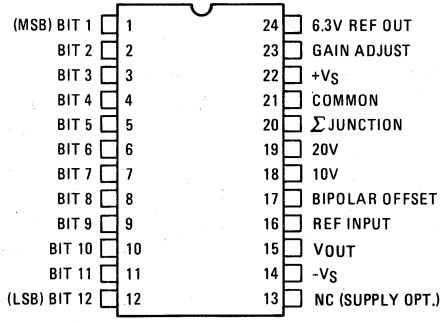
- IMPROVED REPLACEMENT FOR DAC 87
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING VOLTAGE OUTPUT 600ns
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5697 is a fast settling voltage output 12 bit digital to analog converter. Single chip construction makes this converter the optimum choice for low cost, high reliability applications. Also, the Harris unique Dielectric Isolation (DI) processing reduces internal parasitics to provide fast switching time and minimum glitch. Wafer level laser trimming of ladder and span resistors ensure high accuracy and exceptional tracking over temperature. All models include a low noise buried zener reference with low temperature coefficient, and a high speed on-board output amplifier.

Power requirements include $\pm V_S$, each with a range of 11.4V to 16.5V. Connection of a logic supply is optional, with TTL logic levels derived from the $\pm V_S$ supplies. The package is a 24 pin side brazed DIP.

MODEL	TEMP RANGE	INPUT CODE
HI-5690	0°C to +75°C	Complementary Binary
HI-5695	-25°C to +85°C	Complementary Binary
HI-5697	-55°C to +125°C	Complementary Binary

HARRIS

HI-7541

12 Bit Multiplying Monolithic Digital-to-Analog Converter

FEATURES

- FULL FOUR QUADRANT MULTIPLICATION
- .01% RELATIVE ACCURACY OVER TEMPERATURE
- LOW OUTPUT CAPACITANCE 100pF MAX
- TTL/CMOS COMPATIBLE
- MONOLITHIC CONSTRUCTION
- VERY LOW OUTPUT LEAKAGE CURRENT ±100nA MAX
- LOW GAIN ERROR 0.1%

APPLICATIONS

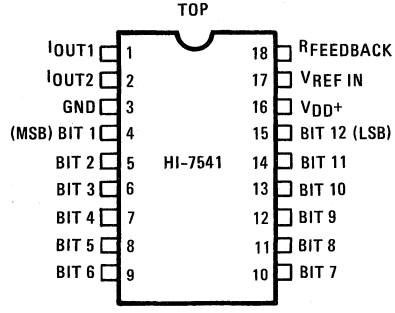
- PROGRAMMABLE GAIN AMPLIFIERS
- PROGRAMMABLE FUNCTION GENERATION

DESCRIPTION

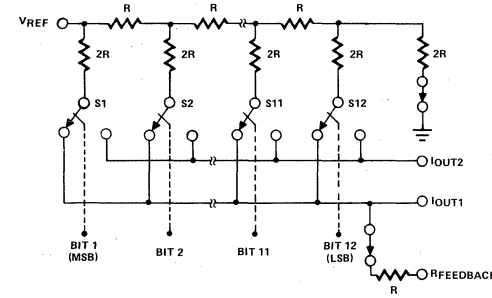
The Harris HI-7541 is a 12-Bit Monolithic Digital to Analog converter, offering full four quadrant multiplying capability. The chip features dielectrically isolated CMOS technology to assure fast settling time and freedom from latch-up. Included are thin film ladder and applications resistors, laser trimmed for accuracy over the full operating temperature range.

The HI-7541 is recommended as a high performance direct replacement for the AD7541 device. It operates on a single +15V supply and is available in an 18-pin ceramic package as well as in dice form. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT



FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL, TTL, CMOS COMPATIBLE)
LOGIC: A SWITCH IS CLOSED TO I_{OUT1} FOR ITS DIGITAL INPUT IN A HIGH (LOGIC 1) STATE.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)1

Power Supply Inputs V_{DD}	+17V	Power Dissipation (Package) up to +75°C	450mW
Reference Inputs VREF (Hi)	±25V	Derate above +75°C by 6mW/°C.	
Digital Input Range Bits 1-12	V_{DD} to GND	Operating Temperature Range	
		HI-7541SD/TD/SO	-55°C to +125°C
		HI-7541AD/BD	-25°C to +85°C
		HI-7541JN/KN/JO	0°C to +75°C
Output Voltage (Pins 1 and 2)	-400mV to V_{DD}	HI-7541SD/883 AND TD/883.	-55°C to +125°C
		Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@25°C, V_{DD} = +15V, V_{REF} = +10V Unless otherwise noted)

PARAMETER	CONDITIONS	HI-7541KN/BD/TD MIN	HI-7541KN/BD/TD TYP	HI-7541KN/BD/TD MAX	HI-7541JN/AD/SD/JO/SO MIN	HI-7541JN/AD/SD/JO/SO TYP	HI-7541JN/AD/SD/JO/SO MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON = "Logic 1" Bit OFF = " Logic 0"							
Input Voltage								
Logic 1, V_{AH}		2.4			2.4			V
Logic 0, V_{AL}				0.8			0.8	V
Input Current								
Logic 1	V_{IN}=15V			1			1	µA
Logic 0	V_{IN}=0V			-1			-1	µA
Reference Input								
Input Resistance		7	9	12	7	9	12	KΩ
Input Voltage		-10		+10	-10		+10	V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temp. Range	12			12			Bits
Integral (2) Nonlinearity	@+25°C Over Full Temp Range			±.01			±.02	%FSR
Differential (2) Nonlinearity	@ +25°C Over Full Temp Range			±.01			±.02	%FSR
Gain Error (2)	@ +25°C Over Full Temp. Range			± 0.1 ±0.15			±0.2 ±0.25	%FSR
Gain Tempco (2)(5)	Over Full Temp. Range			±5			±5	PPM/°C
Settling Time (2) (5) to ±1/2 LSB				1			1	µs
PSRR (2)	12.0V ≤ V_{DD} ≤ 16.0V Over Full Temp. Range			±.01 ±.02			±.01 ±.02	%FSR/ %ΔV_{DD}
OUTPUT CHARACTERISTICS								
Output (2) Leakage Current	V_{REF} = ±10V @ +25°C			±50			±50	nA
	Over Full Temp. Range			±100			±100	nA
Capacitance (2) (5)				100			100	pF
Feed Through (2)(5)	V_{REF} = 20 V_{pp} @ 10kHz			±1			±1	mVpp
POWER REQUIREMENTS								
V_{DD}	(See Fig. 6, 8 & 9)	+5	+15	+16	+5	+15	+16	V
I_{DD} (3)				2			2	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. After 30 seconds warm-up.
4. Specification's subject to change without notice.
5. Guaranteed by design, not tested.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

FEEDTHROUGH ERROR

Variation in V_{OUT} due to variation in V_{REF}, for the condition all bits OFF (zero output current).

GAIN

The gain is defined only when the MDAC is used with an output operational amplifier in which case it is V_{OUT}/V_{REF}.

POWER SUPPLY REJECTION RATIO (PSRR)

Variation in V_{OUT} due to variation in V_{DD}, expressed in %FSR/% V_{ps}.

OUTPUT CAPACITANCE

Measured capacity from I_{OUT1} or I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current leakage to ground from I_{OUT1} (all bits low) or I_{OUT2} (all bits high) with no connection to the span resistor (Pin 18).

OPERATING INSTRUCTIONS

BYPASSING AND GROUNDING

For best accuracy and high frequency performance the grounding and bypass scheme shown in Figure 1 should be used. Bypass capacitors should be connected close to the HI-7541 (preferably to the device pins) and should be tantalum in parallel with a smaller ceramic type for best high frequency noise rejection.

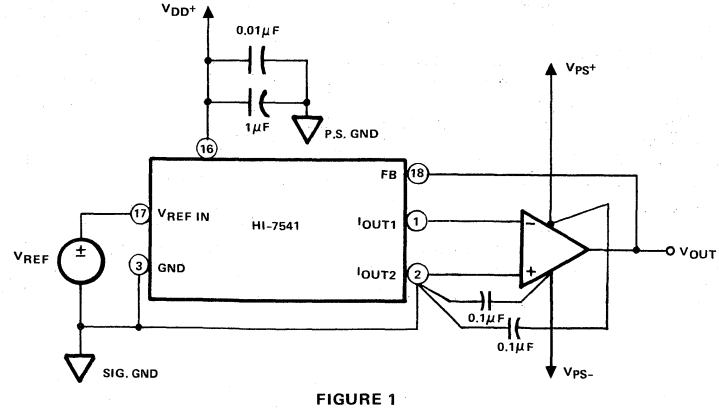
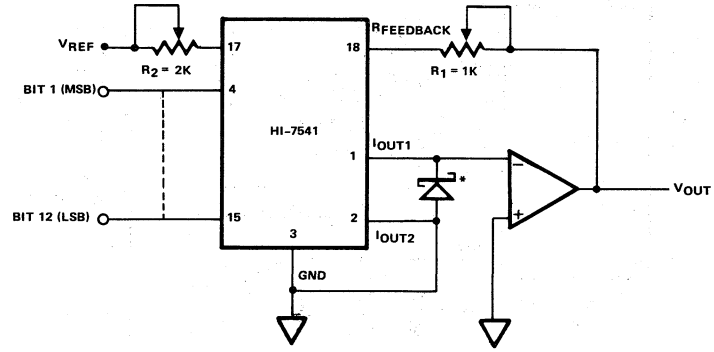


FIGURE 1

UNIPOLAR BINARY OPERATION

For most applications the HI-7541 requires an output operational amplifier, since both I_{OUT1} and I_{OUT2} should remain at ground potential to avoid linearity errors. Figure 2 shows the connections for unipolar straight binary operation. The calibration of gain will require either R_1 (to increase gain) or R_2 (to decrease gain), but not both. If both these resistors are omitted, the gain error is guaranteed not to exceed ±0.15% of full scale, over the military temperature range. See the "Offset" section for calibration of the error at zero.



*A Schottky diode to ground should be connected to I_{OUT1} or I_{OUT2}, for any application in which a negative voltage greater than 400mV may be applied. This can occur with certain high speed op amps, whose inverting input may offer a low impedance to the negative supply rail during turn-on of power.

For these applications, the HI-7541 output will source excessive current and suffer damage unless it is clamped with a Schottky diode (such as the HP5082-2811 or equivalent).

FIGURE 2

CODE TABLE- UNIPOLAR OPERATION

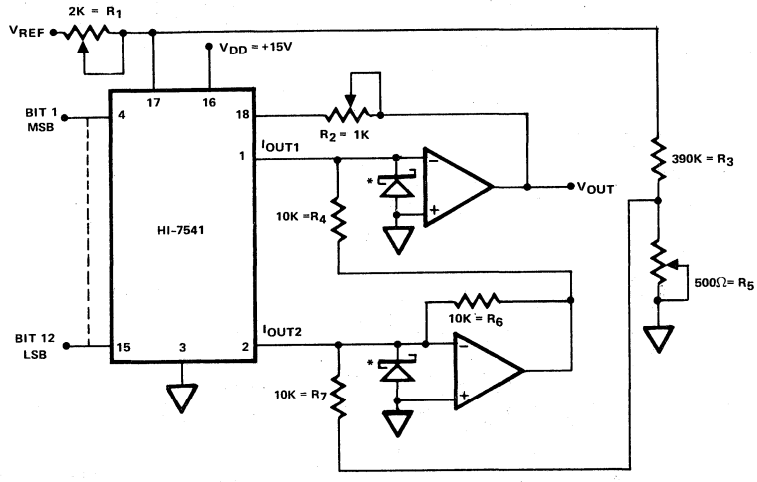
DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(1/2+2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}/2$
0	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1/2-2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	0	0

CODE TABLE - BIPOLAR (OFFSET) OPERATION

DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	$V_{REF}(2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	1	$V_{REF}(1-2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	0	V_{REF}

BIPOLAR (4-QUADRANT) BINARY OPERATION

Figure 3 shows the configuration for bipolar offset binary coded operation. As in the unipolar case, gain calibration requires either R_1 or R_2, but not both. The network $R_3/R_5/R_7$ assures that V_O = 0V at the zero (midrange) code 100000 000000, for which I_{OUT1} and I_{OUT2} differ by 1/2 LSB.



*A Schottky diode to ground should be connected to I_{OUT1} or I_{OUT2}, for any application in which a negative voltage greater than 400mV may be applied. This can occur with certain high speed op amps, whose inverting input may offer a low impedance to the negative supply rail during turn-on of power.

For these applications, the HI-7541 output will source excessive current and suffer damage unless it is clamped with a Schottky diode (such as the HP5082-2811 or equivalent).

FIGURE 3

OFFSET AND GAIN CALIBRATION

UNIPOLAR CALIBRATION (Fig. 2)	
Step 1:	Unipolar Zero Offset Adjustment • Turn all bits OFF (00...00) • Adjust offset trimpot (See Figure 5) for V_{OUT} = 0V.
Step 2:	Unipolar Gain Adjustment • Turn all bits ON (11...11) • Adjust R_1 or R_2 for an output of $V_{OUT} = -V_{REF}(1-2^{-12})$
BIPOLAR CALIBRATION (Fig. 3)	
Step 1:	Bipolar Offset Adjustment • Set V_{REF} = +10V • Turn all bits OFF (0000...00) • Adjust R_5 so that V_{OUT} = 10V
Step 2:	Bipolar Gain Adjustment • Set V_{REF} = +10V • Turn all bits ON (1111...11) • Adjust R_1 or R_2 so that V_{OUT} = -9.99512V

OPERATING INSTRUCTIONS

SELECTING AN OPERATIONAL AMPLIFIER

The outputs I_{OUT1} and I_{OUT2} must remain very close to ground potential for the HI-7541 to maintain its accuracy. Because of this constraint, most applications require selection of a suitable output op-amp. Harris Analog Products Division offers a wide range of high performance op-amps which are well suited to a variety of applications.

COMPENSATION

In the standard configurations of Figures 1 and 2 the output capacitance of the MDAC along with the feedback resistance introduces a pole in the open loop response of the system. This pole may cause undesirable phase shift leading to excessive ringing or even oscillation. The phase shift may be compensated by placing a capacitor in the feedback loop. Figure 4 shows this scheme. The compensation is exact for $R_oC_o = R_{FB}C_{FB}$. This is a special case, however, since both Ro and Co are dependent on the digital code for a CMOS MDAC.

A practical approach is to turn all bits of the MDAC ON while applying a square wave of appropriate magnitude to the reference input. Then select a feedback capacitor which gives approximately 20% of overshoot, which is equal to a 45° Phase Margin. This form of compensation reduces the overall bandwidth of the system, which is dependent on the op amp selected.

MDAC EQUIVALENT CIRCUIT WITH COMPENSATION

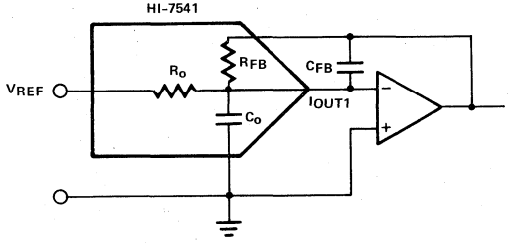


FIGURE 4

OP AMP PARAMETERS

The addition of the output amplifier has a direct effect on many of the MDAC parameters, including bandwidth, settling time, accuracy and tempco. Settling time is difficult to measure for the HI-7541 since the current outputs have almost no voltage compliance. The output settling time of the MDAC-OP AMP system can be measured; and if the settling time of the Op Amp itself is known, that of the MDAC can be estimated by the Root-Sum of Squares method;

$$T_{MDAC} = \sqrt{T^2_{MDAC/AMP} - T^2_{AMP}}$$

The bandwidth of the MDAC itself can be approximated by modeling it as a voltage source (V_{ref}) followed by a series resistance (Ro) and capacitance (Co) as in figure 4. The half-power frequency then is;

$$f = \frac{1}{2\pi RoCo}$$

If R_O = 10KΩ and C_O = 50pf then f = 318KHz. However, an output amplifier virtually eliminates C_O by maintaining zero volts across it, thus extending the DAC/amplifier bandwidth almost to that of the amplifier alone.

TABLE 1 HARRIS OP AMPS (TYPICAL AT T_A = +25°C)

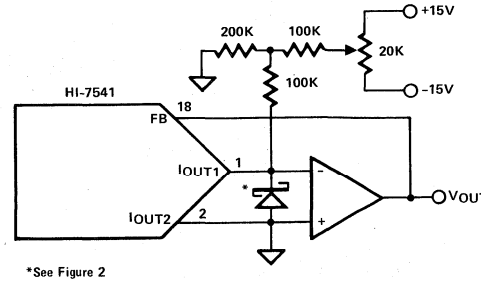
Op Amp HA-	Full Power B. W.	Offset Voltage	Offset Voltage Drift	Bias Current	C_{FB}* Compensation for 45° P.M.	Settling Time**
2600	75KHz	500μV	5μV/°C	1nA	20pf	1.5μs
2525	1.6MHz	5mV	30μV/°C	125nA	12pf	200ns
5100	150KHz	500μV	5μV/°C	20pA	18pf	1.7μs
5130	600KHz	100μV	1μV/°C	1nA	30pf	11μs
5190	6.5MHz	3mV	20μV/°C	5μA	2pf	70ns

* For standard configuration such as Figure 3. Vref equals 1KHz 10V peak to peak square wave.

** For the Op Amp alone. A_{VCL} = -1, 10V step to 0.1%.

OFFSET

The amplifier's Offset Voltage V_{OS} contributes a code dependent output error, since V_{OS} is multiplied by a gain factor (1 + R_F/R_{OUT}) in which R_{OUT} is code dependent. R_{OUT} ranges from 10kΩ to 30kΩ for nonzero input codes. R_F is 10kΩ , which leads to an output error variation of 2/3 V_{OS} (from 4/3 V_{OS} to 2 V_{OS}).



*See Figure 2

FIGURE 5

OPERATING INSTRUCTIONS (Continued)

This effect applies for offset introduced at the noninverting terminal as well as V_{OS} inherent in the amplifier. Therefore, the common technique of nulling V_{OS} (due to bias current) with a resistor from the noninverting input to ground is not recommended. Instead, choose an amplifier with low V_{OS} (200μV or less) and low I_{BIAS} (75nA or less), and connect the noninverting input directly to ground. The HA-5130 and HA-5170 are recommended for these high accuracy applications.

Output Leakage Current from the HI-7541 flows through the feedback resistor to create another type of offset error. This leakage is insignificant except at high temperature, where the maximum output error is one millivolt. To null this error, inject an opposing current at the summing junction using a network as shown in Figure 5. All lead lengths connecting to I_{OUT1} should be short, to minimize capacitance to ground and maintain a fast settling time.

PERFORMANCE CURVES

GAIN ERROR vs. SUPPLY VOLTAGE

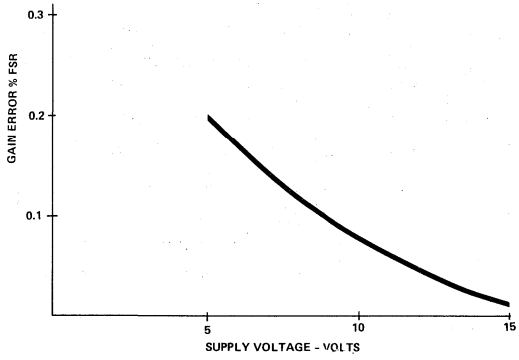


FIGURE 6

FEEDTHROUGH ERROR vs. FREQUENCY

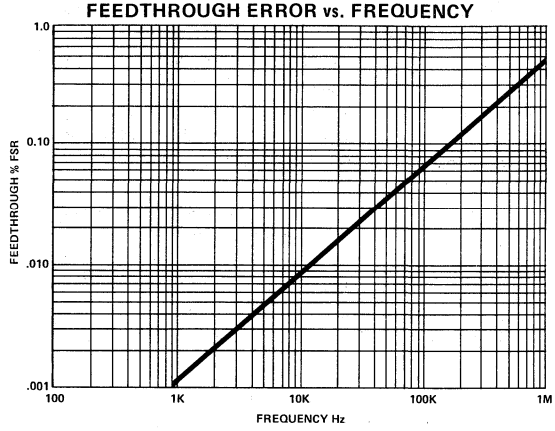


FIGURE 7

LINEARITY vs. SUPPLY VOLTAGE

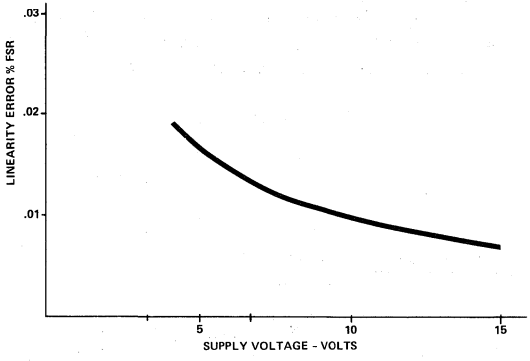


FIGURE 8

SUPPLY CURRENT vs. SUPPLY VOLTAGE

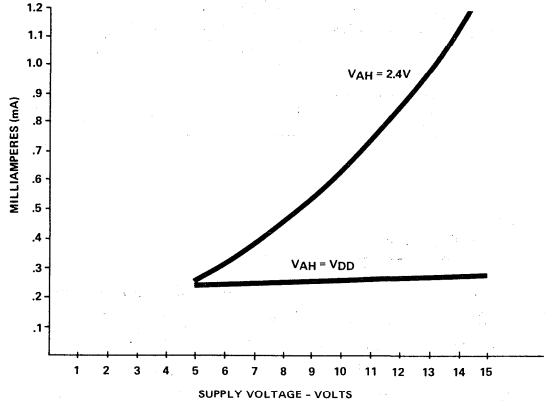


FIGURE 9

DIE CHARACTERISTICS

Transistor Count		198	Tie Substrate to:	Ground
Die Size:		113 x 101 mils	Process:	CMOS - DI
Thermal Constants;	θ_{ja}	82°C/W		
	θ_{jc}	23°C/W		

HARRIS

HI-DAC16B/DAC16C

16-Bit D to A Converter

FEATURES

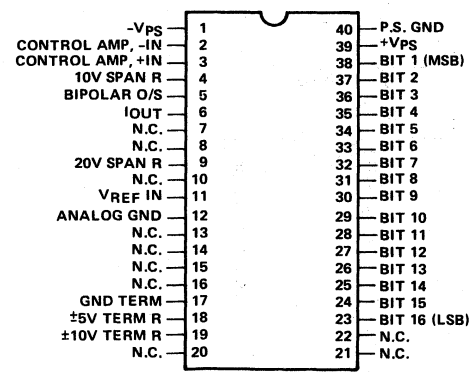
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ±0.3ppm/°C
- LOW GAIN DRIFT — ±1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤1/2LSB@+25°C
- LOW UNIPOLAR OFFSET T.C. — ±0.2ppm/°C
- EXCELLENT STABILITY

APPLICATIONS

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

PINOUT

TOP VIEW



DESCRIPTION

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V. The HI-DAC16B is monotonic to 15 bits; and the HI-DAC16C to 14 bits.

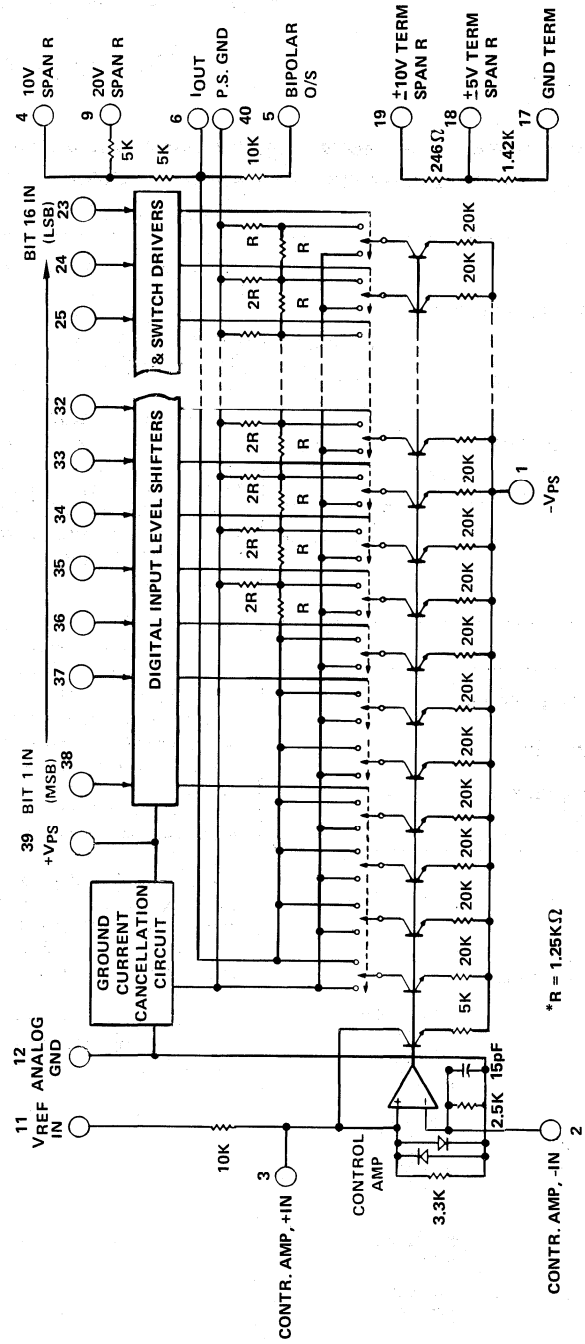
Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Two accuracy grades are offered, and typical power dissipation is 450mW. Package is a 40 pin ceramic DIP. For further information, see Application Note 539.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V	Power Dissipation Pd, Package	1000 mW
	$V_{ps}-$	−20V	Operating Temperature Range	
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$		
Digital Inputs	Bits 1 to 16	−1V, +12V	HI-DAC 16B/C	0°C to +75°C
Outputs		$\pm V_{ps}$	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Full Temperature Range	2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		-50			-50			μA
Reference Input								
Input Resistance			10			10		KΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Full Temperature Range		16			16		Bits
Nonlinearity	25°C		±0.0023			±0.0045		%FSR(3)
	Full Temperature Range			±0.0045			±0.009	
Differential Nonlinearity	25°C		±0.0015			±0.003		%FSR
	Full Temperature Range			±0.003			±0.006	
Relative Accuracy (5)	With 100Ω(1%) Trim Resistors							
Unipolar Gain Error	All Bits ON		±0.1	±0.25		±0.1	±0.25	
Bipolar Offset Error	All Bits OFF		±0.15	±0.43		±0.15	±0.43	%FSR
Unipolar Offset Error			±0.002	±0.05		±0.002	±0.05	
Adjustment Range	See Operating Instructions							
Gain	Using Trim Potentiometers			±3			±3	%FSR
Bipolar Offset	as shown in Figure 1			±0.43			±0.43	
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Full Temperature Range		±1	±5		±1	±5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±0.2			±0.2		
Bipolar Offset			±0.5			±0.5		
Differential Nonlinearity	Full Temperature Range		±0.3			±0.3		
Settling Time (2) to ±0.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	HI-DAC16B			HI-DAC16C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Glitch (2)	From 0111 . . .1 to 100 . . . 0 or 100 . . . 0 to 011 . . . 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3)								
V_{ps}+			1.5			1.5		ppm of FSR/% V_{ps}
V_{ps}-			1.5			1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2	-2.4	-1.6	-2	-2.4	mA
Bipolar		±0.8	±1	±1.2	±0.8	±1	±1.2	
Resistance			2.5k			2.5k		
Capacitance			10			10		pF
Output Voltage Ranges	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5			0 to +5		
Unipolar			0 to +10			0 to +10		V
			±2.5			±2.5		
Bipolar			±5			±5		
			±10			±10		
Compliance Limit (2)		-3		+10	-3		+10	V
Compliance Voltage (2)	Full Temperature Range		±1			±1		V
Output Noise	0.1 to 5MHz (All bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
V_{ps}+ (7)	Full Temperature Range	13.5	+15	16.5	13.5	+15	16.5	V
V_{ps}-		-13.5	-15	-16.5	-13.5	-15	-16.5	
I_{ps}+ (4)	All Bits ON or OFF		+13	+18		+13	+18	mA
I_{ps}- (4)	Full Temperature Range	-25	-18		-25	-18		
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	Zero − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON−OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

OPERATING INSTRUCTIONS

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

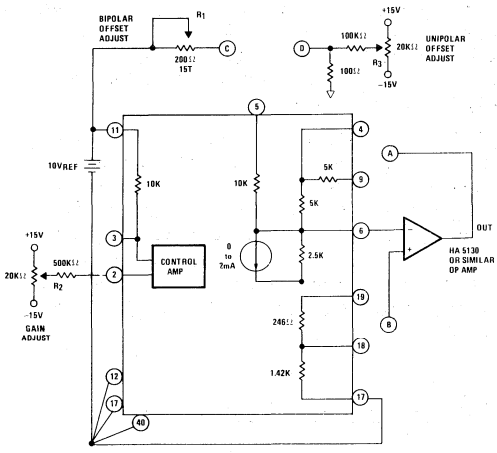


TABLE 1

	OUTPUT RANGE	CONNECTIONS			
		PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI-DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1 LSB

That is, adjust for:

9.999847 for +10V range
4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset

Turn all bits OFF (00..0)
Adjust R_1 for an output of
−10V for ± 10V range
−5V for ± 5V range
−2.5V for ± 2.5V range

Step 2: Gain

Turn all bits ON (11..1)
Adjust R_2 for FS-1LSB output
That is, adjust for:

9.999695 for ±10V range
4.999847 for ± 5V range
2.499924 for ± 2.5V range

OTHER CONSIDERATIONS

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI–DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI–DAC16 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

THERMAL EFFECTS

A consideration when using the DAC16 is Temperature Stability. In applications where full scale shift could be a problem, the use of a heat sink and/or a cooling fan is suggested. This will decrease the magnitude of the total variation by lowering the effective thermal resistance between the package and its environment. The device should be kept in a stable isothermal environment, and a warm-up time consistent with accuracy requirements should be provided.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an op-amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4 μV/°C leading to an error over temperature of 30 μV (0.0003% FSR for a 10V FS). Initial offset and bias current are 10 μV and 3nA respectively, while input noise current of 0.2pA/ $\sqrt{Hz}$. Settling time is adequate for most audio applications. (11 μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

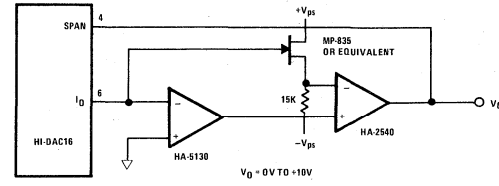


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

Offset; $$V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$$

Bias; $$I_{BIAS} = I_{BIAS2} + I_{BIAS1}$$

Gain; $$\frac{V_0}{V_1} = A_V(S) = A_{V2}(S)\,[1 + A_{V1}(S)]$$

The amplifier A_2 should be of wide bandwidth and fast settling time.

DIE CHARACTERISTICS

Transistor Count		190
Die Size:		215 x 125 mils
Thermal Constants;	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

ANALOG

Sample and Hold Amplifiers and Signal Processors

7

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Product Index

HA-2420-1	High Temperature Sample and Hold Amplifier	7-5
HA-2420/2425	Fast Sample and Hold	7-10
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier	7-17
HA-5330	High Speed Precision Monolithic Sample and Hold Amplifier	7-24
HI-5900	Analog Data Acquisition Signal Processor	7-25
HI-5901	Analog Data Acquisition Signal Processor	7-31

Selection Guide

SAMPLE AND HOLD

Part Number	Multiplexer	Temperature Range	Package	Acquisition Time, (to 0.01%) Typ., 25°C	Charge Transfer Typ., 25°C	Aperture Time Typ., 25°C	Gain Bandwidth Product Typ., 25°C	Page
HA1-2420-1 HA1-2420-2 HA1-2425-5	Fast Low charge transfer Low droop rate	200°C Mil Com	14 pin Cerdip*	5μs	5pC	30ns	2.5MHz	7-5 7-10 7-10
HA1-5320-2 HA1-5320-5	High speed Precision Complete-includes hold capacitor	Mil Com	14 pin Cerdip	1μs	0.1pC	25ns	2.0MHz	7-17 7-17
HA1-5330-2 HA1-5330-5	High speed Precision Complete-includes hold capacitor	Mil Com	14 pin Cerdip	0.4μs	0.05pC 0.05pC	25ns	6.5MHz	7-24 7-24

* Leadless chip carriers available.

SIGNAL PROCESSOR FRONT END

Part Number	Number of Channels	Temperature Range	Gain Error, Max for All Gains Full Temp.	Hold Mode Feed Through (C_H = 1000pF, $20V_{p-p}$, 1kHz)	Droop Rate (C_H = 1000pF) Full Temp.	CMRR Full Temp.	Aperture Delay Typ. 25°C	Aperture Uncertainty Typ. 25°C	Page
HI5-5900-2	8 differential	Mil	0.1%	-76dB	20nV/μs	80dB	50ns	5ns	7-25
HI5-5900-5	8 differential	Com	0.2%	-76dB	5nV/μs	74dB	50ns	5ns	7-25
HI5-5901-2	16 single-ended	Mil	0.1%	-76dB	20nV/μs	80dB	50ns	5ns	7-31
HI5-5901-5	16 single-ended	Com	0.2%	-76dB	5nV/μs	74dB	50ns	5ns	7-31

HARRIS

HA-2420-1

High Temperature Sample and Hold Amplifier

FEATURES (T_A = 200°C)

- LOW DROOP RATE (C_H = 0.01μF) — 22μV/μs
- FAST ACQUISITION TIME (±0.01%) — 5μs
- HIGH SLEW RATE — 7V/μs
- WIDE BANDWIDTH — 2.5MHz
- LOW EFFECTIVE APERTURE DELAY TIME — 30ns
- TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- GEOTHERMAL AND NUCLEAR INSTRUMENTATION
- OIL WELL LOGGING
- AUTOMOTIVE ENGINE MONITORING
- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420-1 is a monolithic sample-and-hold amplifier guaranteed to operate over the -55°C to +200°C temperature range. The circuit consists of a high performance operational amplifier in series with an ultra low leakage analog switch and a MOSFET input unity gain output buffer amplifier.

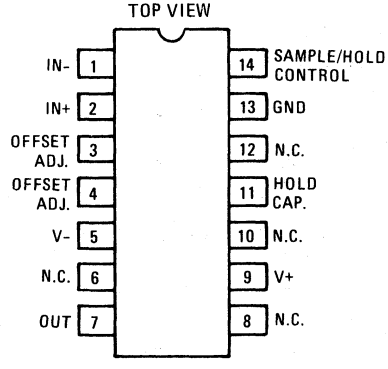
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened, the output will remain at its last level.

Performance as a sample-and-hold at 200°C compares very favorably with other monolithic, hybrid and discrete circuits having lower temperature ranges. High slew rate, wide bandwidth, and low acquisition time provide an excellent dynamic response. The ability to operate at gains other than unity eliminate the need for an external scaling amplifier.

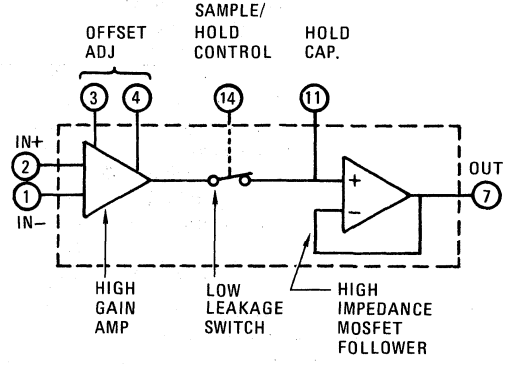
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, multiplexed sample-and-holds, etc.

Power requirement is ± 15V. The package is a 14 pin ceramic DIP.

PINOUT



FUNCTIONAL DIAGRAM



7 S/H AMPS & SIG. PROCESSORS

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW
Differential Input Voltage	±24V	Operating Temperature Range	-55°C ≤ T_A ≤ +200°C
Digital Input Voltage (Pin 14)	+8V, -15V	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C
Output Current	Short Circuit Protected		

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input (Pin 14), V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold)

PARAMETER	TEMP	HA-2420-1 MIN	HA-2420-1 TYP	HA-2420-1 MAX	UNITS
INPUT CHARACTERISTICS					
*Offset Voltage	+25°C		2	4	mV
	Full		3	6	mV
*Bias Current	+25°C		50	200	nA
	Full			400	nA
*Offset Current	+25°C		10	50	nA
	Full			100	nA
Input Resistance	+25°C	5	10		MΩ
Common Mode Range	Full	±10			V
TRANSFER CHARACTERISTICS					
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		dB
Hold Mode Feedthrough Attenuation (Note 8)	+25°C		-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5		MHz
OUTPUT CHARACTERISTICS					
*Output Voltage Swing (Note 1)	Full	±10			V
Output Current	+25°C	±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100		kHz
Output Resistance (D.C.)	+25°C		.15		Ω
TRANSIENT RESPONSE					
Rise Time (Note 3, 5)	+25°C		50		ns
Overshoot (Note 3, 5)	+25°C		25		%
Slew Rate (Note 3, 6)	+25°C		7		V/μs
DIGITAL INPUT CHARACTERISTICS					
Digital Input Current (V_{IN} = 0V)	Full			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20	μA
Digital Input Voltage (Low)	Full			0.8	V
Digital Input Voltage (High)	Full	2.0			V
SAMPLE/HOLD CHARACTERISTICS					
Acquisition Time to .1% 10V Step (Note 3)	+25°C		4		μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		5		μs
Aperture Time	+25°C		30		ns
Effective Aperture Delay Time	+25°C		30		ns
Aperture Uncertainty Time	+25°C		5		ns
*Drift Current (Note 3, 7)	+25°C		5	50	pA
	Full		220		nA
*Hold Step Error (Note 7)	+25°C		9	15	mV
POWER SUPPLY CHARACTERISTICS					
*Supply Current (+)	Full		5.5	7	mA
*Supply Current (-)	Full		4.5	6	mA
*Power Supply Rejection	Full	80	90		dB

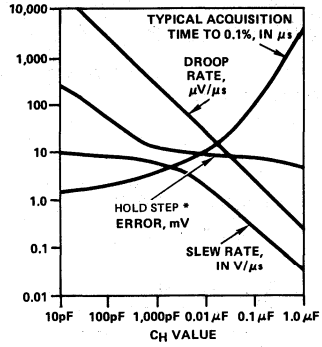
NOTES:
1. R_L = 2kΩ
2. V_{CM} = ±10VDC
3. A_V = +1, R_L = 2kΩ, C_L = 50pF
4. V_{OUT} = 20V peak-to-peak
5. V_{OUT} = 400mV peak-to-peak
6. V_{OUT} = 10.0V peak-to-peak
7. V_{IN} = 0V
8. f_{IN} ≤ 100kHz

*100% Tested

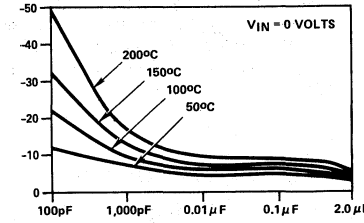
PERFORMANCE CURVES

$V_{SUPPLY} = \pm 15V$, $C_H = 1{,}000pF$, $T_A = +200^oC$, unless otherwise specified.

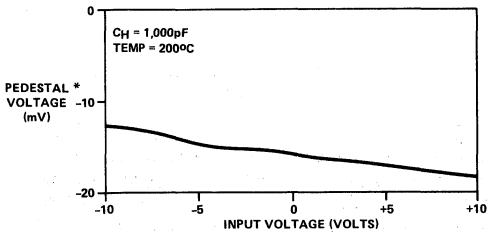
TYPICAL PERFORMANCE VS. HOLD CAPACITANCE



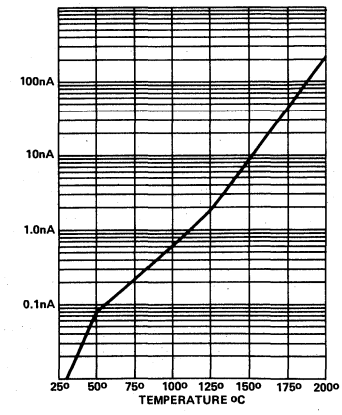
HOLD STEP VOLTAGE * VS. HOLD CAPACITANCE



HOLD STEP VOLTAGE * VS. INPUT VOLTAGE



DRIFT CURRENT VS. TEMPERATURE



*Hold step voltage is the output error following a switch from sample to hold.

APPLICATIONS

Operation of the HA-2420-1 at +200°C is similar to that of the -2 version at +125°C. Most of the maximum limits are the same, except for slight increases in supply and input bias currents, and a 55X increase in drift current. (Drift current is responsible for voltage droop error in the HOLD mode.) At high temperatures, a guard ring is essential, to counteract the increased flow of drift current from the hold capacitor. See Figure 2.

The components and materials external to this integrated circuit must carry a similar qualification for high temperature operation. TEFLON® * wire insulation and a TEFLON IC socket (if used) are recommended, along with TEFLON dielectric for the bypass and hold capacitors. In addition, the holding capacitor should have extremely high insulation resistance and low dielectric absorption.

Figure 1 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420-1. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

For more applications, consult Harris Application Note 517, or factory applications group.

BASIC SAMPLE-AND-HOLD
(TOP VIEW)

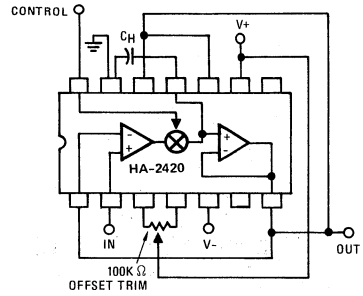


Figure 1

GUARD RING LAYOUT
(BOTTOM VIEW)

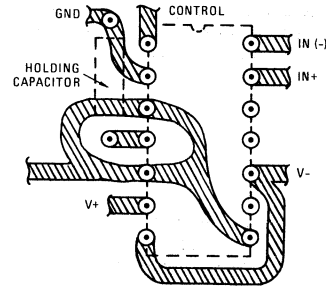


Figure 2

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ± 0.1% or ± 0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

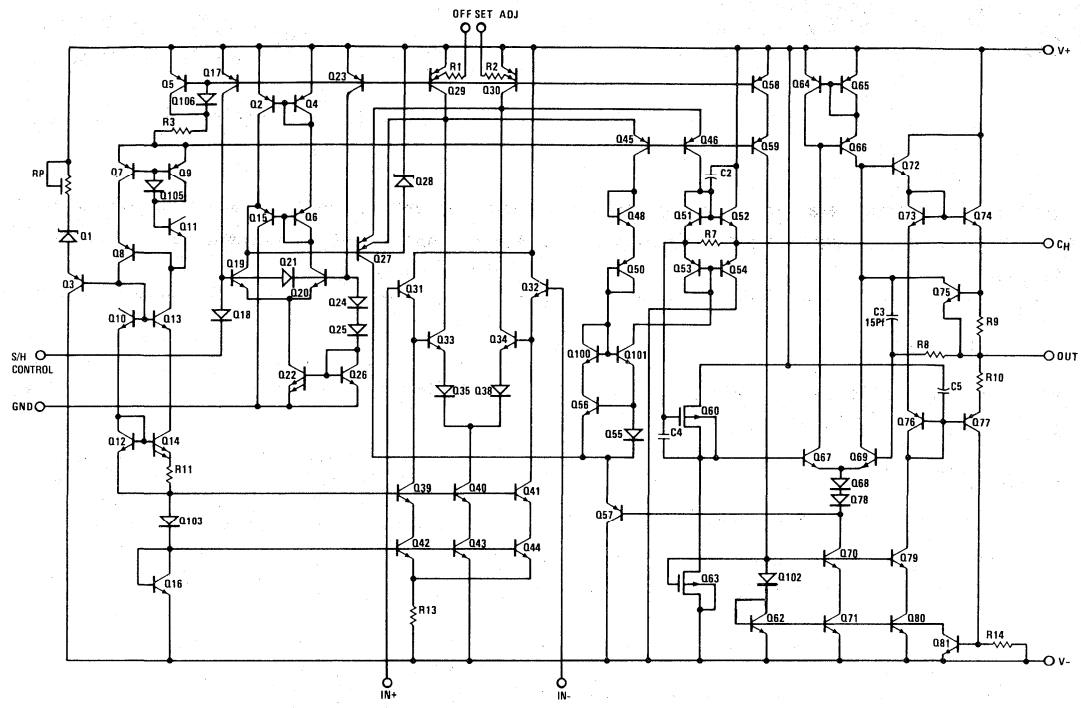
DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (Volts/sec)$$

* TEFLON is a registered trademark of Dupont Corporation

SCHEMATIC



DASH 1 PRODUCT FLOW

HARRIS SEMICONDUCTOR DASH 1 PRODUCT FLOW
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND
1	Internal Visual	2010 Cond. B
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests
11	Final Electrical	Harris Specifications @ +200°C

HARRIS

HA-2420/2425

Fast Sample and Hold

FEATURES

- LOW DROOP RATE (C_H = 1000pF) 5μV/ms
- FAST ACQUISITION TIME (10V STEP TO .01%) 5μs
- HIGH SLEW RATE 7V/μs
- BANDWIDTH 2.5MHz
- LOW EFFECTIVE APERTURE DELAY TIME 30ns
- TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

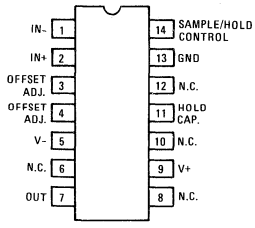
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

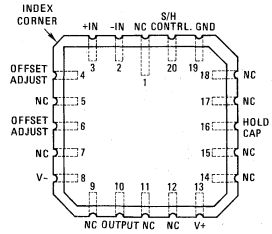
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note number 517.

PINOUT

TOP VIEW

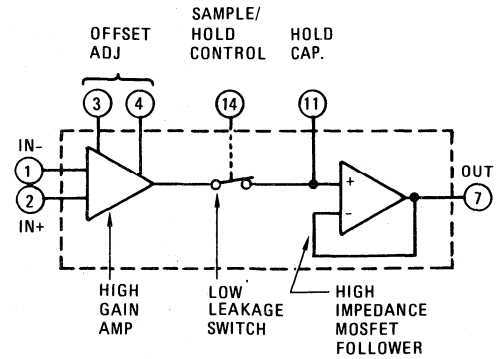


14 PIN DIP



LEADLESS CHIP CARRIER (LCC) PACKAGE

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	
Differential Input Voltage	±24V	HA-2420-2/8	$-55^{o}C \leq T_A \leq +125^{o}C$
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2425-5	$0^{o}C \leq T_A \leq +75^{o}C$
Output Current	Short Circuit Protected	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$
Internal Power Dissipation	300mW (Note 7)		

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5 MIN	HA-2425-5 TYP	HA-2425-5 MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		40	200		40	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	-80	-90		-74	-90		dB
Hold Mode Feedthrough Attenuation (Note 9)	Full		-76			-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5			2.5		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±15			±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100			100		kHz
Output Resistance (D.C.)	+25°C		.15			.15		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		50	75		50	75	ns
Overshoot (Note 3, 5)	+25°C		25	40		25	40	%
Slew Rate (Note 3, 6)	+25°C	5	7		3	7		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			-0.8			-0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (Note 3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		5			5		μs
Aperture Time (Note 10)	+25°C		30			30		ns
Effective Apeture Delay Time	+25°C		30			30		ns
Aperture Uncertainty	+25°C		5			5		ns
*Drift Current (Note 3, 8)	+25°C		5	50		5	50	pA
	Full		0.5	4.0		0.5	1.0	nA
*Hold Step Error (Note 8)	+25°C		10	20		10	20	mV
POWER SUPPLY CHARACTERISTICS								
*Supply Current (+)	+25°C		3.5	5.5		3.5	5.5	mA
*Supply Current (-)	+25°C		2.5	3.5		2.5	3.5	mA
*Power Supply Rejection	Full	-80	-90		-74	-90		dB

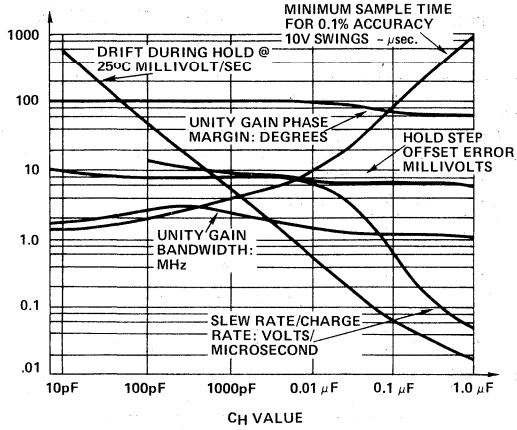
NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
4. V_{OUT} = 20V peak-to-peak
5. V_{OUT} = 200mV peak-to-peak
6. V_{OUT} = 10.0V peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature
8. V_{IN} = 0V. See Figure 4.
9. $f_{IN} \leq 100kHz$
10. Derived from computer simulation only; not tested.

*100% Tested for DASH 8

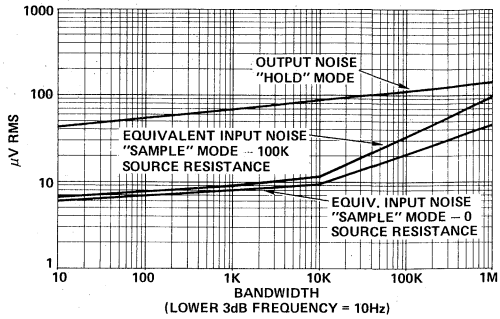
PERFORMANCE CURVES

V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF Unless Otherwise Specified

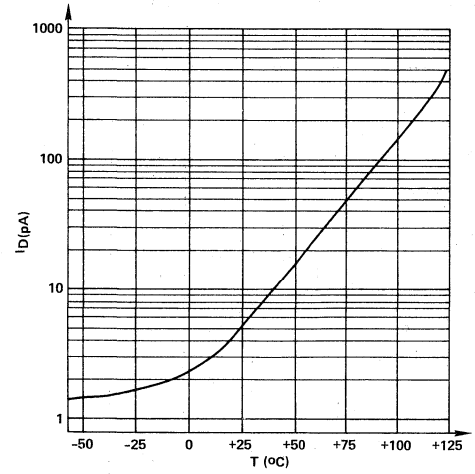
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



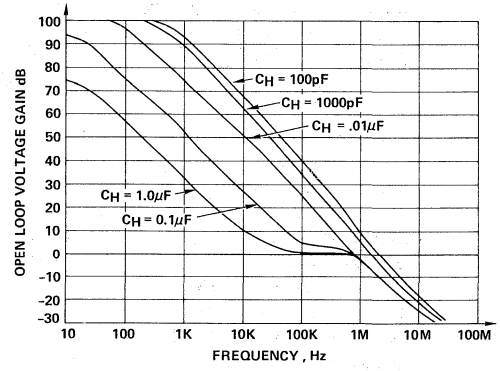
BROADBAND NOISE CHARACTERISTICS



DRIFT CURRENT VS. TEMPERATURE

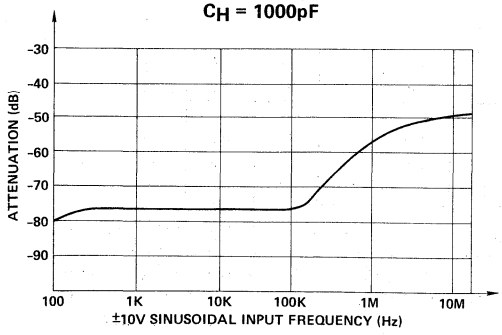


OPEN LOOP FREQUENCY RESPONSE

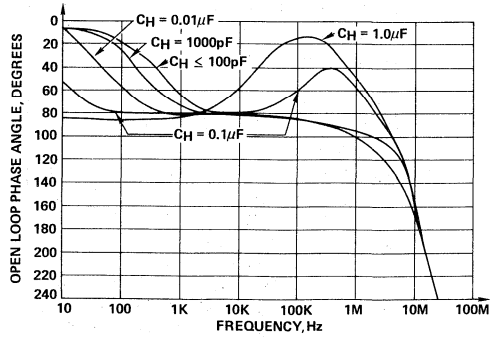


HOLD MODE FEED THROUGH ATTENUATION

C_H = 1000pF



OPEN LOOP PHASE RESPONSE



HOLD STEP VS. INPUT VOLTAGE

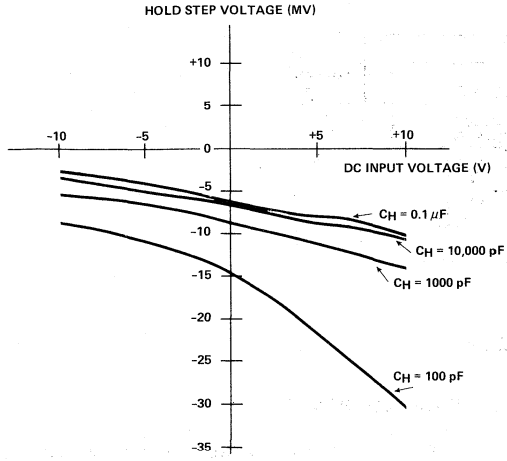


Figure 1

OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the S/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL})+(-10V)}{2}$$

INVERTING CONFIGURATION

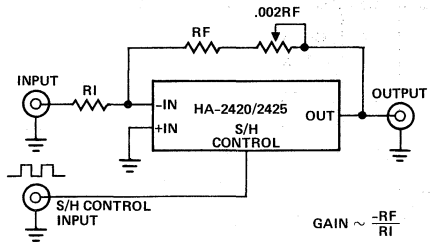


Figure 2

NONINVERTING CONFIGURATION

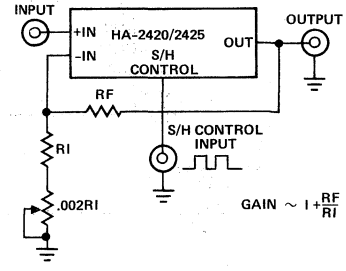


Figure 3

CHARGE TRANSFER AND DRIFT CURRENT

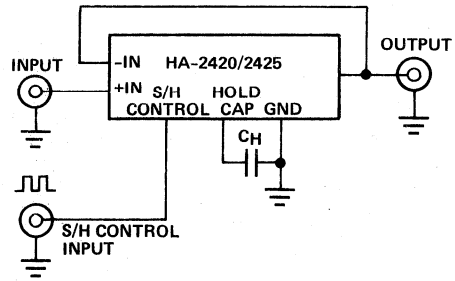
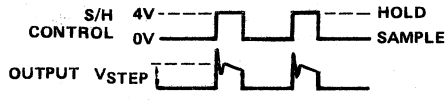


Figure 4

HOLD STEP ERROR TEST

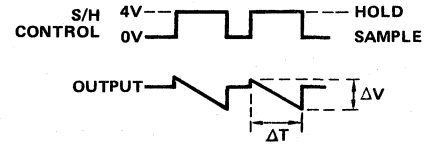
1. With a D.C. input voltage, observe the following waveforms:



2. Set rise/fall times of S/H Control to approximately 20 ns.

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$

HOLD MODE FEEDTHROUGH ATTENUATION

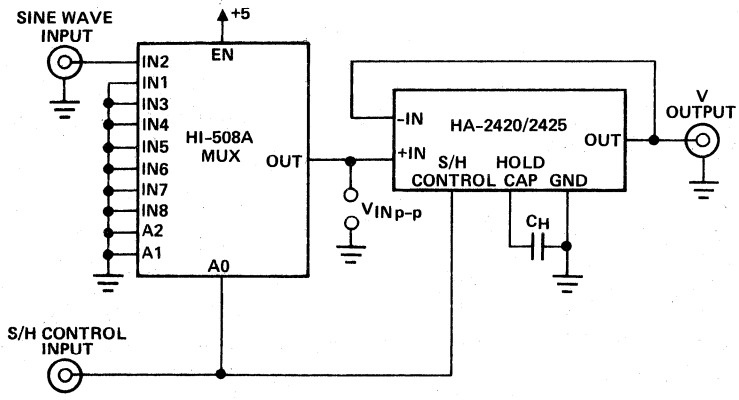


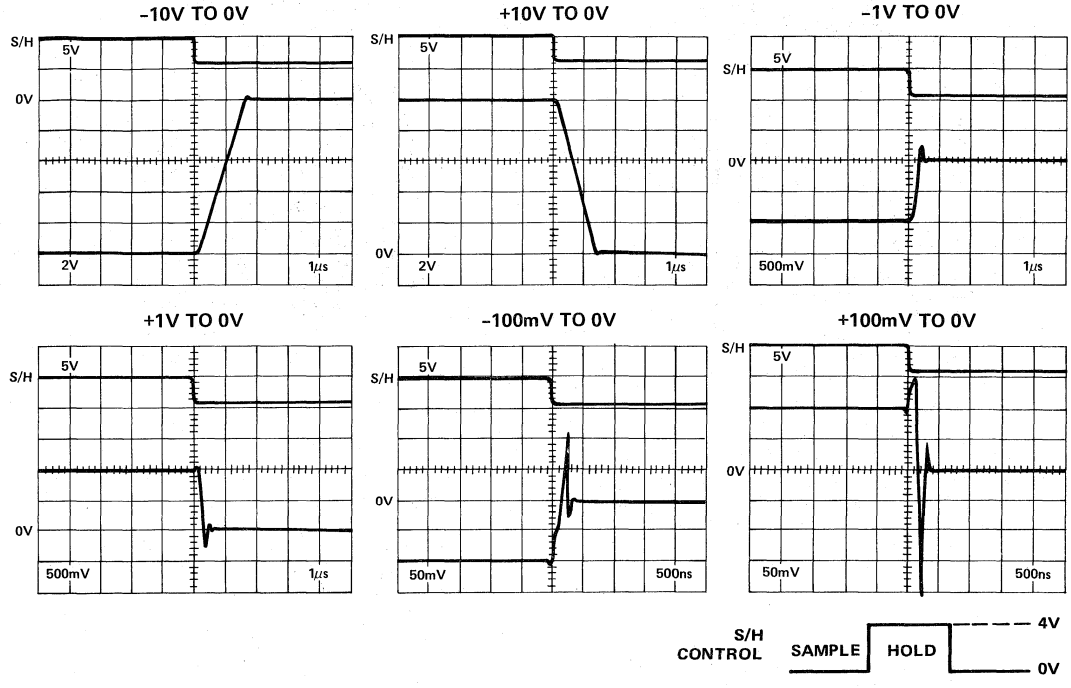
Figure 5

NOTE: Compute hold mode feedthrough attenuation from the formula:

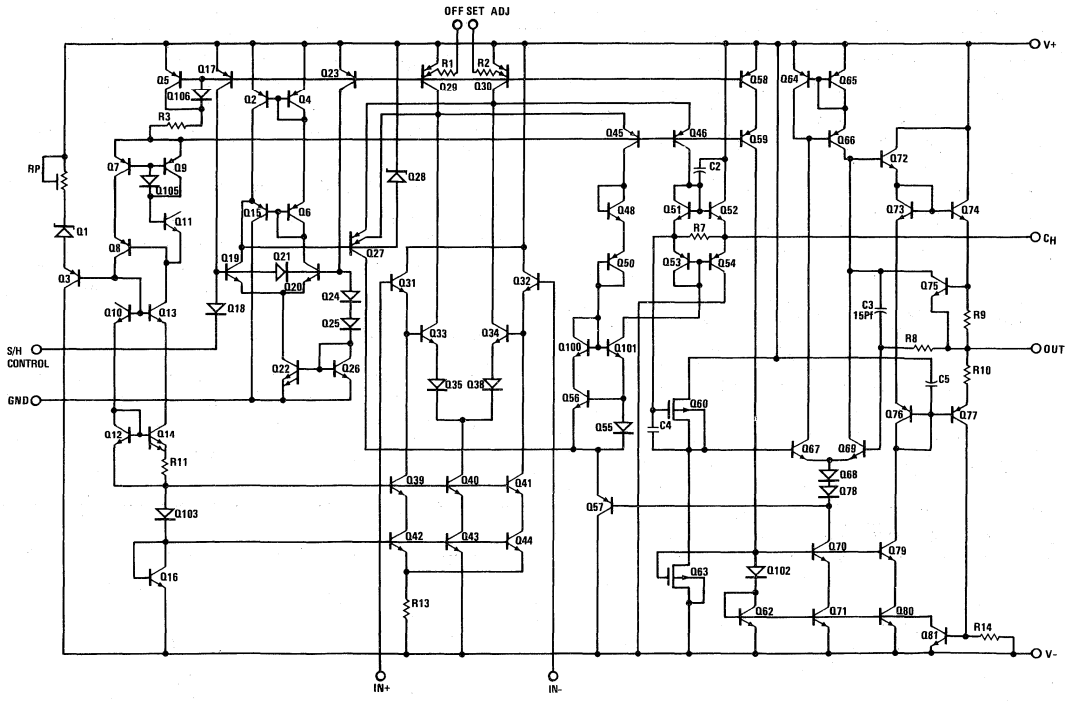
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}}$$

Where $V_{OUT\ HOLD}$ = Peak-Peak value of output sinewave during the hold mode.

ACQUISITION TIMES (C_H = 1000pF)



SCHEMATIC



APPLICATIONS

BASIC SAMPLE-AND-HOLD
(TOP VIEW)

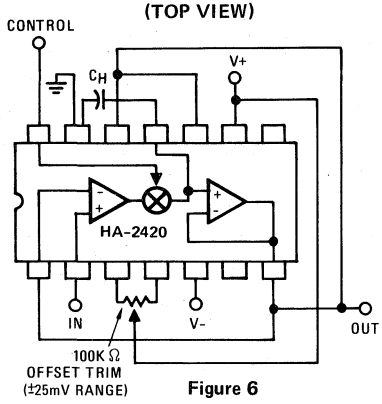


Figure 6

GUARD RING LAYOUT
(BOTTOM VIEW)

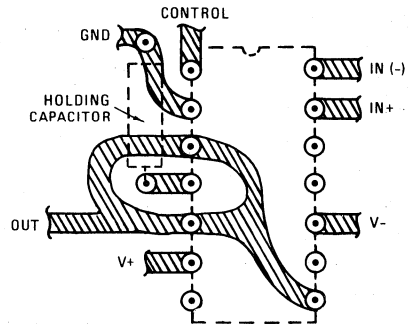


Figure 7

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.

3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D(pA) = C_H(pF) \times \frac{\Delta V}{\Delta T}(Volts/sec)$$

DIE CHARACTERISTICS

Transistor Count:		78	Tie Substrate to:	$-V_{SUPPLY}$
Die Dimensions:		97 x 61 mils	Process:	Bipolar, Dielectric Isolation
Thermal Constants:	θ_{ja}	96 °C/W		
	θ_{jc}	41 °C/W		

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

FEATURES

- GAIN, dc — 2×10^6 V/V
- ACQUISITION TIME — 1.0 µs (0.01%)
- DROOP RATE — 0.08 µV/µs (25°C); 17 µV/µs (FULL TEMP)
- APERTURE TIME — 25ns
- HOLD STEP ERROR (SEE GLOSSARY) — 1.0 mV
- INTERNAL HOLD CAPACITOR
- FULLY DIFFERENTIAL INPUT
- TTL COMPATIBLE

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

DESCRIPTION

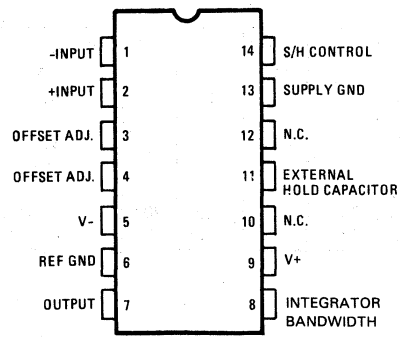
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

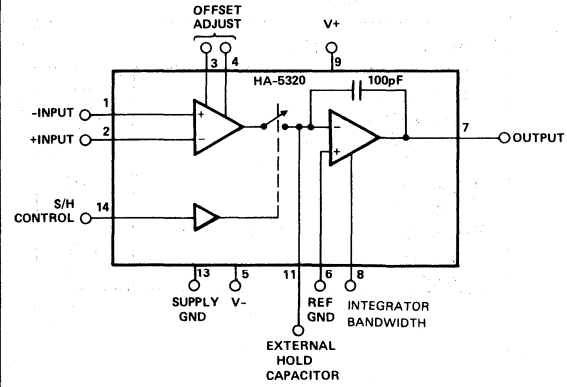
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 requires ±15V, and is available in a ceramic or plastic 14-pin DIP. For further information, please see Application Note number 538.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V^+ and V^- terminals	40V	Internal Power Dissipation	450mW
Differential Input Voltage	±24V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, −15V	HA-5320-2/8	$-55^oC \leq TA \leq +125^oC$
Output Current, continuous	±20mA (Note 2)	HA-5320-5	$0^oC \leq TA \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq TA \leq +150^oC$

ELECTRICAL CHARACTERISTICS Test Conditions (unless otherwise specified)

V Supply = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (sample), V_{AH} = +2.0V (hold).

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2			0.5		mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 3)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	$2x10^6$		$3x10^5$	$2x10^6$		V/V
Gain Bandwidth Product (A_V = +1)	25°C							
(Note 5) CH = 100pF			2.0			2.0		MHz
CH = 1000pF			.18			.18		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 4)	25°C		600			600		KHz
Output Resistance (Hold mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10 MHz								
Sample	25°C		125	200		125	200	µV RMS
Hold	25°C		125	200		125	200	µV RMS

SPECIFICATIONS (continued)

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		nS
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 6)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0			2.0			V
Input Voltage (Low), V_{IL}	Full			0.8			0.8	V
Input Current (V_{IL} = 0V)	Full			4			4	µA
Input Current (V_{IH} = +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (.1%) (Note 7)	25°C		0.8	1.2		0.8	1.2	µS
Acquisition Time (.01%) (Note 7)	25°C		1.0	1.5		1.0	1.5	µS
Aperture Time (Note 8)	25°C		25			25		ns
Effective Aperture Delay Time (See Glossary)	25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	25°C		0.3			0.3		ns
Droop Rate	25°C		0.08	0.5		0.08	0.5	µV/us
Droop Rate	Full		17	100		1.2	100	µV/us
Drift Current (Note 9)	25°C		8	50		8	50	pA
Drift Current (Note 9)	Full		1.7	10		0.12	10	nA
Charge Transfer (Note 9)	25°C		0.1	0.5		0.1	0.5	pC
Hold Mode Settling Time (.01%)	Full		165	250		165	250	ns
Hold Mode Feedthrough ($10V_{p-p}$, 100kHz)	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Voltage	Full	+14.5	+15	+16	+14.5	+15	+16	V
Negative Supply Voltage	Full	−14.5	−15	−16	-14.5	−15	−16	V
Positive Supply Current (Note 10)	25°C		11	13		11	13	mA
Negative Supply Current (Note 10)	25°C		−11	−13		−11	−13	mA
Power Supply Rejection V^+	Full	80			80			dB
(Note 11) V^-	Full	65			65			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below +20mA.
3. $V_{CM} = \pm 5V$ DC
4. $V_O = 20V_{p-p}$; $R_L = 2K\Omega$; $C_L = 50pF$; unattenuated output.
5. $V_O = 200mV_{p-p}$; $R_L = 2K\Omega$; $C_L = 50pF$.
6. V_O = 20V Step; $R_L = 2K\Omega$; $C_L = 50pF$.
7. V_O = 10V Step; $R_L = 2K\Omega$; $C_L = 50pF$.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{AH} = +3.5V, $t_r < 20ns$ (V_{IL} to V_{IH})
10. Specified for a zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ± 28mA at 20V.
11. Based on a one volt delta in each supply, ie. 15V ± 0.5V DC.

APPLYING THE HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas. (Note, however, these apply to a different Sample/Hold amplifier. The HA-5320 is not necessarily plug-in compatible.)

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Power Gnd terminal on pin 13.

The ideal ground connections are pin 6 (Reference Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100 pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characteristics section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value $0.1C_H$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon ® * and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

APPLICATIONS

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier – its most widely used configuration. As an input device for a fast successive – approximation A/D converter, it offers the highest throughput rate available from a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12 bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, $0.1C_H$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

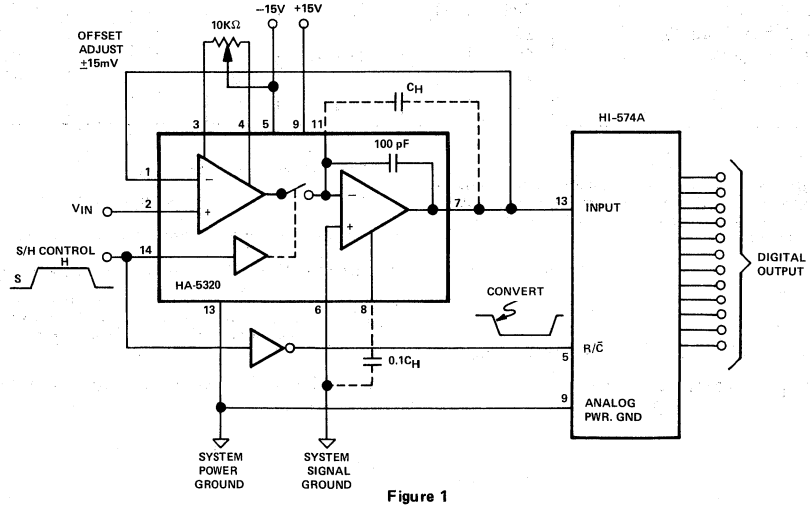


Figure 1

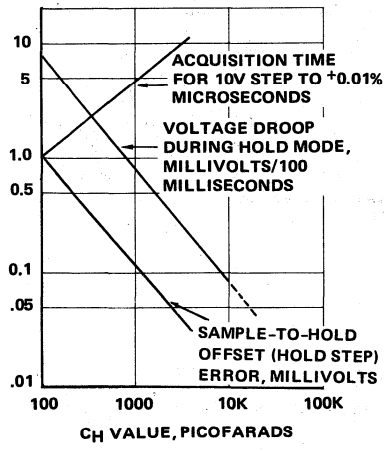
TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE.

* Teflon is a registered trademark of Dupont Corporation.

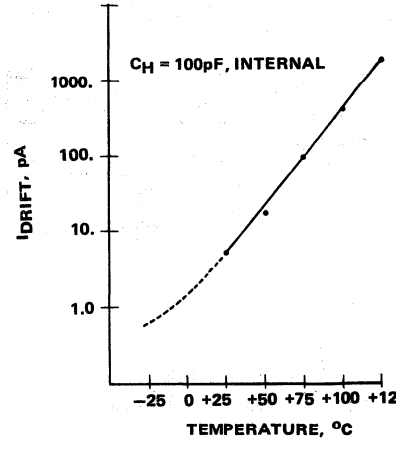
PERFORMANCE CURVES

V_{SUPPLY} = ±15VDC

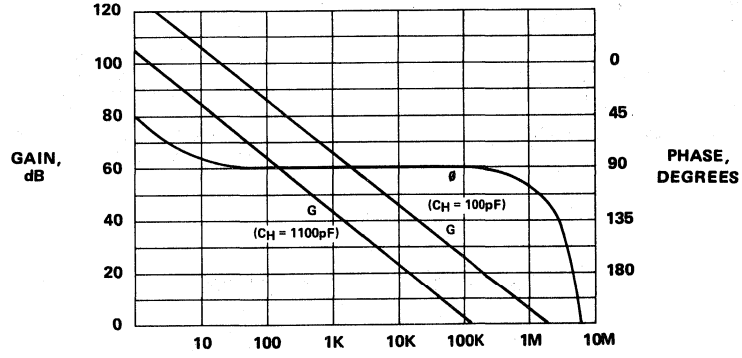
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT VS. TEMPERATURE

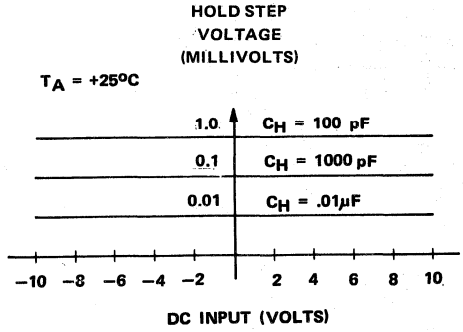


OPEN LOOP GAIN AND PHASE RESPONSE

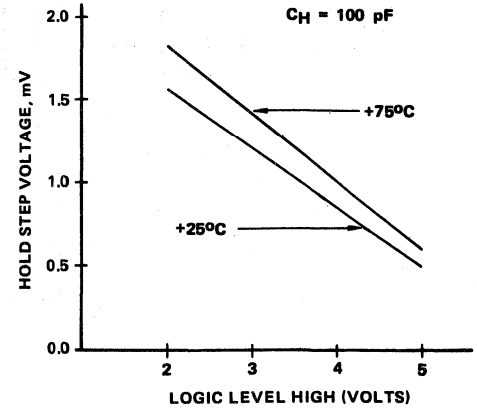


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

HOLD STEP vs. INPUT VOLTAGE

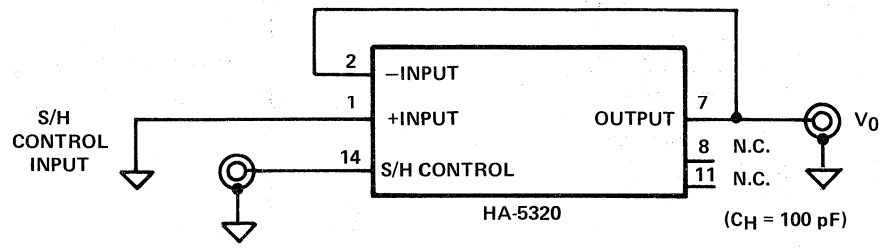


HOLD STEP vs. LOGIC (V_{AH}) VOLTAGE



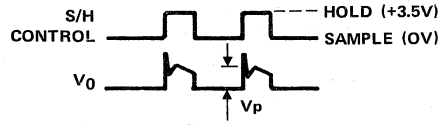
7 S/H AMPS & SIG. PROCESSORS

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

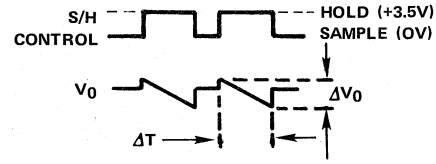
1. Observe the "hold step" voltage V_p:



2. Compute charge transfer: $Q = V_p C_H$

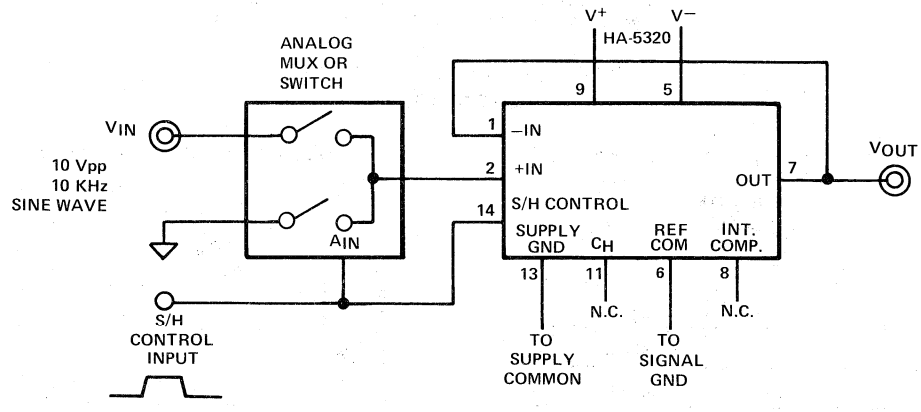
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O / \Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O / \Delta T$, and compute drift current: $I_D = C_H \Delta V_O / \Delta t$.

HOLD MODE FEEDTHROUGH ATTENUATION



Feedthrough in dB = 20 log $\frac{V_{OUT}}{V_{IN}}$ where

V_{OUT} = Volts pp, Hold mode ,

V_{IN} = Volts pp.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

HOLD STEP ERROR:

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{(Volts/sec)}$$

DIE CHARACTERISTICS

Transistor Count:		175
Die Dimensions:		90.2 x 143.7 mils
Thermal Constants:	θ_{ja}	75°C/W
	θ_{jc}	17°C/W
Tie Substrate to		$-V_{Supply}$
Process:		Bipolar Dielectric Isolation

HARRIS

ADVANCE

HA-5330

Very High Speed Precision Monolithic Sample and Hold Amplifier

FEATURES

- ACQUISITION TIME 400ns (0.01%)
- DROOP RATE 0.1μV/μs (25°C)
  10μV/μs (+125°C)
- APERTURE TIME 25ns
- HOLD STEP ERROR 0.6mV (ADJ. TO ZERO)
- HIGH ACCURACY ≥12 BITS
- INTERNAL HOLD CAPACITOR
- FULLY DIFFERENTIAL INPUT
- TTL COMPATIBLE
- LOW OFFSET VOLTAGE T.C.

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

DESCRIPTION

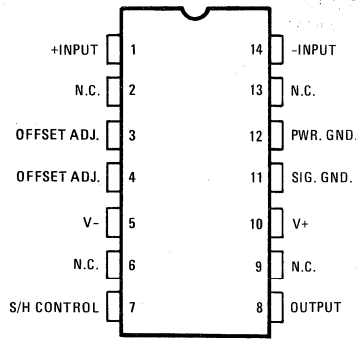
The HA-5330 was designed for use with high speed A/D converters. It offers a 400ns acquisition time (to ±1/2 LSB, 12 bits) and supports system accuracy requirements to 12 bits and above. The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits, and if necessary, the resulting 0.6mV hold step error may be adjusted to zero via the Offset Adjust terminals. Also, compensation is used to minimize Drift Current, which causes voltage droop in the Hold mode. The chip includes a 90pF hold capacitor.

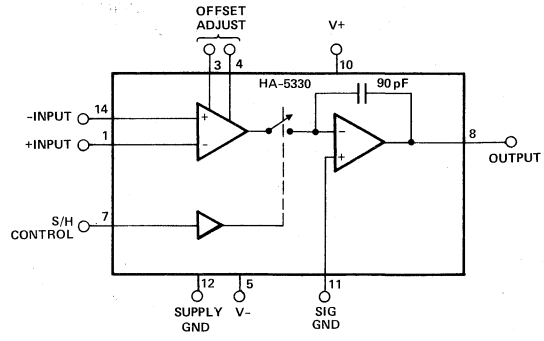
This monolithic device is manufactured using the Harris Dielectric Isolation process, minimizing stray capacitance and eliminating SCRs. This allows higher speed and latch-free operation. The HA-5330 requires ± 15V, and is available in a ceramic or plastic 14-pin DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS

HI-5900

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- 50kHz THROUGHPUT
- 12-BIT ACCURACY
- OUTPUT TRACK/HOLD AMPLIFIER
- ZERO OFFSET ADJUSTMENT
- DIFFERENTIAL INPUT CHANNELS
- SOFTWARE CONTROLLED GAIN AND CHANNEL SELECT
- 85dB CMRR
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION
- MILITARY SYSTEMS

DESCRIPTION

The HI-5900 comprises "front end" components of a data acquisition system including an eight channel differential multiplexer, programmable gain instrumentation amplifier (PGA), and Track and Hold amplifier. Adding a timing circuit and one A to D converter yields a complete data acquisition system. A 50kHz channel-to-channel throughput rate is achieved when the HI-5900 is used with a fast 12 bit A to D converter such as HARRIS HI-5712.

Each output line of the input multiplexer is buffered by a high-quality non-inverting amplifier. This isolates each line from source resistances external to the 5900, preserving the high CMRR of the instrumentation amplifier block. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, a monolithic resistor network and a four channel differential multiplexer, offers precision inverting gain values of -1, -2, -4, and -8. The voltage gain is selected by a two bit digital word. The output of the PGA drives the Track and Hold amplifier, and the ground side of the PGA is isolated by a buffer amplifier to maintain a high CMRR.

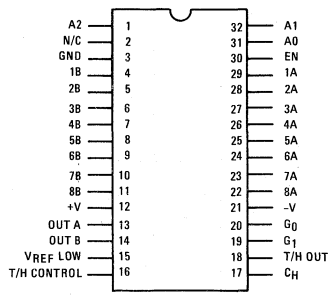
The output Track/Hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the sample mode it operates as a high performance buffer amplifier. With an external holding capacitor, it may be swiched to HOLD with an effective aperture delay time of 30ns.

The packaging technique involves monolithic chips mounted in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. The HI-5900 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. The resulting package is a compact 32 pin DIP.

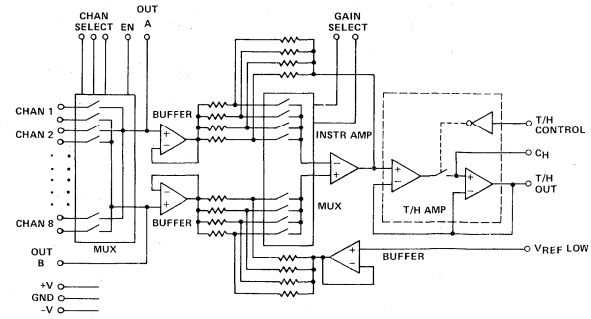
The HI-5900 is offered as a high performance front-end section for military and industrial data acquisition systems. It is designed for interface with computers and is well suited for high-rel applications. For further information see Application Notes numbered 527, 529, and 530.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V

Digital Input Overvoltage (Multiplexers)

V_{Supply} (+) +4V

V_{Supply} (-) -4V

Analog Input Overvoltage

V_{Supply} (+) +20V

V_{Supply} (-) -20V

Output Current: Short Circuit Protected

Operating Temperature Range

HA-5900-5: $0^oC \leq T_A \leq +75^oC$

HA-5900-2: $-55^oC \leq T_A \leq +125^oC$

Storage Temperature Range: $-65^oC \leq T_A \leq +150^oC$

Internal Power Dissipation: 650mW

T/H Control Input: +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

		HI-5900-2 -55°C to +125°C			HI-5900-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7		3	10	mV
	Full			9			12	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
VAL, Input Low Threshold				0.8			0.8	
VAH, Input High Threshold		4.0			4.0			
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Inverting Gain of -1, -2,	Full		0.01	0.1		0.01	0.2	%
Inverting Gain of -4, -8	Full		0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Effective Aperture Delay Time (T/H)	+25°C		30			30		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	76	100		70	100		dB

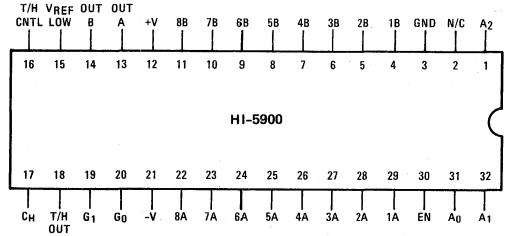
NOTES:
1. Absolute maximum ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = -1.

PIN FUNCTIONS AND DESCRIPTION

PIN	SYMBOL	DESCRIPTION
4 5 6 7 8 9 10 11	1B 2B 3B 4B 5B 6B 7B 8B	Non-Inverting Side of the Eight Differential Input Channels
29 28 26 25 24 23 22	1A 2A 4A 5A 6A 7A 8A	Inverting Side of the Eight Differential Input Channels
31 32 1	A_0 A_1 A_2	Digital Channel Select Inputs*
20 19	G_0 G_1	Digital Gain Select Inputs*

PIN	SYMBOL	DESCRIPTION
16	T/H CONTROL	Track/Hold Mode Select*
2	NC	No Connection
3	GND	Signal and Power Ground
12	+V	Positive Supply (+15V)
21	-V	Negative Supply (-15V)
18	T/H OUT	Output of the HI-5900
17	C_H	Hold Capacitor Connection
15	V_{REF} LOW	Reference for the Output on Pin 18
13	OUT A	"A" Output of the Input Multiplexer (Inverting Side of each Channel)
14	OUT B	"B" Output of the Input Multiplexer (Non-Inverting Side of each Channel)
30	EN	Enable Strobe for the Input Multiplexer; Normally Forced High. EN may be used in Conjunction with OUT A and OUT B, to Poll Additional Channels through an External Multiplexer.

* See Programmable Functions



PROGRAMMABLE FUNCTIONS

Input Codes are as follows:

X = DON'T CARE
0 = $V_{IN} \leq +0.8V$;
1 = $V_{IN} \geq +4.0V$, where V_{IN} is the digital input voltage.

1. T/H Control (PIN 16)

0	Track
1	Hold

2. Gain Select

G_1 (PIN 19)	G_0 (PIN 20)	GAIN
0	0	−1
0	1	−2
1	0	−4
1	1	−8

3. Channel Select

A_2 (PIN 1)	A_1 (PIN 32)	A_0 (PIN 31)	EN (PIN 30)	CHANNEL
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

PERFORMANCE CURVES

ACQUISITION TIME vs. OUTPUT STEP CHANGE

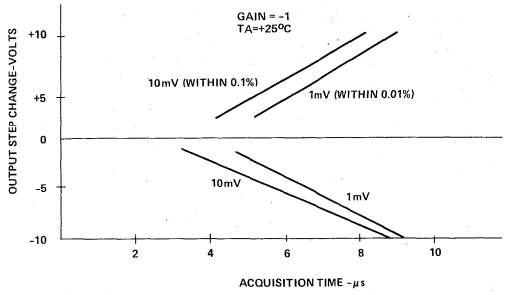


FIGURE 1

INPUT NOISE VOLTAGE vs. FREQUENCY

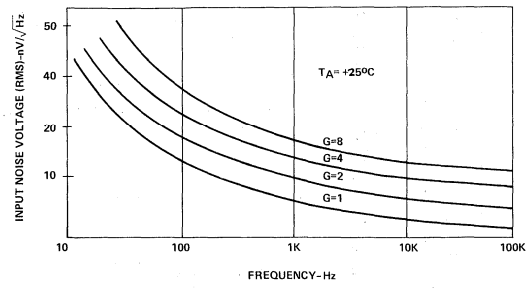


FIGURE 2

TYPICAL T/H AMPLIFIER PERFORMANCE vs. HOLD CAPACITANCE Ch

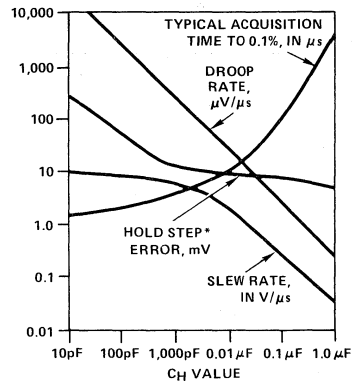


FIGURE 3

*Hold step voltage is the output error following a switch from sample to hold.

INPUT LEAKAGE, BIAS & OFFSET CURRENT vs. TEMPERATURE

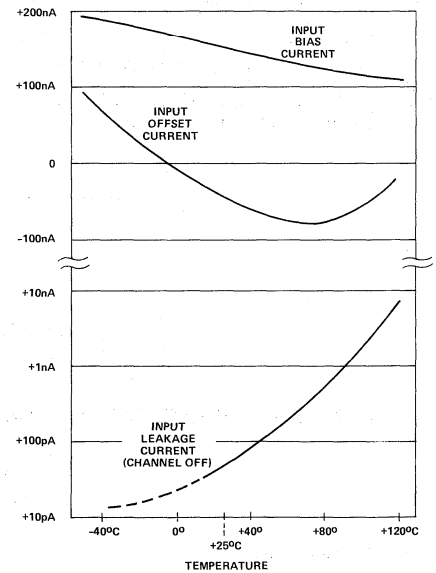


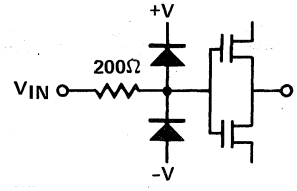
FIGURE 4

APPLYING THE HI-5900

GENERAL CONSIDERATIONS

The HI-5900 was designed to provide a versatile front-end section for a data acquisition system. Both hardwired and computer-controlled systems may be implemented in a variety of configurations. The following general considerations and precautions should be observed.

1. HANDLING – Each digital input is protected by a resistor-diode network, to minimize failures due to static discharge through the MOS gate:



For additional protection, it is wise to observe all of the proper shipping and handling procedures customary for CMOS devices.

2. POWER SUPPLY CONNECTIONS – Each of the four active chips in the HI-5900 are bypassed to ground by internal .01 μF capacitors. These eight nonpolarized capacitors prevent high frequency variations in the supply voltage.

   To bypass lower frequencies, connect a polarized capacitor from the ground pin to each supply pin, with value from 10μF to 50μF.

3. LAYOUT

   A. Distributed capacitance between signal paths external to the HI-5900 is a major source of crosstalk. Within the HI-5900, careful substrate design and packaging have ensured that "static" crosstalk will not exceed -80dB. ("Static") refers to the absence of channel-to-channel switching. Thus, a maximum of 2mV p-p can feed into a selected channel, from 20V p-p applied to one or more OFF channels.)

   When a multiplexer is continuously cycled from channel to channel, two other forms of crosstalk arise. These are dynamic crosstalk and adjacent* channel crosstalk, which are both minimized along with static crosstalk by careful attention to circuit board layout. A strip of ground plane should separate conductors for adjacent channels on a printed circuit board. See Fig. 5. Make these traces (and the conductors) short, and as narrow as practical for maximum separation.

   *Adjacent in time – for example, channels 1 and 8 may occupy adjacent time slots during time – division multiplexing.

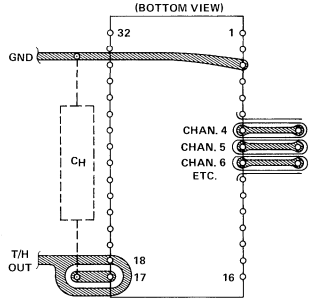


FIGURE 5
HI-5900 GUARD RING LAYOUT

B. The holding capacitor C_H is the only essential external component required for operation of the HI-5900. The value selected determines droop rate, offset error and acquisition time according to curves shown in Fig. 3. Board layout should include a guard ring to prevent voltage-driven leakage at the capacitor terminal. See Fig. 5.

   For minimum droop error in the HOLD mode, choose a capacitor with high insulation resistance and low dielectric absorption. Since type of dielectric is the best performance indicator for hold capacitor applications, consider these guidelines: Teflon is best (especially at high temperature) but the most expensive. In descending order of choice, polystyrene, polypropylene, and polycarbonate are all acceptable. Least acceptable are ceramic and mica, which can allow several percent of change in the held voltage due to dielectric absorption (vs. .01% for the other types).

OFFSET ADJUSTMENT

The V_{REF} LOW input (pin 15) is a convenient point for nulling any DC offset voltage in an HI-5900 system. This can be done with a simple manual trim:

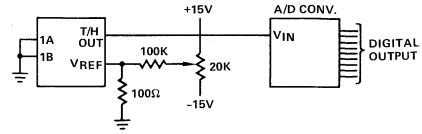


FIGURE 6

With zero volts on the selected input channel, the HI-5900 output (T/H OUT) may be adjusted to zero. If the system includes an A to D converter, net DC offset may be nulled by adjusting the converter's digital output to zero. In either case, readjustment is required after a change in temperature or a change in the HI-5900 gain. The need for readjustment may be eliminated by using an auto-zero circuit as shown in Fig. 7.

The offset at V_O is driven to zero by application of a voltage at V_{REF} LOW, opposite in sign and with magnitude (G + 1) V_O, where G is the digitally selected gain. This voltage is updated each time channel 8 is addressed. Since channel 8 is chosen for the zero (ground) reference input, the SN7420 decoder output is wired to go low only when channel 8 is addressed. The HA-2420 track/hold amplifier acquires a new sample of the offset at V_O during this interval. This sample is of opposite sign to V_O and approximately 100X V_O in magnitude, due to the 10K/100Ω attenuator. Storing 100X the actual correction value minimizes the percent droop error during hold. Finally, OFFSET TRIM is used to remove any residual offset at V_O, introduced by the HA-2420.

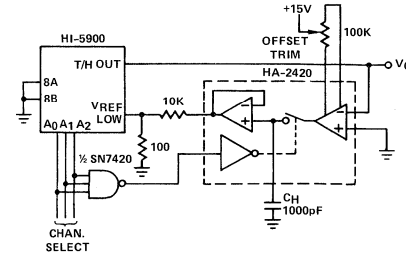


FIGURE 7

TIMING AND CONTROL

The HI-5900 is intended to operate with a fast A to D converter such as the Harris 12 bit HI-5712. A single monostable (one-shot) multivibrator such as half of the dual SN74123 provides the necessary timing and control.

The pulse rate at $\overline{Q}$ is equal to the conversion rate of the A to D converter, since the one-shot is driven by the converter's STATUS output. Polarity of the Q output is correct for initiating a conversion each time the HI-5900 returns to the HOLD mode. For maximum channel-to-channel throughput rate, the $\overline{Q}$ pulse duration (determined by R and C) may be set equal to the HI-5900 acquisition time.

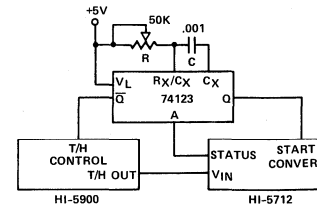


FIGURE 8

HARRIS

HI-5901

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- SOFTWARE CONTROLLED GAIN AND INPUT CHANNEL SELECTION
- 16 PSEUDO-DIFFERENTIAL/SINGLE ENDED INPUT CHANNELS
- INVERTING GAINS OF -1, -2, -4 AND -8
- -90dB CROSSTALK
- 0.01% GAIN ERROR
- 9μs ACQUISITION TIME
- DROOP RATE: 5nV/μsec
- LOW POWER DISSIPATION 250mW
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

The HI-5901 is a data acquisition front end subsystem intended for multisensor based high-level applications, requiring conversion of analog input data to digital form for computer processing. It provides sixteen single-ended or pseudo differential channels of fault-protected multiplexed inputs, programmable gains of -1, -2, -4, -8 and a buffered track and hold output block compatible with any commercially available A/D converter. All these functions are digitally selectable through appropriate coding of seven control terminals. Input channel expansion can be easily implemented through addition of external multiplexers and proper utilization of the enable-command pin.

Being self-contained units except for the holding capacitor, they facilitate user applications and eliminate the need for selection of high-priced precision resistors or labor intensive adjustments to achieve the accuracy levels specified.

This product provides channel to channel throughput rates of 50kHz at $\pm$10 volt signal range when used in connection with a fast 12 bit A/D converter such as the HI-5712. In addition, it offers excellent input characteristics such as low input offset voltage with offset nulling capability, low input currents, very high input impedance, and very low crosstalk. Typical acquisition time and gain error are 9 microseconds and $\pm$0.01%, respectively. The internal track and hold amplifier features an effective aperture delay time of 30ns and a droop rate of 5nV/μsec. Total power dissipation is only 250mW.

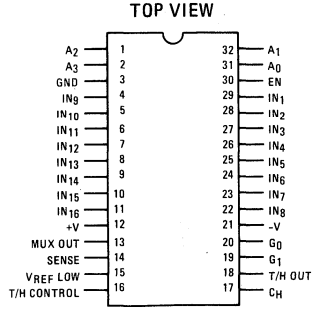
A complete high-speed and high precision data acquisition system with 15 bits of dynamic range can be easily implemented with only three components: the HI-5901, the HI-5712, and an offset nulling DAC. Board space required is 3 sqare inches and total weitht is less than 25 grams.

The manufacturing technique adopted for the HI-5901 involves monolithic dice packaged in leadless chip carriers (LCCs) and soldered to both sides of a multilayer ceramic substrate. The resulting product is a compact and easy-to-use 32 pin DIP.

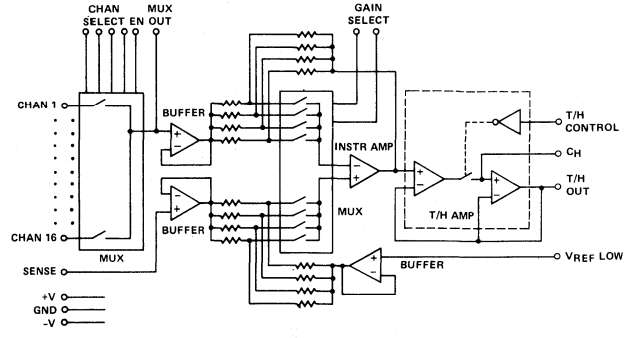
The HI-5901 is intended for military, aerospace, industrial and instrumentation applications. High reliability, military and commercial grades are both available as standard products. For further information see Application Notes 527, 529 and 530.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V

Digital Input Overvoltage (Multiplexers)

V_{Supply} (+) +4V

V_{Supply} (-) -4V

Analog Input Overvoltage

V_{Supply} (+) +20V

V_{Supply} (-) -20V

Output Current Short Circuit Protected

Operating Temperature Range

HA-5901-5, -7 $0^oC \leq T_A \leq +75^oC$

HA-5901-2, -8 $-55^oC \leq T_A \leq +125^oC$

Storage Temperature Range $-65^oC \leq T_A \leq +150^oC$

Internal Power Dissipation 650mW

T/H Control Input +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

		HI-5901-2, -8 -55°C to +125°C			HI-5901-5, -7 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7.5		3	10.5	mV
	Full			9.5			13	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
VAL, Input Low Threshold				0.8			0.8	
VAH, Input High Threshold		4.0			4.0			
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Inverting Gain of -1, -2,	Full		0.01	0.1		0.01	0.2	%
Inverting Gain of -4, -8	Full		0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Effective Aperture Delay Time (T/H)	+25°C		30			30		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	76	100		70	100		dB

NOTES: 1. Absolute maximum ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

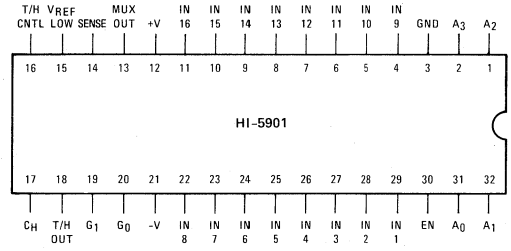
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = -1.

PIN FUNCTIONS AND DESCRIPTION

PIN	SYMBOL	DESCRIPTION
4	IN_9	16 Single Ended Input Channels. The Signals Applied to these Input Channels are Inverted at the Output of HI-5901
5	IN_{10}	
6	IN_{11}	
7	IN_{12}	
8	IN_{13}	
9	IN_{14}	
10	IN_{15}	
11	IN_{16}	
29	IN_1	
28	IN_2	
27	IN_3	
26	IN_4	
25	IN_5	
24	IN_6	
23	IN_7	
22	IN_8	
31	A_0	Digital Channel Select Inputs*
32	A_1	
1	A_2	
2	A_3	

PIN	SYMBOL	DESCRIPTION
20	G_0	Digital Gain Select Inputs*
19	G_1	
16	T/H CONTROL	Track/Hold Mode Select*
3	GND	Signal and Power Ground
12	+V	Positive Supply (+15V)
21	-V	Negative Supply (-15V)
18	T/H OUT	Output of the HI-5901
17	C_H	Hold Capacitor Connection
15	$V_{REF}LOW$	Reference for the Output on Pin 18
13	MUX OUT	Input Multiplexer Output
14	SENSE	Analog Signal Return
30	EN	Enable Strobe for the Input Multiplexer; Normally Forced High. EN may be used in Conjunction with MUX OUT and SENSE, to Poll Additional Channels through an External Multiplexer

*See Programmable Functions



PROGRAMMABLE FUNCTIONS

Input Codes are as follows:

X = DON'T CARE
0 = $V_{IN} \leq +0.8V$
1 = $V_{IN} \geq +4.0V$, where V_{IN} is the digital input voltage

1. T/H CONTROL (Pin 16)

0	TRACK
1	HOLD

2. GAIN SELECT

G_1 (Pin 19)	G_0 (Pin 20)	GAIN
0	0	−1
0	1	−2
1	0	−4
1	1	−8

3. CHANNEL SELECT

A_3 (Pin 2)	A_2 (Pin 1)	A_1 (Pin 32)	A_0 (Pin 31)	EN (Pin 30)	CHANNEL
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

PERFORMANCE CURVES

ACQUISITION TIME vs. OUTPUT STEP CHANGE

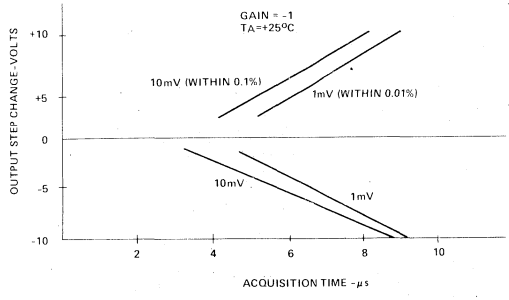


FIGURE 1

INPUT NOISE VOLTAGE vs. FREQUENCY

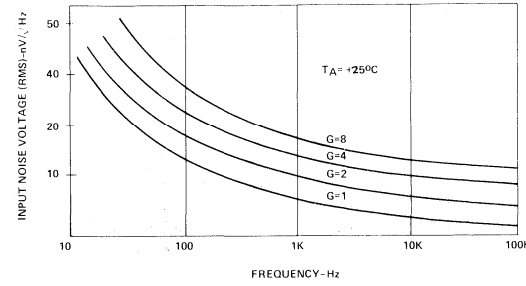


FIGURE 2

TYPICAL T/H AMPLIFIER PERFORMANCE vs. HOLD CAPACITANCE Ch

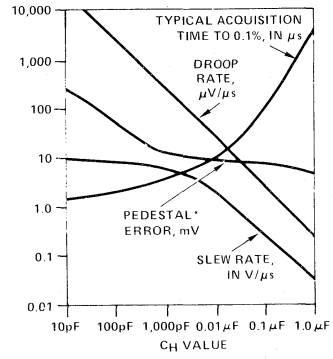


FIGURE 3

INPUT LEAKAGE, BIAS & OFFSET CURRENT vs. TEMPERATURE

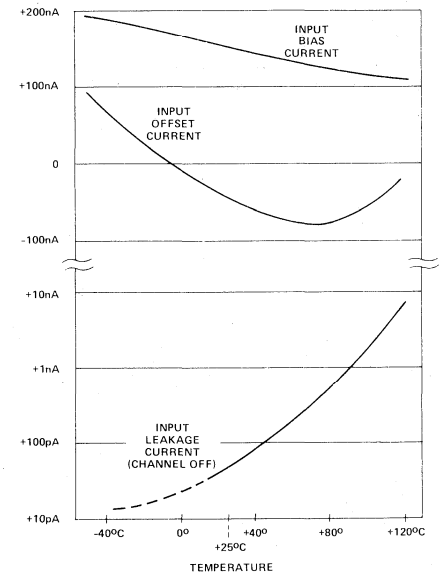


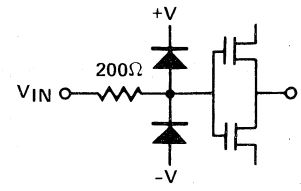
FIGURE 4

APPLYING THE HI-5901

GENERAL CONSIDERATIONS

The HI-5901 was designed to provide a versatile front-end section for a data acquisition system. Both hardwired and computer-controlled systems may be implemented in a variety of configurations. The following general considerations and precautions should be observed.

1. HANDLING – Each digital input is protected by a resistor-diode network, to minimize failures due to static discharge through the MOS gate:



For additional protection, it is wise to observe all of the proper shipping and handling procedures customary for CMOS devices.

2. POWER SUPPLY CONNECTIONS – Each of the four active chips in the HI-5901 are bypassed to ground by internal .01 μF capacitors. These eight nonpolarized capacitors prevent high frequency variations in the supply voltage.

   To bypass lower frequencies, connect a polarized capacitor from the ground pin to each supply pin, with value from 10μF to 50μF.

3. LAYOUT

   A. Distributed capacitance between signal paths external to the HI-5901 is a major source of crosstalk. Within the HI-5901, careful substrate design and packaging have ensured that "static" crosstalk will not exceed -80dB. ("Static") refers to the absence of channel-to-channel switching. Thus, a maximum of 2mV p-p can feed into a selected channel, from 20V p-p applied to one or more OFF channels.)

   When a multiplexer is continuously cycled from channel to channel, two other forms of crosstalk arise. These are dynamic crosstalk and adjacent* channel crosstalk, which are both minimized along with static crosstalk by careful attention to circuit board layout. A strip of ground plane should separate conductors for adjacent channels on a printed circuit board. See Fig. 5. Make these traces (and the conductors) short, and as narrow as practical for maximum separation.

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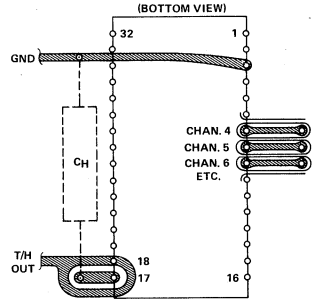

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   For minimum droop error in the HOLD mode, choose a capacitor with high insulation resistance and low dielectric absorption. Since type of dielectric is the best performance indicator for hold capacitor applications, consider these guidelines: Teflon is best (especially at high temperature) but the most expensive. In descending order of choice, polystyrene, polypropylene, and polycarbonate are all acceptable. Least acceptable are ceramic and mica, which can allow several percent of change in the held voltage due to dielectric absorption (vs. .01% for the other types).

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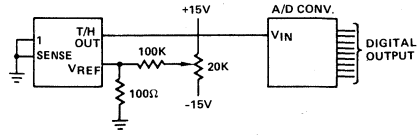

FIGURE 6

With zero volts on the selected input channel, the HI-5901 output (T/H OUT) may be adjusted to zero. If the system includes an A to D converter, net DC offset may be nulled by adjusting the converter's digital output to zero. In either case, readjustment is required after a change in temperature or a change in the HI-5901 gain. The need for readjustment may be eliminated by using an auto-zero circuit as shown in Fig. 7.

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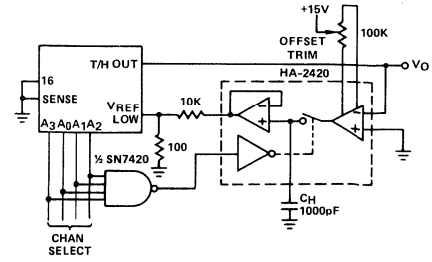

FIGURE 7

TIMING AND CONTROL

The HI-5901 is intended to operate with a fast A to D converter such as the Harris 12 bit HI-5712. A single monostable (one-shot) multivibrator such as half of the dual SN74123 provides the necessary timing and control:

The pulse rate at $\overline{Q}$ is equal to the conversion rate of the A to D converter, since the one-shot is driven by the converter's STATUS output. Polarity of the Q output is correct for initiating a conversion each time the HI-5901 returns to the HOLD mode. For maximum channel-to-channel throughput rate, the $\overline{Q}$ pulse duration (determined by R and C) may be set equal to the HI-5901 acquisition time.

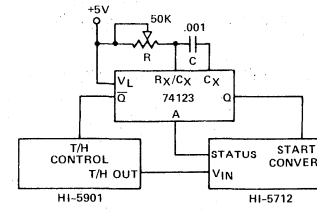

FIGURE 8

ANALOG

Communications

8

Product Index 8-2

Product Information 8-3

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Communication Product Index

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HARRIS

HC-5502

SLIC-LC Subscriber Line Interface Circuit

Not Recommended For New Designs See HC-5502A

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltages.

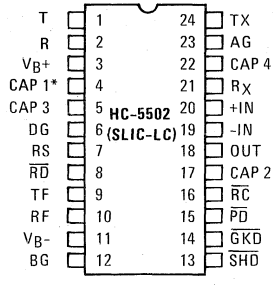
The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC-LC is ideally suited in the design of new digital PABX systems, by eliminating bulky, expensive hybrid transformers.

SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC-LC is also available as unpackaged die.

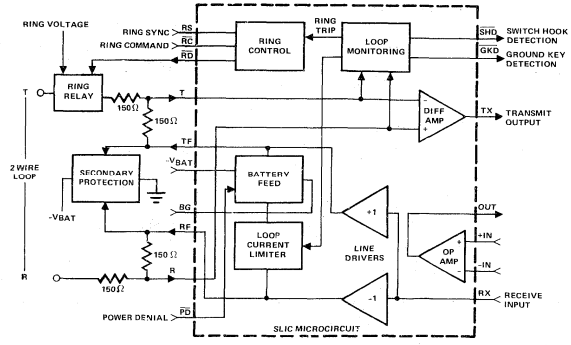
PINOUT

TOP VIEW



*Optional

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages	(V_B-)	-60 to +.5 Volts
	(V_B+)	-.5 to +15 Volts
	(V_B+ - V_B-)	75 Volts
Operating Ambient Temperaure Range	(T_A)	0°C to +75°C
Storage Temperature Range (R_{SRG})		-40°C to +85°C
Thermal Resistnace (θ_{J-A}) (Plastic)		52°C/W
Thermal Resistance (θ_{J-A}) (Ceramic)		55°C/W

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (V_B+)	10.8 to 13.2 Volts
Negative Supply Voltage (V_B-)	-42 to -58 Volts
Minimum High Level Logic Input Voltage	2.4 Volts
Maximum Low Level Logic Input Voltage	0.8 Volts
Loop Resistance (R_L)	200 to 1200 Ohms
Ambient Operating Temperature Range (T_A)	0°C to +70°C

ELECTRICAL CHARACTERISTICS

(V_B- = -48V, V_B+ = +12V, AG = BG = DG = 0V, T_A = 25°C Unless Otherwise Stated)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{Long} = 0		110	180	mW
Off Hook Power Dissipation	R_{LOOP} = 600 Ohms, I_{Long} = 0		743	795	mW
Off Hook IB+	R_{LOOP} = 600 Ohms, I_{Long} = 0			4.2	mA
Off Hook IB-	R_{LOOP} = 600 Ohms, I_{Long} = 0			38	mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, I_{Long} = 0		21		mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, V_B- = -42V, I_{Long} = 0	17.5			mA
Off Hook Loop Current	R_{LOOP} = 200 Ohms, I_{Long} = 0	24	27	30	mA
Fault Currents					
TIP to Ground			14		mA
RING to Ground			54		mA
TIP to RING			27		mA
TIP and RING to Ground			85		mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA		0.3	0.9	V
Ring Trip Detection Period	R_{LOOP} = 600 Ohms		2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = VOL	10			mA
	$\overline{SHD}$ = VOH			5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = VOL	20			mA
	$\overline{GKD}$ = VOH			10	mA
Dial Pulse Distortion		0		5	ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz				
2 Wire Off Hook		58	65		dB
2 Wire On Hook		60	63		dB
4 Wire Off Hook		50	58		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@ 1kHz, 0dBm Input Level				
2 Wire – 4 Wire			±.05	±0.2	dB
4 Wire – 2 Wire			±.05	±0.2	dB
Frequency Response	200 – 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02	±0.05	dB
Idle Channel Noise					
2 Wire – 4 Wire				10	dBrnC
4 Wire – 2 Wire				10	dBrnC
Absolute Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Envelope Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40		dB
Overload Level					
2 Wire – 4 Wire		+4			dBm
4 Wire – 2 Wire		+4			dBm
Level Linearity	at 1kHz				
2 Wire – 4 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
4 Wire – 2 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
Power Supply Rejection Ratio					
V_{B+} to 2 Wire	30 – 60Hz, R_{LOOP} = 600Ω	15			dB
V_{B+} to Transmit		15			dB
V_{B-} to 2 Wire		15			dB
V_{B-} to Transmit		15			dB
V_{B+} to 2 Wire	200 – 16kHz	30			dB
V_{B+} to Transmit	R_{LOOP} = 600Ω	30			dB
V_{B-} to 2 Wire		30			dB
V_{B-} to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}				0.8	Volts
Logic '1' V_{IH}		2.4		5.5	Volts
Logic Outputs	Max Two LS Loads				
Logic '0' V_{OL}			0.1	0.5	Volts
Logic '1' V_{OH}		3.0	6.1	6.3	Volts

OVERVOLTAGE PROTECTION AND LONGITUDINAL CURRENT REJECTION

The SLIC-LC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC-LC will withstand longitudinal currents up to a maximum of 30mA rms, 15mA rms per leg, without any performance degradation.

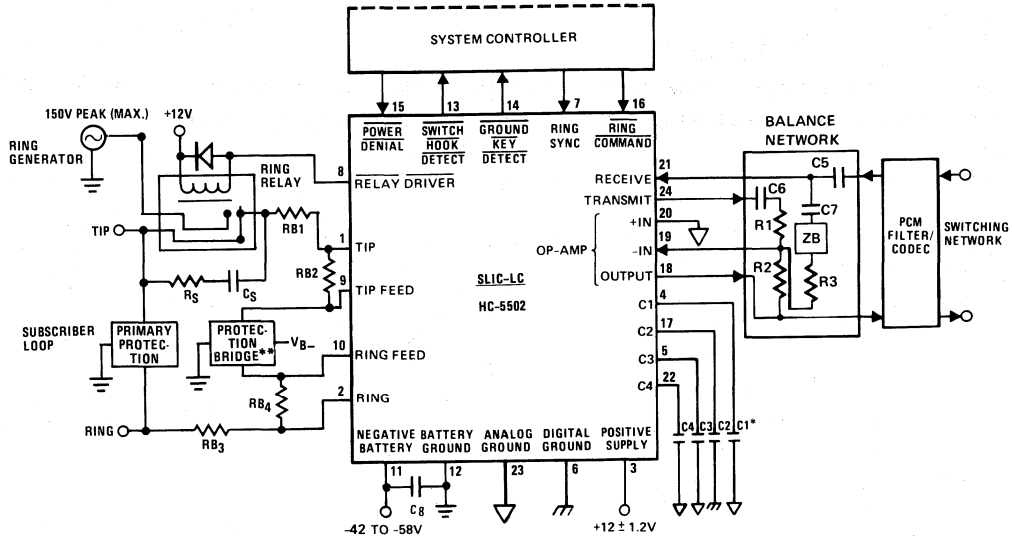
TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MIN)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	T	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the R terminal (Pin 2) to receive voice signals from the telephone and for Loop Monitoring Purposes.
2	R	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the T terminal (Pin1) to receive voice signals from the telephone and for loop monitoring purposes.
3	V_B+	Positive Voltage Source – Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
4	CAP 1	Capacitor #1 – Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
5	CAP 3	Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering -48V supply. Typical value is 0.3μF, 30V.
6	DG	Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
7	RS	Ring Synchronization Input – A TTL-compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
8	$\overline{RD}$	Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized. Maximum $\overline{RD}$ voltage is 15 volts.
9	TF	Tip Feed- A low impedance analog output connected to the T terminal (Pin 1) through a 150Ω feed resistor. Functions with the RF terminal (Pin 10) to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	RF	Ring Feed - A low impedance analog output connected to the R terminal (Pin 2) through a 150Ω feed resistor. Functions with the TF terminal (Pin 9) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	V_B-	Negative Voltage Source – Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
12	BG	Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection – A low active LS TTL -compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
14	$\overline{GKD}$	Ground Key Detection – A low active LS TTL-compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA , and disabled if this current difference is less than 10mA.
15	$\overline{PD}$	Power Denial – A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command – A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
17	CAP 2	Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.
18	OUT	The analog output of the spare operational amplifier.
19	-IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side – A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
22	CAP 4	Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF to 1.0μF, 20V. This capacitor should be nonpolarized.
23	AG	Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side – A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONENT VALUES

*C1 = 0.5μF
C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μF to 1.0μF, ±10%, 20V (Should be nonpolarized)
C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required) Note 2, 20V
C8 = 0.01μF, 100V

R1 → R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations Note 2
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)
R_S = 1KΩ, C_S = 0.1μF ,200V typically, depending on V_{ring} and line length.

*NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -18 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op-amp output to the PCM Filter/CODEC. A 0.5μF and 100KΩ gives a time constant of 50msec.

**NOTE 3: Secondary protection diode bridge recommended is MDA 220 or similar.

HARRIS

HC-5502A

SLIC-LC Subscriber Line Interface Circuit

Preliminary

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

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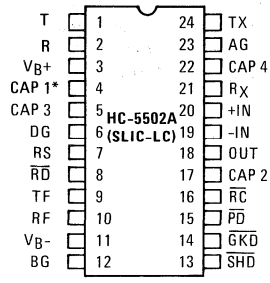
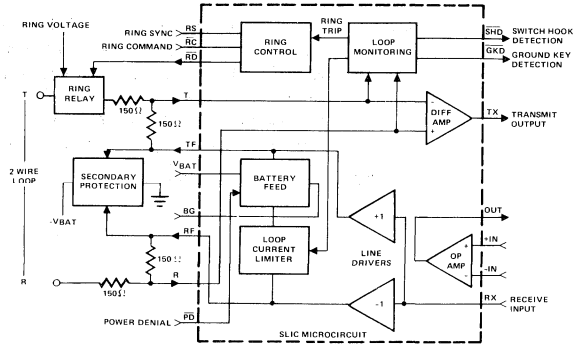
PINOUT

TOP VIEW



*Optional

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages	(V_{B-})	-60 to +.5 Volts
	(V_{B+})	-.5 to +15 Volts
	($V_{B+} - V_{B-}$)	75 Volts
Operating Ambient Temperaure Range	(T_A)	0°C to +75°C
Storage Temperature Range (R_{SRG})		-40°C to +85°C
Thermal Resistance (θ_{J-A}) (Plastic)		52°C/W
Thermal Resistance (θ_{J-A}) (Ceramic)		55°C/W

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (V_{B+})	10.8 to 13.2 Volts
Negative Supply Voltage (V_{B-})	-42 to -58 Volts
Minimum High Level Logic Input Voltage	2.4 Volts
Maximum Low Level Logic Input Voltage	0.8 Volts
Loop Resistance (R_L)	200 to 1200 Ohms
Ambient Operating Temperature Range (T_A)	0°C to +70°C

ELECTRICAL CHARACTERISTICS

(V_{B-} = -48V, V_{B+} = +12V, AG = BG = DG = 0V, T_A = 25°C Unless Otherwise Stated)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{Long} = 0		135	174	mW
Off Hook Power Dissipation	R_{LOOP} = 600 Ohms, I_{Long} = 0		743	795	mW
Off Hook IB+	R_{LOOP} = 600 Ohms, I_{Long} = 0			4.3	mA
Off Hook IB-	R_{LOOP} = 600 Ohms, I_{Long} = 0			38	mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, I_{Long} = 0		21		mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, V_{B-} = -42V, I_{Long} = 0	17.5			mA
Off Hook Loop Current	R_{LOOP} = 200 Ohms, I_{Long} = 0	25.5	30	34.5	mA
Fault Currents					
TIP to Ground			14		mA
RING to Ground			52		mA
TIP to RING			30		mA
TIP and RING to Ground			66		mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA		0.2	0.5	V
Ring Trip Detection Period	R_{LOOP} = 600 Ohms		2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = VOL	10			mA
	$\overline{SHD}$ = VOH			5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = VOL	20			mA
	$\overline{GKD}$ = VOH			10	
Dial Pulse Distortion		0		5	ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz				
2 Wire Off Hook		58	65		dB
2 Wire On Hook		60	63		dB
4 Wire Off Hook		50	58		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@ 1kHz, 0dBm Input Level				
2 Wire – 4 Wire			±.05	±0.2	dB
4 Wire – 2 Wire			±.05	±0.2	dB
Frequency Response	200 – 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02	±0.05	dB
Idle Channel Noise					
2 Wire – 4 Wire			1	5	dBrnC
4 Wire – 2 Wire			1	5	dBrnC
Absolute Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Envelope Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40		dB
Overload Level					
2 Wire – 4 Wire		+4			dBm
4 Wire – 2 Wire		+4			dBm
Level Linearity	at 1kHz				
2 Wire – 4 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
4 Wire – 2 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
Power Supply Rejection Ratio					
V_{B+} to 2 Wire	30 – 60Hz, R_{LOOP} = 600Ω	15			dB
V_{B+} to Transmit		15			dB
V_{B-} to 2 Wire		15			dB
V_{B-} to Transmit		15			dB
V_{B+} to 2 Wire	200 – 16kHz	30			dB
V_{B+} to Transmit	R_{LOOP} = 600Ω	30			dB
V_{B-} to 2 Wire		30			dB
V_{B-} to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}				0.8	Volts
Logic '1' V_{IH}		2.0		5.5	Volts
Logic Outputs	Max Two LS Loads				
Logic '0' V_{OL}			0.1	0.5	Volts
Logic '1' V_{OH}		2.7	5.0	5.5	Volts

OVERVOLTAGE PROTECTION AND LONGITUDINAL CURRENT REJECTION

The SLIC-LC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC-LC will withstand longitudinal currents up to a maximum or 30mA rms, 15mA rms per leg, without any performance degradation.

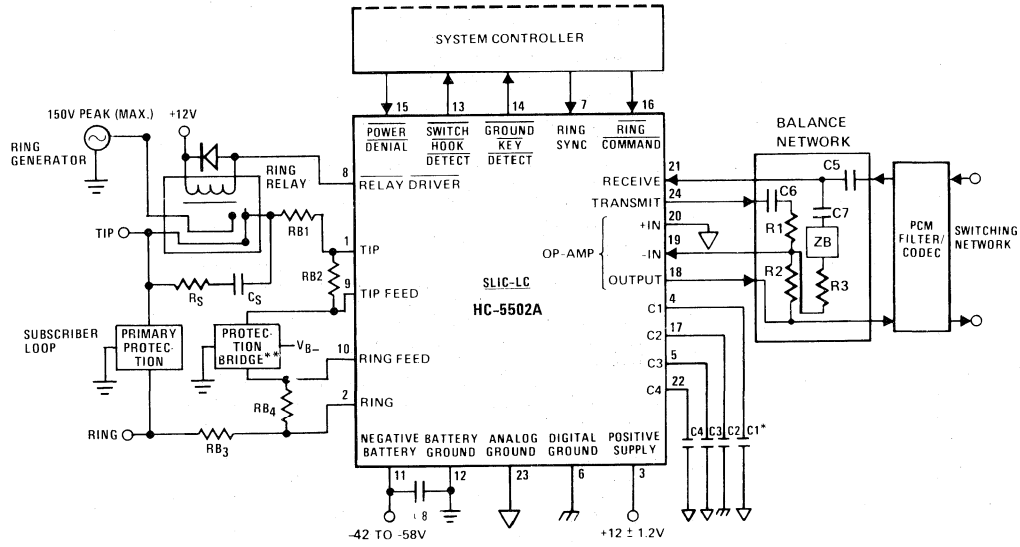
TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MIN)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	T	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω2feed resistor and a ring relay. Functions with the R terminal (Pin 2) to receive voice signals from the telephone and for Loop Monitoring Purposes.
2	R	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω2feed resistor. Functions with the T terminal (Pin1) to receive voice signals from the telephone and for loop monitoring purposes.
3	V_B+	Positive Voltage Source – Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
4	CAP 1	Capacitor #1 – Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
5	CAP 3	Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering -48V supply. Typical value is 0.3μF, 30V.
6	DG	Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
7	RS	Ring Synchronization Input – A TTL-compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
8	$\overline{RD}$	Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized. Maximum $\overline{RD}$ voltage is 15 volts.
9	TF	Tip Feed- A low impedance analog output connected to the T terminal (Pin 1) through a 150Ω2feed resistor. Functions with the RF terminal (Pin 10) to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	RF	Ring Feed - A low impedance analog output connected to the R terminal (Pin 2) through a 150Ω2feed resistor. Functions with the TF terminal (Pin 9) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	V_B-	Negative Voltage Source – Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
12	BG	Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection – A low active LS TTL -compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
14	$\overline{GKD}$	Ground Key Detection – A low active LS TTL -compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA , and disabled if this current difference is less than 10mA.
15	$\overline{PD}$	Power Denial – A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command – A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
17	CAP 2	Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.
18	OUT	The analog output of the spare operational amplifier.
19	-IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side – A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
22	CAP 4	Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF,to 1.0μF, 20V. This capacitor should be nonpolarized.
23	AG	Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side – A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONENT VALUES

* C1 = 0.5 μF
C2 = 0.15 μF, 10V
C3 = 0.3 μF, 30V
C4 = 0.5 μF to 1.0 μF, ±10%, 20V (Should be nonpolarized)
C5 = 0.5 μF, 20V
C6 = C7 = 0.5 μF (10% Match Required) Note 2, 20V
C8 = 0.01 μF, 100V

R1 → R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations Note 2
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)
R_S = 1KΩ, C_S = 0.1 μF ,200V typically, depending on V_{ring} and line length.

* NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1 μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op-amp output to the pcm Filter/CODEC.
A 0.5 μF and 100KΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

NOTE 3: Secondary protection diode bridge recommended is MDA 220 or similar.

HARRIS

HC-5504

SLIC-LC Subscriber Line Interface Circuit

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- ALLOWS INTERFACING WITH NEGATIVE SUPERIMPOSED RINGING SYSTEMS
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents.

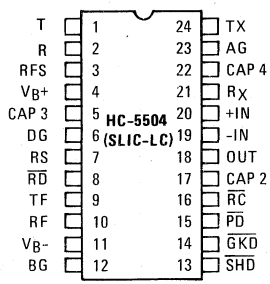
The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC-LC is ideally suited for the design of new PABX systems, by eliminating bulky, expensive hybrid transformers.

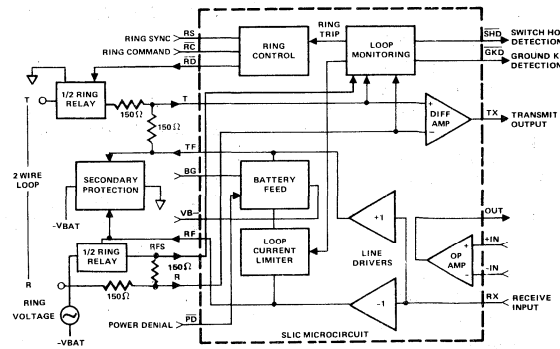
SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC-LC is also available in die form.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



8 COMMUNICATION

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages (V_{B-})	-60 to +0.5V
(V_{B+})	-.5 to +15V
($V_{B+} - V_{B-}$)	75V
Operating Ambient Temperature Range (T_A)	0°C to +75°C
Storage Temperature Range (R_{SRG})	-40°C to +85°C
Thermal Resistance (θ_{J-A}) (Plastic)	52°C/W
Thermal Resistance (θ_{J-A}) (Ceramic)	55°C/W

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (V_{B+})	10.8 to 13.2V
Negative Supply Voltage (V_{B-})	-42 to -58V
Mimimum High Level Logic Input Voltage	2.4V
Maximum Low Level Logic Input Voltage	0.8V
Loop Resistance (R_L)	200 to 1200Ω
Ambient Operating Temperature Range (T_A)	0°C to +70°C

ELECTRICAL CHARACTERISTICS V_{B-} = -48, V_{B+} = +12V, AG=BG=DG =0V, T_A =25°C Unless Otherwise Stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	$I_{Long.} = 0$		135	174	mW
Off Hook Power Dissipation	R_{LOOP} = 600 Ohms, $I_{Long.} = 0$		390	704	mW
Off Hook IB+	R_{LOOP} = 600 Ohms, $I_{Long.} = 0$		3	4.3	mA
Off Hook IB-	R_{LOOP} = 600 Ohms, $I_{Long.} = 0$		35	40	mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, $I_{Long.} = 0$		21		mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, V_{B-} = -42V, $I_{Long.} = 0$	17.5			mA
Off Hook Loop Current	R_{LOOP} = 200 Ohms, $I_{Long.} = 0$	36	41	48	mA
Fault Currents					
TIP to Ground			14		mA
RING to Ground			53		mA
TIP to RING			30		mA
TIP and RING to Ground			67		mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA		0.2	0.5	V
Ring Trip Detection Period	R_{LOOP} = 600 Ohms		2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10			mA
	$\overline{SHD} = V_{OH}$			5	mA
Ground Key Detection Threshold	$\overline{GKD} = V_{OL}$	20			mA
	$\overline{GKD} = V_{OH}$			10	mA
Dial Pulse Distortion		0		5	ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak (200Hz-3400Hz)				
2 Wire Off Hpok		58	65		dB
2 Wire On Hook		60	63		dB
4 Wire Off Hook		50	58		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC
Inspection Loss	@ 1kHz, 0dBm Input Level				
2 Wire - 4 Wire			±.05	±0.2	dB
4 Wire - 2 Wire			±.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02	±0.05	dB
Idle Channel Noise					
2 Wire - 4 Wire			1	5	dBrnC
4 Wire - 2 Wire			1	5	dBrnC
Absolute Delay					
2 Wire - 4 Wire				2	μs
4 Wire - 2 Wire				2	μs

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Envelope Delay					
2 Wire - 4 Wire				2	μs
4 Wire - 2 Wire				2	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40		dB
Overload Level					
2 Wire - 4 Wire		+4			dBm
4 Wire - 2 Wire		+4			dBm
Level Linearity	at 1kHz				
2 Wire - 4 Wire	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
4 Wire - 2 Wire	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
Power Supply Rejection Ratio					
VB+ to 2 Wire	30 – 60Hz, R_{LOOP} = 600Ω	15			dB
V_{B+} to Transmit		15			dB
V_{B-} to 2 Wire		15			dB
V_{B-} to Transmit		15			dB
V_{B+} to 2 Wire	200 - 16kHz	30			dB
V_{B+} to Transmit	R_{LOOP} = 600Ω	30			dB
V_{B-} to 2 Wire		30			dB
V_{B-} to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}		0.0		0.8	V
Logic '1' V_{IH}		2.0		5.5	V
Logic Outputs	Max Two LS Loads				
Logic '0' V_{OL}			0.1	0.5	V
Logic '1' V_{OH}		2.7		5.5	V

OVERVOLTAGE PROTECTION AND LONGITUDINAL CURRENT REJECTION

The SLIC-LC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC-LC will withstand longitudinal currents up to a maximum or 30mA rms, 15mA rms per leg, without any performance degradation.

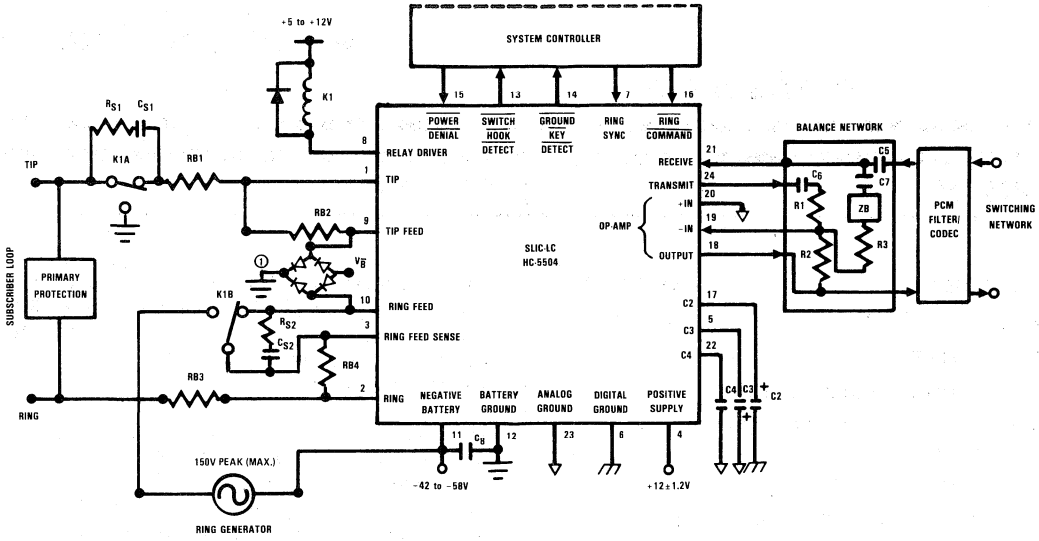
TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MIN)	UNITS
Longitudinal Surge	10 μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	T	An Analog input connected to the TIP (More Positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the R terminal (Pin 2) to receive voice signals from the telephone and for loop monitoring purposes.
2	R	An Analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the T terminal (Pin 1) to receive voice signals from the telephone and for loop monitoring purposes.
3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
4	V_B+	Positive Voltage Source—Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
5	CAP 3	Capacitor #3—An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering −48V supply. Typical value is 0.3μF, 30V.
6	DG	Digital Ground—To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	RS	Ring Synchronization Input—a TTL - compatible clock input. The clock is arranged such that a positive pulse (50-500μs) occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, then tie to +5V.
8	$\overline{RD}$	Relay Driver—a low active open collector logic output. When enabled, the external ring relay is energized. Maximum $\overline{RD}$ voltage is 15 volts.
9	TF	Tip Feed—A low impedance Analog output connected to the T terminal (Pin 1) through a 150Ω feed resistor. Functions with the RF terminal (Pin 10) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
10	RF	Ring Feed—A low impedance Analog output connected to the R terminal (Pin 2) through a 150Ω feed resistor. Functions with the TF terminal (Pin 9) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	V_B-	Negative Voltage Source—Most negative supply. VB− is typically −48 volts with an operational range of −42 to −58 volts. Frequently referred to as "battery."
12	BG	Battery Ground—To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection—A low active LS TTL-compatible logic output. This output is typically enabled for loop currents exceeding 7.5 mA and typically disabled for loop currents less than 7.5mA.
14	$\overline{GKD}$	Ground Key Detection—A low active LS TTL-compatible logic output. This output is typically enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 12.5 mA, and typically disabled if this current difference is less than 12.5mA.
15	$\overline{PD}$	Power Denial—A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$)and ground key detect ($\overline{GKD}$) are not necessarily valid and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command—A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ −0) or the subscriber is not already off-hook ($\overline{SHD}$ =0).
17	CAP 2	Capacitor #2—An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occuring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not needed if ground key function is not required and pin 17 may be left open or connected to digital ground.
18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
19	−IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side—A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
22	CAP 4	Capacitor #4—An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occuring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capactior is also required for the proper operation of ring trip detection. Typical value is 0.5μF to 1.0μF, 20V. This capacitor should be nonpolarized.
23	AG	Analog ground—To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side—A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

APPLICATIONS DIAGRAM



TYPICAL COMPONENT VALUES

C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μF – 1.0μF ±10%, 20V (Should be nonpolarized)
C5 = 0.5 μF, 20V
C6 = C_7 = 0.5 μF (10% Match Required) (2)
C8 = 0.01 μF, 100V
R1 = R2 = R3 = 100k (0.1% Match Required, 1% Absolute Value), ZB = 0 for 600Ω Terminations (2)
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% Absolute Value)
R_{S1} = R_{S2} = 1KΩ Typically
C_{S1} = C_{S2} = 0.1 μF, 200V typically, depending on V_{Ring} and line length

NOTES

(1) Secondary protection diode bridge recommended is an MDA 220 or similar.

(2) To obtain the specified transhybrid loss of 40dB it is necessary for the 3 legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. If C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -29 volt step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op-amp output to the PCM Filter/CODEC. A 0.5μF and 100kΩ gives a time constant of 50msec. The uncommited op-amp output is internally clamped to stay within ± 5.5V and also has current limiting protection.

HARRIS

HC-5510/HC-5511

Monolithic CODECs

Preliminary

FEATURES

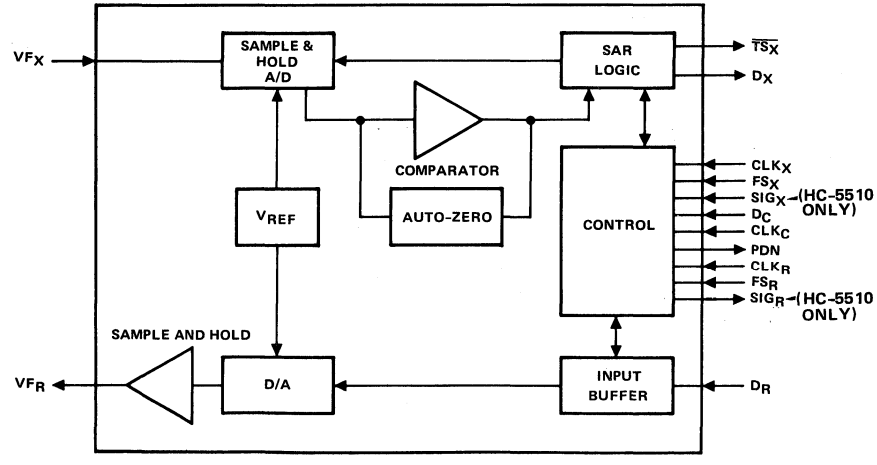
- LOW OPERATION POWER 45mW TYPICAL
- LOW STANDBY POWER 1mW TYPICAL
- ±5V OPERATION
- TTL COMPATIBLE DIGITAL INTERFACE
- TIME SLOT ASSIGNMENT OR ALTERNATE FIXED TIME SLOT MODES
- INTERNAL PRECISION REFERENCE
- INTERNAL SAMPLE AND HOLD CAPACITORS
- INTERNAL AUTO-ZERO CIRCUIT
- HC-5510 – μ-LAW CODING WITH SIGNALING CAPABILITIES
- HC-5511 – A-LAW CODING
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

DESCRIPTION

The HC-5510 and HC-5511 are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5510 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The HC-5511 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the HC-5510/HC-5511 may be operated in a fixed time slot mode. Both devices are intended to be used with the HC-5512/12A monolithic PCM filters which provide the input anti-aliasing function for the encoder and smooth the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-25°C to +125°C
Storage Temperature	-65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	-7V
Voltage at Any Input or Output	V_{BB} -0.3V to V_{CC} +0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, V_{BB} = -5.0V ± 5%. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = -5.0V and T_A = 25°C. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INTERFACE						
I_I	Input Current	-10		10	µA	$0 < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4 0.4 0.4 0.4	V V V V	D_X, I_{OL} = 4.0mA SIG_R, I_{OL} = 0.5mA $\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4 2.4			V V	D_X, I_{OH} = 6mA SIG_R, I_{OH} = 0.6mA
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	2.0			kΩ	Resistance in Series with Approximately 70pF
Z_O	Output Impedance at VF_R		10	20	Ω	-3.1V < VF_R < 3.1V
V_{OS}	Output Offset Voltage at VF_R	-25		25	mV	D_R = PCM Zero Code, HC-5510 or Alternating ±1 Code, HC-5511
I_{IN}	Analog Input Bias Current	-0.1		0.1	µA	V_{IN} = 0V
R1 x C1	DC Blocking Time Constant	4.0			ms	
C1	DC Blocking Capacitor	0.1			µF	
R1	Input Bias Resistor			160	kΩ	
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}		0.1	0.4	mA	
I_{BB0}	Standby Current, V_{BB}		0.03	0.1	mA	
I_{CC1}	Operating Current, V_{CC}		4.5	8.0	mA	
I_{BB1}	Operating Current, V_{BB}		4.5	8.0	mA	

AC ELECTRICAL CHARACTERISTICS Unless otherwise noted, the analog input is a 0dBm0, 1.02kHz sine wave. The digital input is a PCM bit stream generated by passing a 0dBm0, 1.02kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Absolute Level					The nominal 0dBm0 levels for the HC-5510 and HC-5511 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the HC-5510/ HC-5511 are based on these nominal levels after the necessary sin x/x corrections are made.
G_{RA}	Receive Gain, Absolute	-0.125		0.125	dB	T = 25°C, V_{CC} =+5V,V_{BB} = -5V
G_{RAT}	Absolute Receive Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} =-5V±5%
G_{XA}	Transmit Gain, Absolute	-0.125		0.125	dB	T = 25°C, V_{CC} = 5V, V_{BB} = -5V
G_{XAT}	Absolute Transmit Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V ±5%
G_{RAL}	Absolute Receive Gain Variation with Level					CCITT Method 2 Relative to -10dBm0
		-0.3		0.3	dB	0dBm0 to 3dBm0
		-0.2		0.2	dB	-40dBm0 to 0dBm0
		-0.4		0.4	dB	-50dBm0 to -40dBm0
		-1.0		1.0	dB	-55dBm0 to -50dBm0
G_{XAL}	Absolute Transmit Gain Variation with Level					CCITT Method 2 Relative to -10dBm0
		-0.3		0.3	dB	0dBm0 to 3dBm0
		-0.2		0.2	dB	-40dBm0 to 0dBm0
		-0.4		0.4	dB	-50dBm0 to -40dBm0
		-1.0		1.0	dB	-55dBm0 to -50dBm0
S/D_R	Receive Signal to Distortion Ratio					Sinusoidal Test Method Input Level
		35			dBc	-30dBm0 to 0dBm0
		29			dBc	-40dBm0
		25			dBc	-45dBm0
S/D_X	Transmit Signal to Distortion Ratio					Sinusoidal Test Method Input Level
		35			dBc	-30dBm0 to 0dBm0
		29			dBc	-40dBm0
		25			dBc	-45dBm0
N_R	Receive Idle Channel Noise			6	dBnrc0	D_R = Steady State PCM Code
N_X	Transmit Idle Channel Noise			13	dBrnc0	HC-5510, VF_X = 0V (no signalling)
				-67	dBm0p	HC-5511, VF_X = 0V
HD_R	Receive Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
HD_X	Transmit Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
$PPSR_R$	Positive Power Supply Rejection, Receive	40			dB	D_R = Steady PCM Code, V_{CC} = $5.0V_{DC}$ +20mVrms, f = 1.02kHz
$PPSR_X$	Positive Power Supply Rejection, Transmit	50			dB	Input Level = 0V, V_{CC} = $5.0V_{DC}$ +20mVrms, f = 1.02kHz
$NPSR_R$	Negative Power Supply Rejection, Receive	45			dB	D_R = Steady PCM Code, V_{BB} = $-5.0V_{DC}$ +20mVrms, f = 1.02kHz
$NPSR_X$	Negative Power Supply Rejection Transmit	50			dB	Input Level = 0, V_{BB} = $-5.0V_{DC}$ +20mVrms, f = 1.02kHz
CT_{XR}	Transmit to Receive Crosstalk			-75	dB	D_R = Steady PCM Code
CT_{RX}	Receive to Transmit Crosstalk					Transmit Input Level = 0V
				-70	dB	HC-5510
				-65	dB	HC-5511

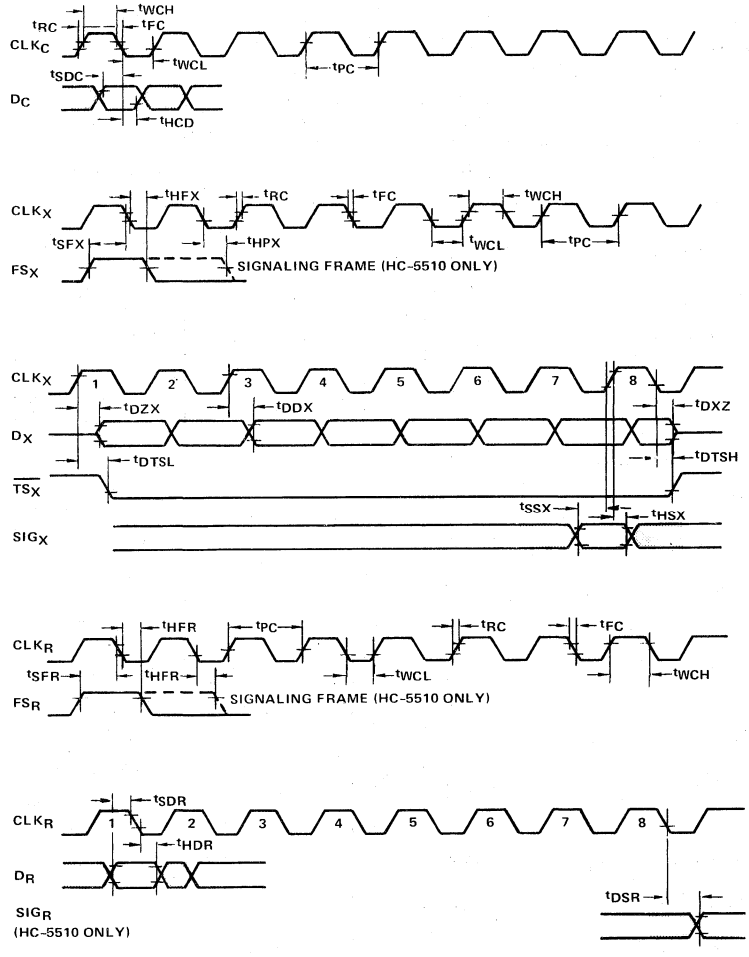
SPECIFICATIONS (Continued)

TIMING SPECIFICATIONS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ±5%, V_{BB} = -5.0 ±5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the timing waveforms.

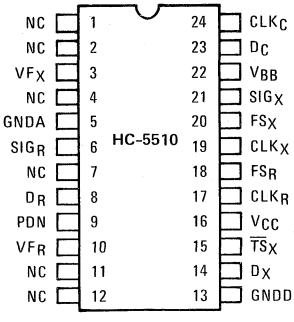
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PC}	Period of Clock	488			ns	CLK_C, CLK_R, CLK_X
t_{RC}, t_{FC}	Rise and Fall Time of Clock			30	ns	CLK_C, CLK_R, CLK_X
t_{WCH}	Width of Clock High	165			ns	CLK_C, CLK_R, CLK_X
t_{WCL}	Width of Clock Low	165			ns	CLK_C, CLK_R, CLK_X
$t_{A/D}$	A/D Conversion Time			16	Time Slots	From End of Encoder Time Slot to Completion of Conversion
$t_{D/A}$	D/A Conversion Time			2	Time Slots	From End of Decoder Time Slot to Transition of VF_R
t_{SDC}	Set-Up Time, D_C to CLK_C	100			ns	
t_{HDC}	Hold Time, CLK_C to D_C	100			ns	
t_{SFC}	Set-Up Time FS_X or CLK_X	100			ns	
t_{HFX}	Hold Time, CLK_X to FS_X	100			ns	
t_{DZX}	Delay Time to Enable D_X on TS Entry	25		125	ns	C_L = 150pF
t_{DDX}	Delay Time, CLK_X to D_X			125	ns	C_L = 150pF
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	50		165	ns	C_L = 0pF
t_{DTSL}	Delay to $\overline{TS}_X$ Low	30		185	ns	$0 \leq C_L \leq 150pF$
t_{DTSH}	Delay to $\overline{TS}_X$ Off	30		185	ns	C_L = 0pF
t_{SSX}	Set-Up Time, SIG_X to CLK_X	100			ns	
t_{HSX}	Hold Time, CLK_X to SIG_X	100			ns	
t_{SFR}	Set-Up Time, FS_R to CLK_R	100			ns	
t_{HFR}	Hold Time, CLK_R to FS_R	100			ns	
t_{SDR}	Set-Up Time, D_R to CLK_R	40			ns	
t_{HDR}	Hold Time, CLK_R to D_R	30			ns	
t_{DSR}	Delay Time, CLK_R to SIG_R			300	ns	C_L = 100pF

TIMING WAVEFORMS

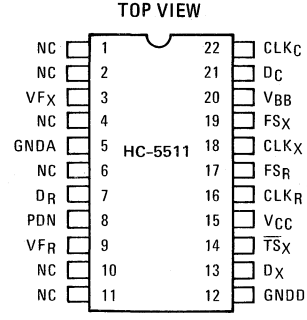


PINOUTS

TOP VIEW



TOP VIEW



PIN ASSIGNMENTS

HC-5510

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	-5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlay a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

HC-5511

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DR, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most signficant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz, or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	-5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or -5V is required. In the power-down mode, all non-essential circuits are deactivated, the Three-State PCM data output D_X is placed in the high impedance state and the receive signaling output of the HC-5510, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the HC-5510/5511 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequential control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputed during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the HC-5510/5511 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the HC-5510/HC-5511 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The HC-5510 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

FUNCTIONAL DESCRIPTION (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048MHz clock, the FS rate could be increased to 15kHz reducing the delay from 125μs to 67μs.

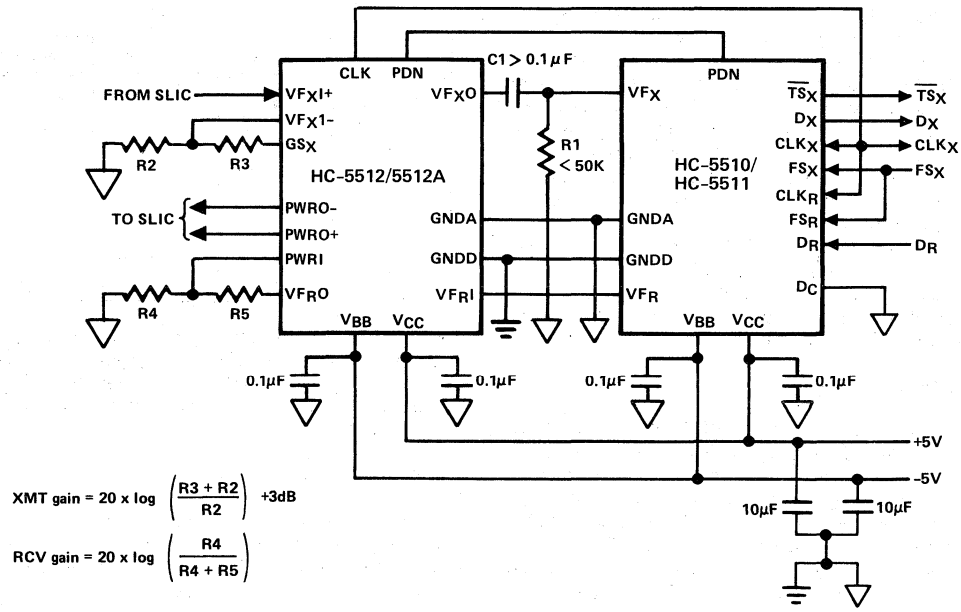
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81μs for a 1.544MHz system with an 8kHz frame rate or 76μs for a 2.048MHz system with an 8kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the HC-5510/11 used in conjunction with the HC-5512/12A PCM filter is shown. The values of resistor R1 and D_C blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1μF, R1 should be less than 50kΩ , and the product R1 x C1 should exceed 4ms.

TYPICAL APPLICATION



The power supply decoupling capacitors should be 0.1μF. In order to take advantage of the excellent noise performance of the HC-5510/HC5511/HC-5512, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. The above application is configured for a fixed time slot mode of operation.

HARRIS

HC-5512/5512A

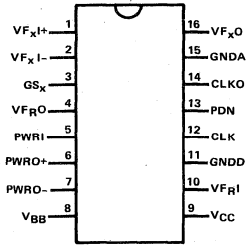
PCM Monolithic Filter

FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  - 45mW (600Ω 0dBm LOAD)
  - 30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW



DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

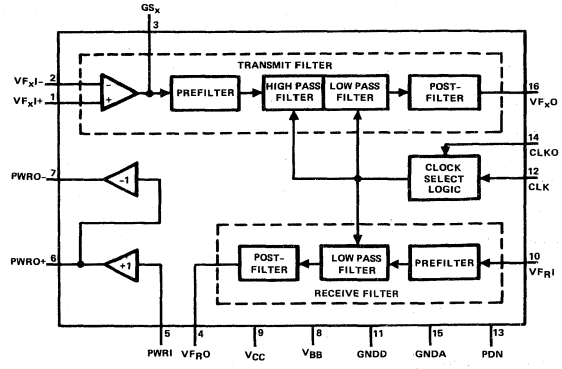


FIGURE 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-25°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V±5%, V_{BB} = -5.0V ±5%, clock frequency is 1.544MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	-10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	-100			μA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC}$ -0.5V	-10		-0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}-0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_x I$	Input Leakage Current, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	-100		100	nA
$RI_x I$	Input Resistance, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	10			MΩ
$VOS_x I$	Input Offset Voltage, $VF_x I$	$-2.5V \le V_{IN} \le +2.5V$	-20		20	mV
V_{CM}	Common-Mode Range, $VF_x I$		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \le V_{IN} \le 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
$VO_x I$	Output Voltage Swing, GS_x	$R_L \ge 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_xI = 1.09 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, VF_xI+ = 0 Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (HC-5512A)	2.9	3.0	3.1	dB
		f = 1 kHz (HC-5512)	2.875	3.0	3.125	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (HC-5512A)	−1.5		0	dB
		200 Hz (HC-5512)	−1.5		0.05	dB
		300 Hz to 3 kHz (HC-5512A)	−0.125		0.125	dB
		300 Hz to 3 kHz (HC-5512)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 T_A = 0°C to 70°C		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	V_{CC} = 5.0V ± 5% V_{BB} = −5.0V ± 5%		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \leq V_{IN} \leq 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (HC-5512A) f = 1 kHz (HC-5512)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (HC-5512A) 300 Hz to 3.0 kHz (HC-5512) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_xO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

SPECIFICATIONS

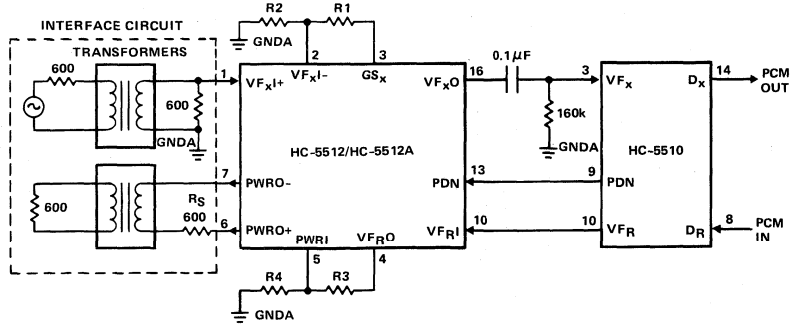
AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A =25°C. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_P+	Gain, PWRI to PWRO+	R_L = 600Ω Connected Between		1		V/V
GA_P-	Gain, PWRI to PWRO−	PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5)	−0.1		0.1	dB
		V = 1.75 Vrms, R_L = 300Ω (Notes 4, 5)	−0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5)			−45	dB
		V = 1.75 Vrms, R_L = 300Ω (Notes 4, 5)			−45	dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The odBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for R_L = 300Ω the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

INTERFACE CIRCUIT FOR HC-5510 CODEC



Note 1: Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k).

Note 2: Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10k)

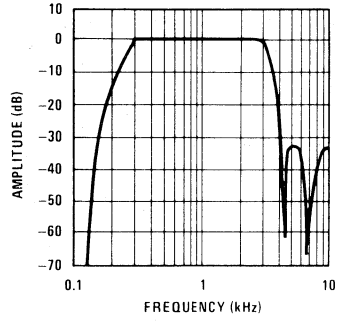
Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

PIN ASSIGNMENTS

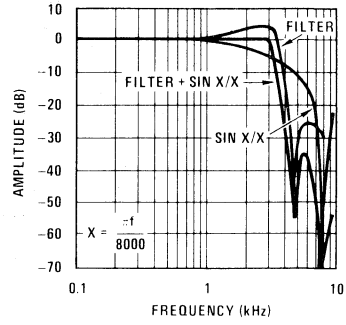
Pin No.	Name	Function
1	VF_xI+	The non-inverting input to the transmit filter stage.
2	VF_xI-	The inverting input to the transmit filter stage.
3	GS_x	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO–	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is –5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512/12A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048 kHz — V_{CC} 1544 kHz — GNDD 1536 kHz — V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_xO	The output of the transmit filter stage.

TYPICAL PERFORMANCE CHARACTERISTICS

Transmit Filter Stage



Receive Filter Stage



FUNCTIONAL DESCRIPTION

The HC-5512/12A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 5,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband reejction and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to V_{BB}, the power amplifier output will enter a high impedance (tri-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

APPLICATIONS INFORMATION

Gain Adjust

Figure 2 shows the signal path interconnections between the HC-5512/12A and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained for the HC-5512/12A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO. When interfacing to a PCM CODEC with a peak overload voltages outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

HARRIS

HC-5512C

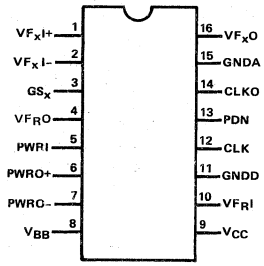
PCM or CVSD Monolithic Filter

FEATURES

- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  - 45mW (600Ω 0dBm LOAD)
  - 30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW



DESCRIPTION

The HC-5512C filter is a monolithic circuit containing both transmit and receive filters originally designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter lends itself well as a cost effective replacement of a discrete audio input/output filter for the continuously variable slope delta modulator (CVSD).

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

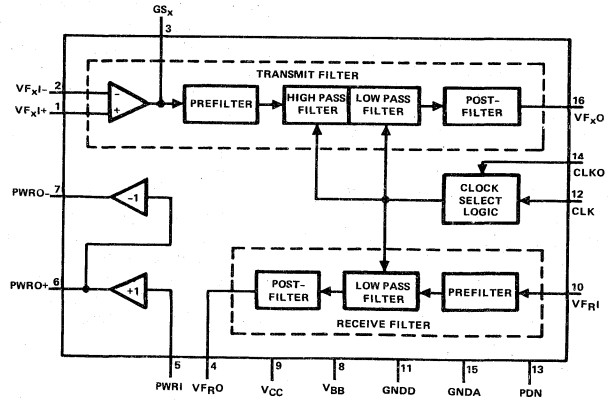


FIGURE 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-25°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, V_{BB} = -5.0V ±5%, clock frequency is 1.544MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	µA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.5	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.5	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	GNDD ≤ V_{IN} ≤ V_{CC}	-10		10	µA
I_{INP}	Input Current, PDN	GNDD ≤ V_{IN} ≤ V_{CC}	-100			µA
I_{IN0}	Input Current, CLK0	GNDD ≤ V_{IN} ≤ V_{CC} - 0.5V	-10		0	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}-0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_x I$	Input Leakage Current, $VF_x I$	V_{BB} ≤ $VF_x I$ ≤ V_{CC}	-100		100	nA
$RI_x I$	Input Resistance, $VF_x I$	V_{BB} ≤ $VF_x I$ ≤ V_{CC}	10			MΩ
$VOS_x I$	Input Offset Voltage, $VF_x I$	-2.5V ≤ V_{IN} ≤ +2.5V	-20		20	mV
V_{CM}	Common-Mode Range, $VF_x I$		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	-2.5V ≤ V_{IN} ≤ +2.5V	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
$VO_x I$	Output Voltage Swing, GS_x	R_L ≥ 10k	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	R_L ≥ 10k	3400			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = 25^oC$. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_XI = 1.09 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	30			dB
GA_x	Absolute Gain	f = 1 kHz	2.8	3.0	3.2	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz	−1.5		0.2	dB
		300 Hz to 3 kHz	−0.15		0.15	dB
		3.3 kHz	−0.45		0.25	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−40	dB
DP_x2	Distortion at Maximum Signal Level	0.16Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−40	dB
NC_x1	Total C Message Noise at VF_xO with $V_{IN} = 0$				10	dBrnc0
NC_x2	Total C Message Noise at VF_xO with $V_{IN} = 0$	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3			10	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms, $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz, Measure VF_xO			−60	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = 25^oC$. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-2.5V \leq V_{IN} \leq 2.5V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	30			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz	−0.2	0	0.2	dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz			0.125	dB
		300 Hz to 3.0 kHz	−0.15		0.15	dB
		3.3 kHz	−0.45		0.25	dB
		3.4 kHz	−0.7		−0.1	dB
		4.0 kHz			−14	dB
		4.6 kHz and Above			−32	dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−40	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−40	dB
NC_R	Total C-Message Noise at VF_RO				10	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_xO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−60	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0 Note 5	−0.1		0.1	dB

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = 25^0C$. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-2.5V \leq V_{IN} \leq 2.5V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO +, PWRO –	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO +, PWRO –				500	pF
GA_P+	Gain, PWRI to PWRO +	$R_L = 600\Omega$ Connected Between		1		V/V
GA_P-	Gain, PWRI to PWRO –	PWRO + and PWRO –, Input Level = 0 dBm0 (Note 4)		–1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5) V = 1.75 Vrms, $R_L = 300\Omega$	– 0.1 – 0.1		0.1 0.1	dB dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5) V = 1.75 Vrms, $R_L = 300\Omega$			– 45 – 45	dB dB
VOSP	Output DC Offset, PWRO +, PWRO –	PWRI Connected to GNDA	– 50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ωconnected from PWRO+ to PWRO–.
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO–. Output measured from PWRO+ to PWRO–.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The 0dBm0 level for the power amplifiers is load dependent. For $R_L = 600\Omega$ to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for $R_L = 300\Omega$ the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS

Transmit Filter Stage

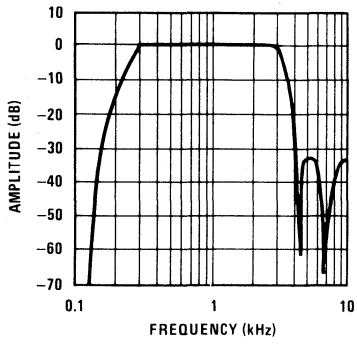


FIGURE 2

Receive Filter Stage

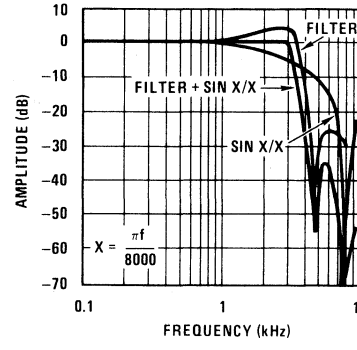


FIGURE 3

PIN ASSIGNMENTS

Pin No.	Name	Function
1	VF_xI+	The non-inverting input to the transmit filter stage.
2	VF_xI-	The inverting input to the transmit filter stage.
3	GS_x	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO–	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is –5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512C during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** **Connect CLK0 to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_xO	The output of the transmit filter stage.

FUNCTIONAL DESCRIPTION

The HC-5512C monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 5,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by a least 40dB. The output of the transmit filter is capable of driving a ±2.5V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits in PCM applications. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 4)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

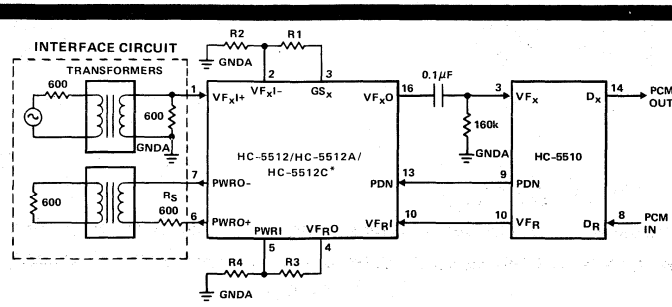
Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to V_{BB}, the power amplifier output will enter a high impedance (tri-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

INTERFACE CIRCUIT FOR HC-5510 CODEC



Note 1: Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k).

Note 2: Receive gain = $\frac{R4}{R3 + R4}$ (R3 + R4 ≥ 10k)

Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

*Note 4: Although the HC-5512C may be used in some PCM telephone applications, it does not meet CCITT and D3/D4 specifications for PCM telephone transmission systems.

FIGURE 4

INTERFACE CIRCUIT FOR HC-55564 CVSD

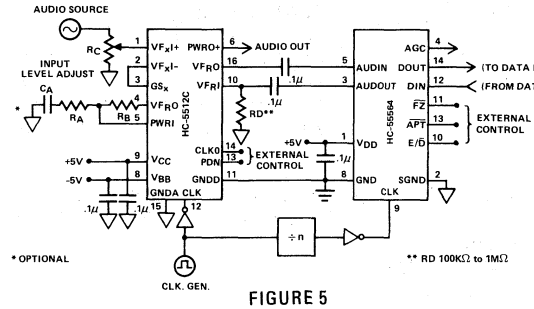


FIGURE 5

APPLICATIONS INFORMATION

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512C and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512C and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead lag filter at the output of the HC-5512C receive filter which introduces a pole and a zero at 3.3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100KΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512C filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/5512A/5512C filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground of each filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.

HARRIS

HC-5521A

SLIC-HC Subscriber Line Interface Circuit

Preliminary

FEATURES

- DESIGNED TO MEET C. O. QUALITY TRANSMISSION REQUIREMENTS
- USER PROGRAMMABLE BATTERY FEED CHARACTERISTICS
- GENERATION OF RINGING VOLTAGE ON CHIP
- TERMINATING IMPEDANCE USER ADJUSTABLE
- ALL SUPERVISORY FUNCTIONS INTEGRATED ON CHIP
- HYBRID FUNCTIONS REALIZED THROUGH ELECTRONIC CIRCUITRY
- ON-HOOK AND OFF-HOOK INJECTION OF 12 TO 16kHz METERING SIGNALS
- REDUCED POWER DISSIPATION FOR SHORT LOOPS
- STANDARD DIGITAL INTERFACE FOR I/O CONTROL
- HIGH VOLTAGE FUNCTIONS INTEGRATED IN UNIQUE DIELECTRIC ISOLATION (DI) TECH.

APPLICATION

- SOLID STATE LINE INTERFACE CIRCUIT FOR DIGITAL PABX AND C. O. SWITCHES

DESCRIPTION

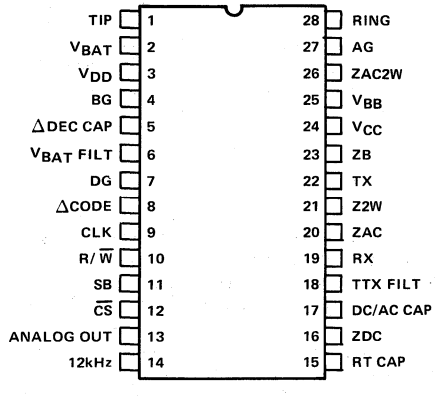
HC-5521A is an advanced, state-of-the-art integrated chip set designed to provide most of the BORSHT functions with On Chip power devices. This includes battery feed, ringing, supervision and hybrid functions. This device is designed to meet stringent C. O. transmission and signalling requirements. Functions have been optimally partitioned according to technology requirements into two chips. First chip incorporates all of the high voltage functions required for interfacing to a subscriber line in DI technology; low voltage functions are implemented in a standard Junction Isolation technique. Two chips are bonded together in a custom 28 pin Dual-In-Line package.

The SLIC-HC provides programmable feed characteristics to the loop. For short loops, the line feed can be accomplished with a lower battery voltage to minimize power to the subscriber loop. The device maintains transmission performance even in presence of externally induced longitudinal voltage.

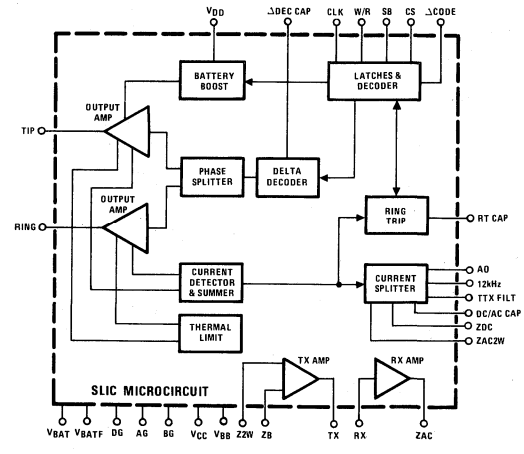
Digital I/O interface is designed to operate in a bus configuration, thus allowing several SLIC devices to be controlled from a single processor.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages	(V_{BAT})	-75 to +0V
	(V_{DD})	+80V
	($V_{DD} + V_{BAT}$)	TBD
Maximum DC Metallic Loop Current (I_{LOOP})		61.8mA
Storage Temperature Range (R_{srg})		-40°C to 85°C
Operating Ambient Temperature Range (T_A)		0°C to 75°C
Maximum Off Hook Power Dissipation		PDO 2.7 Watt
Maximum Power Dissipation during ringing with admissable longitudinal currents and 30% duty cycle on ring cadence.		P_{RING} 1.3 Watts

RECOMMENDED OPERATING CONDITIONS

Operating Voltage	V_{BAT}	-30 to -56 Vdc
	*V_{BAT} FILT	-30 to -56 Vdc
	V_{DD}	+50 to +70 Vdc
	V_{CC}	+5 ± 10%Vdc
	V_{BB}	-5 ± 10% Vdc
Metallic Loop Current Range		I_{LOOP} 20 to 61.8mA
**Ring Voltage Range		V_{RING} 50 to 70 Vrms

* This voltage cannot go more negative than VB-.

**Magnitude of the positive voltage required for generating specified ringing voltage is given by the following equation: $V_{DD} = V_{RING}$ (RMS) x 1.414 + 23.2 - $|V_{BAT}|$.

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{BB} = -5V, V_{BAT} FILT = V_{BAT}, AG = BG = DG = 0)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BATTERY FEED					
Open Loop Voltages		31.2			Volts
Loop Current Feed Characteristics (Programmable)					
2 Wire Input Impedance		400		600	Ohms
Boost Voltages		+60		+70	Volts
Longitudinal Balance Off-Hook	300 - 3400Hz	52			dB
On-Hook	10 - 3400Hz	30			dB
Loop Current Variation after Polarity Reversal				± 1%	
Polarity Reversal Time Constant				16	ms
Power Denial Mode Loop Current				4	mA
Forced Release Standby Current		14.5			mA
On-Hook Power Dissipation				85	mW
On-Hook Half Power Detection Threshold		TBD			
RINGING *					
Ringing Frequency (Programmable)				50	Hz
Ringing Current				45	mA_{rms}
Harmonic Distortion				5%	
AC Ringing Leakage on Transmit Lead	Test with 600 connected to TX Lead			0.1	mA
Ring Trip Detection Threshold		10			mA
Ring Trip Detection Period				150	ms
Cadenced Ringing Ring Time				1.7	μs
On/Off Duty Cycle				0.6	
SIGNALLING					
Off-Hook Detection Sense Loop Current		8		10	mA
On-Hook Detection Sense Loop Current		4		7	mA
Dialing Speed				22	Pulses/s
Dial Pulse Off/On Time Ratio		0.3		3	
Dial Pulse Distortion				3	ms
Off-Hook Detection Response Time			10	ms	

*The limits established in this specification refer to a ringer load of 1K ohms in series with two microfarads. For other ringer loads, safe operating regions and compliance between ringer load, frequency and voltage has to be established.

SPECIFICATIONS (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMISSION					
Two Wire Return Loss	300 - 500Hz	16			dB
	500 - 3400Hz	20			dB
Insertion Loss 2W/4W	300 - 3400Hz		±0.05		dB
4W/2W	300 - 3400Hz		±0.05		dB
Level Linearity	+3 to -40dBm		±0.05		dB
	-40 to -50dBm		±0.1		dB
2W/4W & 4W/2W	-50 to -55dBm		±0.3		dB
Overload Level 2W/4W & 4W/2W	300 - 3400Hz	+3.17			dBm
4 Wire Longitudinal Balance	180 - 3400Hz	50			dB
Low Frequency 4 Wire Longitudinal Balance	50 - 60Hz			23	dBrnc
Admissable Low Frequency Longitudinal Current				15	mA
Trans-Hybrid Loss	Balance Network optimized appropriate terminating impedance	40	45		dB
Absolute Delay				TBD	μs
Envelope Delay				TBD	μs
Harmonic Distortion				0.15	%
Idle Channel Noise					
2W/4W	Input Terminated			5	dBrnc
4W/2W (Note 1, 9)	Output Terminated			5	dBrnc
Power Supply Rejection	2V Peak-Peak @ 60Hz/100mV				
2W/4W	Peak-Peak from 300 to 1kHz	30			dB
4W/2W	injected on to the battery	30			dB
ANALOG INTERFACE					
Input Impedance of Receive Port		1			Megaohms
Output Impedance of Transmit Port				10	Ohms
Output Voltage Swing	R_L = 19K, f = 1kHz	±3.2			Volts
Analog Output Voltage Range				-3.0	Volts
METERING PULSES					
Metering Signal Port Input Imped.		10			Kilohms
Metering Filter Port Impedance		800		1200	Ohms
Metering Pulse Frequency		12		16	kHz
Signal Level on Subscriber Loop	R_L = 200 Ohms			2	V_{rms}
LOGIC INTERFACE					
Logic "0" Input Voltage V_{IL}				0.4	Volts
Logic "1" Input Voltage V_{IH}		2.0			Volts
Logic "0" Input Current for Serial I/O Bus		TBD			μA
Logic "0" Input Current I_{JL}		40			μA
Logic "0" Output Voltage V_{OL}	I_{OL} = 800μA			0.4	Volts
Logic "0" Output Voltage V_{OH}	I_{OH} = 40μA	2.4			Volts
Clock Frequency				100	kHz

SPECIFICATIONS (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HIGH VOLTAGE PROTECTION **					
Longitudinal Surge	10μs Rise - 1000μs Fall	±1000			V_{PEAK}
Metallic Surge	10μs Rise - 1000μs Fall	±1000			V_{PEAK}
T/GND, R/GND	10μs Rise - 1000μs Fall	±1000			V_{PEAK}
60Hz Current, T/GND, R/GND (Note 10)	700V_{RMS} Limited	11			Cycles
Additional Operating Characteristics					
Common Mode Voltage Difference between Analog Ground and Digital Ground				300	mV
High Voltage Isolation ***					
Metallic		250			V_{rms}
Tip/GND, Ring/GND		250			V_{rms}
Longitudinal		250			V_{rms}

** In conjunction with external protection device.

***Presence of continuous voltage may cause permanent damage to the device, but will not result in a fire hazard.

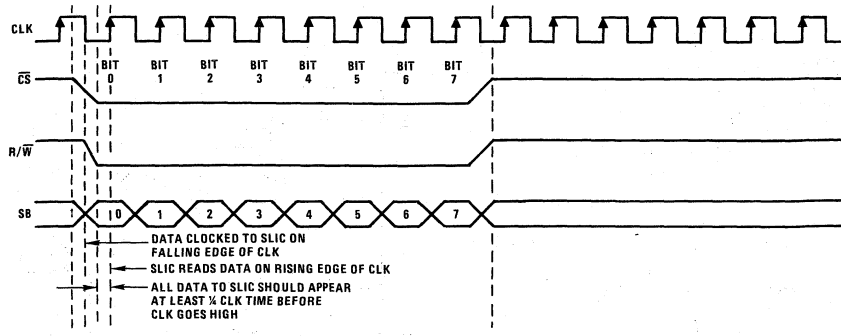
Tip and Ring outputs will be able to sustain the following output shorts:

- Tip to Ring
- Tip to Ground
- Ring to Ground
- Tip and Ring to Ground

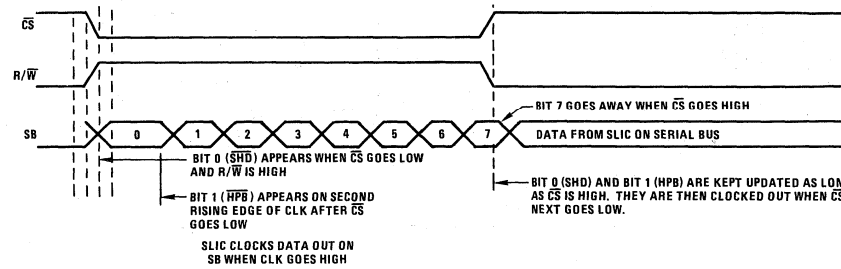
PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	TIP	A low impedance analog output which provides loop feed current voice signals and sinks longitudinal current.
2	V_{BAT}	Most negative voltage source . V_{BAT} has a range of -30 to -56 volts.
3	V_{DD}	+60V supply. Needed for ringing voltages and battery boost.
4	BG	Battery ground. To be connected to zero potential. All loop current flows into this terminal.
5	ΔDECCAP	This capacitor decodes delta code pulses into a smooth ringing waveform. Typical value is 10nf, bi-directional, 100V.
6	V_{BAT} FILT	Filtered negative voltage source. Same range as V_{BAT}.
7	DG	Digital ground. Connected to zero potential, serves as reference for the digital circuitry.
8	ΔCODE	Delta code input. TTL compatible input which generates ringing signals.
9	CLK	Clock input. TTL compatible 100kHz clock strobes the data into the SLIC.
10	R/$\overline{W}$	Read/Write input. Control input port which determines status of bi-directional data bus.
11	SB	Serial bus. Data is written into or read out of the SLIC on this bus.
12	CS	Chip select. This input determines if the data will be written into the SLIC.
13	ANALOG OUT	Analog output voltage. This output is an image of the differential TIP-RING voltage divided by twenty.
14	12kHz	Twelve kilohertz oscillator input for teletax metering signals.
15	RT CAP	Ring trip capacitor is typically 0.1μf, bi-directional, 10V.
16	ZDC	DC impedance setting resistor. Determines the DC resistive feed characteristics. ZDC = 25 (Total DC input impedance - total protect. impedance).
17	DC/AC CAP	DC/AC Current splitting capacitor. Should be greater than 10μf with 25V compliance.
18	TTX FILT	Teletax filter. A series LC filter must be hooked to this node. It should be notched at 12kHz.
19	RX	Receive input.
20	ZAC	AC input impedance adjustment. ZAC = 50X total AC input impedance.
21	Z2W	Protection resistor adjustment. Gain compensation resistor, Z2W = 50X total protection resistant (60Ω in our application diagram)
22	TX	Transmit output. Short circuit current protection is provided.
23	ZB	Balance impedance adjustment, ZB is set to 50X line balance impedance.
24	VCC	+5V supply. Tolerance is ± 10%.
25	VBB	-5V supply. Tolerance is ± 10%.
26	ZAC2W	Return path for the AC input impedance and protection resistor adjustments.
27	AG	Analog ground. Connected to zero potential, serves as reference for the analog circuitry.
28	RING	In conjunction with TIP, a low impedance analog output which provides loop feed current, voice signals and sinks longitudinal current.

WRITE CYCLE



READ CYCLE



NOTE: 1. SHD = SWITCH HOOK DETECTION; HPB = SHORT LOOP INDICATION.
2. ACTUAL DELAYS, SET UP TIMES, RISE AND FALL TIMES ARE TBD.

POWERING ORDERS

ORDER	B7	B6	B5	B4	B3	B2	B1	B0
Normal Feed 60mA	1	0	0	0	0	X	X	X
Normal Feed 45mA	1	0	0	1	0	X	X	X
Normal Feed 30mA	1	0	1	0	0	X	X	X
Normal Feed 15mA	1	0	1	1	0	X	X	X
Reverse Feed 60mA	1	0	0	0	1	X	X	X
Reverse Feed 45mA	1	0	0	1	1	X	X	X
Reverse Feed 30mA	1	0	1	0	1	X	X	X
Reverse Feed 15mA	1	0	1	1	1	X	X	X
Ring Command	1	1	0	0	0	X	X	X
Positive Power Denial	1	1	0	1	0	X	X	X
Negative Power Denial	1	1	1	0	0	X	X	X
Metering Signal ON	1	X	X	X	X	1	X	X
Battery Boost	1	X	X	X	X	X	1	X
No Execute	0	X	X	X	X	X	X	X

B3 - B6 Represent mutually exclusive powering orders.
B1 - B2 Represent nonmutually exclusive powering orders.
B0 Is not used, (X = Don't Care).
B7 Validates the input data by allowing data to be latched into the SLIC upon completion of Read/Write cycle.

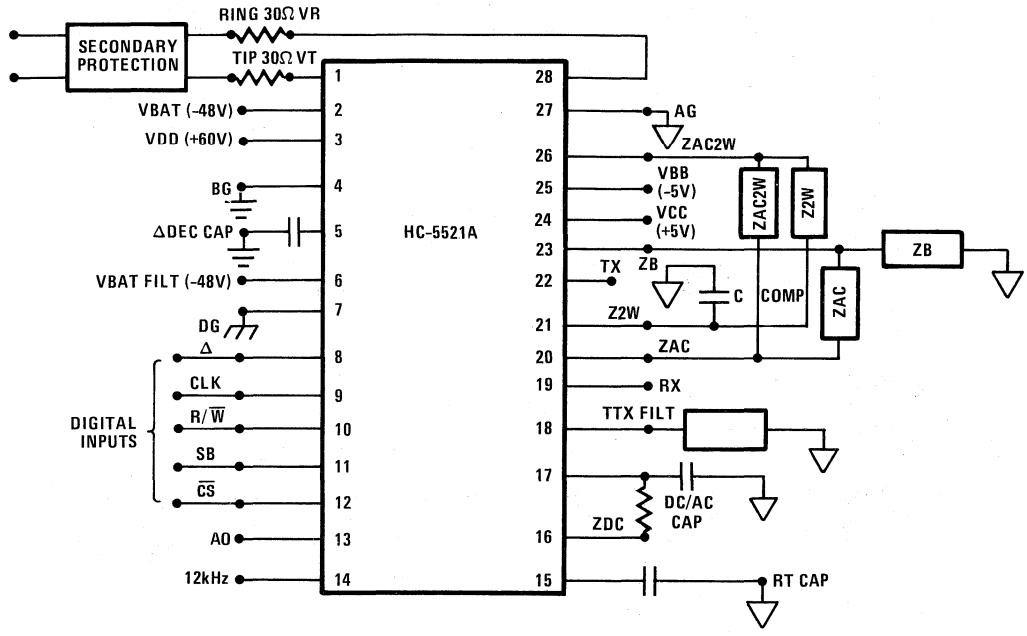
LINE STATUS OUTPUT FORMAT

Switch hook detection (SHD) and half power (HP)* are loaded asynchronously into bits B0 and B1, respectively.

LINE STATUS	B1	B0
Half Power	1	0
Switch Hook Detection	0	1
Idle Condition	0	0
Half Power and Switch Hook Detection	1	1

*Half power bit indicates presence of a short subscriber line.

APPLICATION DIAGRAM



HARRIS

HC-5552/53/54/57

Monolithic CMOS Serial Interface CODEC/Filter Family

Preliminary

FEATURES

COMPLETE CODEC/FILTER (COMBO) FAMILY

- HC-5552 μ-LAW WITH SHORT FRAME SIGNALLING (18 PIN)
- HC-5553 μ-LAW WITH BOTH SHORT AND LONG FRAME SIGNALLING (20 PIN)
- HC-5554 μ-LAW WITHOUT SIGNALLING (16 PIN)
- HC-5557 A-LAW (16 PIN)
- LOW POWER CONSUMPTION (60mW TYPICAL)
- LOW STANDBY POWER (2mW TYPICAL)
- $\pm$ 5V OPERATION
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECS
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- PCM DATA SERIAL INPUT/OUTPUT
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- TIMING COMPATIBLE WITH BOTH INDUSTRY-STANDARD FORMATS
- AUTOMATIC POWER-DOWN

DESCRIPTION

The Harris CODEC/Filter (Combo) Family includes A-Law and μ-Law monolithic CODEC/Filters implemented with double-poly CMOS technology.

The Transmit side of the device consists of an:

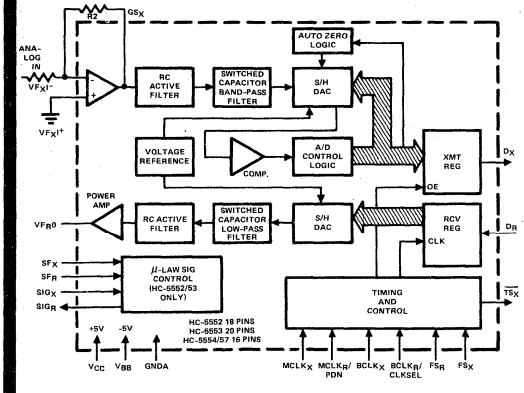
- amplifier with external gain adjust
- RC active prefilter to eliminate phasing of high frequency noise into the passband.
- switched capacitor band-pass filter (including a notch filter at 55Hz) to reject signals below 200Hz and above 3400Hz
- charge-redistribution coder which samples and encodes the filtered signal in the companded μ-Law or A-Law PCM format
- precision voltage reference
- internal auto-zero network to cancel the transmit offset

The Receive side of the device consists of an:

- expanding decoder to reconstruct the analog signal from the companded μ-law or A-law code.
- switched capacitor low-pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400Hz
- RC active post filter followed by a single ended power amplifier able to drive a 600 ohm load

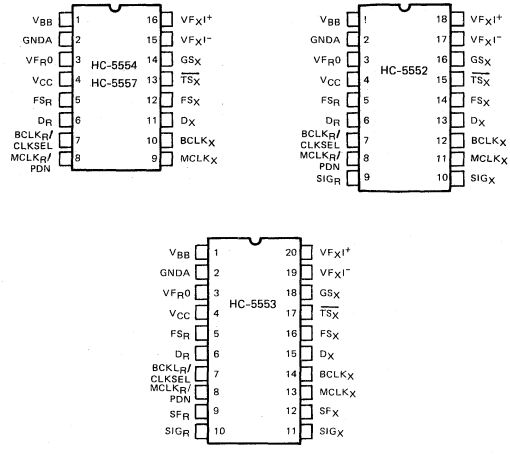
The device is operated with two (transmit and receive) master-clocks (1.536MHz, 1,544MHz or 2.048MHz), which may be asynchronous; transmit and receive bit clocks which may vary from 64kHz to 2.048MHz; and transmit and receive Frame Sync Pulses.

FUNCTIONAL DIAGRAM



PINOUTS

DUAL-IN-LINE PACKAGES
TOP VIEWS



5552 PIN NO.	5553 PIN NO.	5554/57 PIN NO.	NAME	FUNCTION
1	1	1	VBB	-5V (± 5%) Negative Power Supply.
2	2	2	GNDA	Analog Ground. All Signals are referenced to this pin.
3	3	3	VFR_O	Analog Output of the Receive Filter.
4	4	4	V_{CC}	5V (± 5%) Positive Power Supply.
5	5	5	FS_R	Receive Frame Sync Pulse. An 8kHz pulse train which enable $BCLK_R$ to shift PCM data into the receive register.
6	6	6	D_R	Receive Data Input. The receive register clocks in DR input with the $BCLK_R$ falling edge following an FS_R rising edge.
7	7	7	$BCLK_R$/ CLKSEL	Bit Clock which shifts D_R input into the Receive Register. May vary from 64kHz to 2.048MHz. Alternatively may be a Clock Selection Input.
8	8	8	$MCLK_R$/ PDN	Receive Master Clock must be 1.536 or 1.544 or 2.084MHz. May be asynchronous with $BCLK_R$. If $MCLK_R$ is tied Low, the Combo operates in synchronous mode. If $MCLK_R$ is tied High, the Combo is powered down.
	9		SF_R	When High during FS_R, SF_R indicates a Receive Signalling Frame.
9	10		SIG_R	The signalling bit appears at this output after each Receive Signalling Frame.
10	11		SIG_X	Signalling Data Input. This input is inserted in place of LSB of PCM word during signalling frame.
	12		SF_X	When High during FS_X, this input indicates a Long Frame Signalling.
11	13	9	$MCLK_X$	Transmit Master Clock. Must be 1.536 or 1.544 or 2.048MHz. May be asynchronous with $MCLK_R$.
12	14	10	$BCLK_X$	Tramsmit Bit Clock. May vary from 64kHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	Tri-State PCM Data Output.
14	16	12	FS_X	Transmit Frame Sync Pulse. An 8kHz pulse train which enables the PCM word to be shifted out through DX by $BCLK_X$.
15	17	13	$\overline{TSX}$	Open Drain Output. Pulled down during time slot.
16	18	14	GS_X	Analog Output of Transmit Amplifier used to set the gain.
17	19	15	$VFXI^-$	Inverting Input of Transmit Amplifier.
18	20	16	VFXI+	Noninverting Input of Transmit Amplifier.

HARRIS

HC-55536

All-Digital Continuously Variable Slope Delta Demodulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION

APPLICATIONS

- SPEECH SYNTHESIS
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

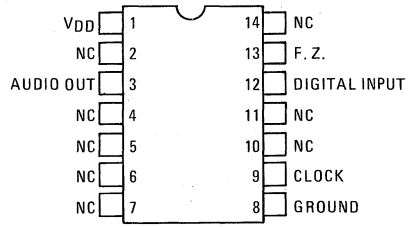
The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the continuously variable slope (CVSD) method.

While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. Internal time constants are optimized for a 16K bit/sec data rate. However, the device is usable from 9K bits/sec to above 64K bits/sec.

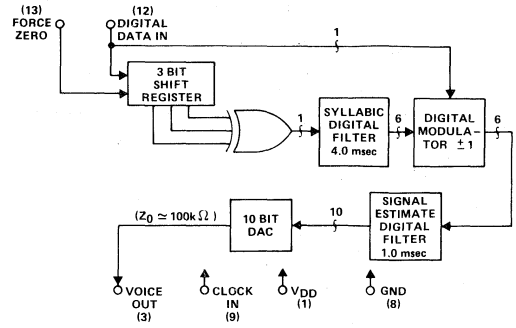
The HC-55536 is available in a 14 pin ceramic DIP package. Chips are available, probe tested at +25°C.

PINOUT AND PIN DESCRIPTION

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin	GND -0.3V to V_{DD} +0.3V	Operating Temperature (-5)	0°C to 75°C
Maximum V_{DD} Voltage	+7.0V		
Minimum V_{DD} Voltage	+3.0V	Storage Temperature Range	-65°C to +150°C
Operating V_{DD} Range	+3.0V to +7.0V		

ELECTRICAL CHARACTERISTICS V_{DD} = +5.0V; Bit Rate = 16K Bits/sec; T_A = +25°C.

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Clock Bit Rate		16	64	K Bits/Sec	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+3.0		+7.0	V	
Supply Current		1.0		mA	
Logic "1" Input, V_{IH}	3.5	4.5		V	(2)
Logic "0" Input , V_{IL}			1.5	V	(2)
Audio Output Voltage		0.5	1.2	V_{RMS}	(3)
Audio Output Impedance		100		kΩ	(4)
Syllabic Filter Time Constant		4.0		ms	(5)
L. P. Filter Time Constant		0.94		ms	(5)
Step Size Ratio		24		dB	(6)
Resolution		0.1		%	(7)
Minimum Step Size		0.2		%	(8)
Slope Overload		Fig. 1		–	(9)
Signal/Noise Ratio	25			dB	
Quieting Pattern Amplitude		10		mV_{p-p}	(10)
Clamping Threshold		0.75		F. S.	(11)

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. As mentioned elsewhere, this output includes a DC bias of VDD/2. Therefore an AC coupling capacitor (min. 4.7 μf) is required unless the output filter also includes this bias (as does the circuit in Fig. 2.)
4. Presents 100 kilohms in series with recovered audio voltage. Zero-signal reference is VDD/2.
5. Note that filter time constants are inversely proportional to clock rate.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels, measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Figure 2.
10. The "quieting" pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
11. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

FIG. 1. Illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering. A suitable filter is illustrated in FIG. 2

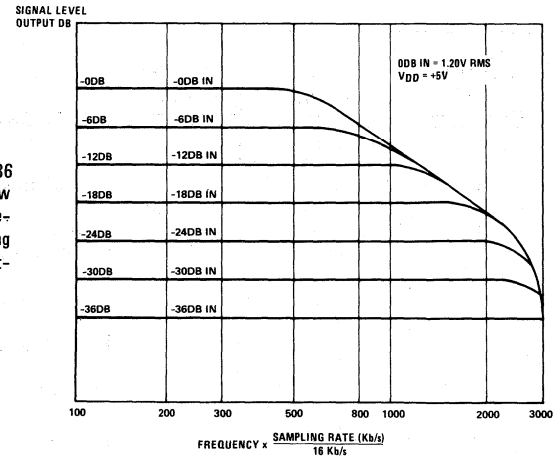
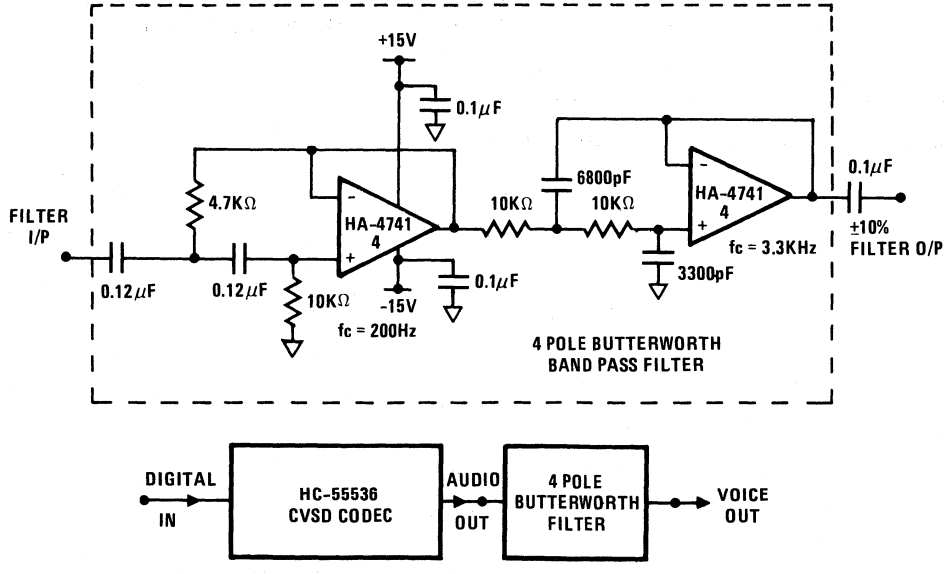


Figure 1 — Transfer Function for CVSD at 16KB

TYPICAL CVSD INPUT AND OUTPUT FILTER



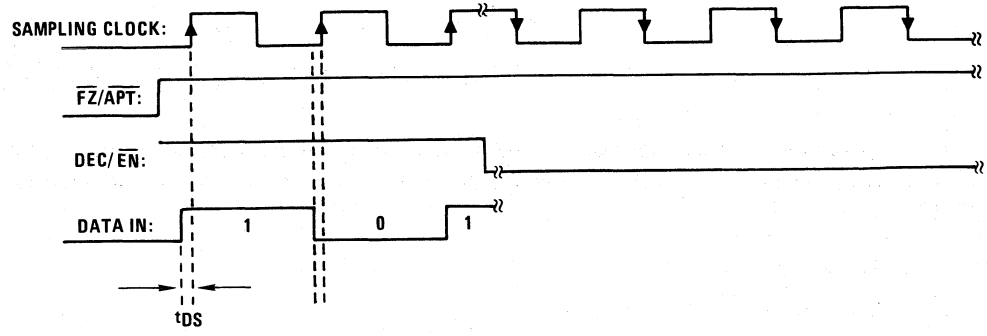
NOTE: The HC-5512C may be useful for this filter application.

Figure 2 — Filtering CVSD Input and Output Signals

PIN ASSIGNMENTS

PIN 14-LEAD D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	N.C.		*No internal connection is made to these pins.
3	Audio Out		Recovered audio out. Presents 100 Kilohm source with DC offset of $V_{DD}/2$.
4	N.C.		*No internal connection is made to these pins.
5	N.C.		*No internal connection is made to these pins.
6,7	N.C.		*No internal connection is made to these pins.
8	Digital Gnd.		Logic ground.
9	Clock		The clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10	N.C.		*No internal connection is made to these pins.
11	N.C.		*No internal connection is made to these pins.
12	Digital In		Input for the received serial NRZ digital data.
13	$\overline{FZ}$	Low	Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	N.C.		

*NOTE: No active input should be left in a "floating condition".



t_{DS}: DATA SET UP TIME, 100ns TYPICAL

Figure 3 – CVSD Timing Diagram

HARRIS

HC-55564

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEW EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 4.5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION UNDER DIGITAL CONTROL
- FILTER RESET UNDER DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS AND SPEECH SYNTHESIS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

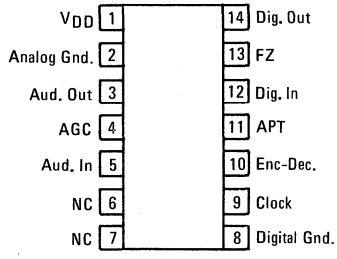
The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

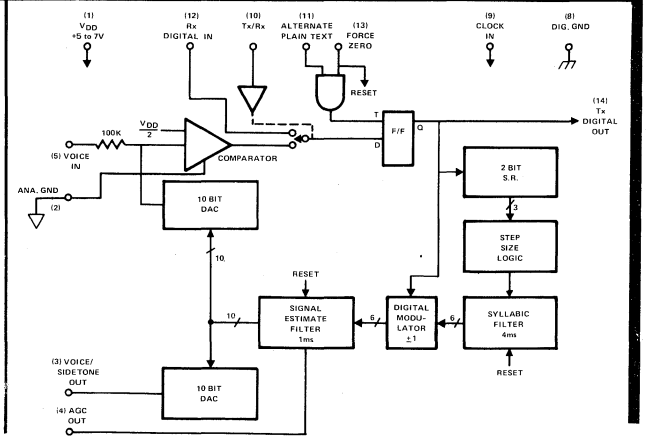
The HC-55564 is usable from 9K bits/sec to above 64K bits/sec. The unit is available in a 14 pin ceramic or plastic DIP package in commercial and military temperature ranges including MIL-STD 883-B processing.

PINOUT

Top View



FUNCTIONAL DIAGRAM



PIN# 14-LEAD D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Analog Gnd.		Ground connection to D/A ladders and comparator.
3	Audio Out		Recovered audio out. May be used as side tone at the transmitter. Presents 100 kilohm source with DC offset of $V_{DD}/2$.
4	$\overline{AGC}$		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	Audio In		Audio input. Should be externally AC coupled. Presents 100 kilohms in series with $V_{DD}/2$.
6,7	N.C.		No internal connection is made to these pins.
8	Digital Gnd.		Logic ground.
9	Clock		The clock must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition.
10	$\overline{Encode}$ (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	$\overline{APT}$	Low	Activating this input causes a digital quieting pattern (alternate plain text) to be transmitted. However internally the CVSD is still functional and a signal is still available at the Audio Out port.
12	Digital In		Input for the received digital data.
13	$\overline{FZ}$	Low	Activating this input resets the internal logic and forces the transmitted output, and the recovered audio output into the "quieting" condition.
14	Digital Out		Output for transmitted digital data.

*NOTE: No active input should be left in a "floating condition".

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	GND -.3V to V_{DD}+0.3V	Operating Temperature (-5)	0°C to +75°C
		(-9)	-40°C to +85°C
Maximum V_{DD} Voltage	+7.0V	(-2)	-55°C to +125°C
		(-8)	-55°C to +125°C
Minimum V_{DD} Voltage	+3.0V		
		Storage Temperature	-65°C to +150°C
Operating V_{DD} Range	+3.0V to +7.0V		

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 5.0V, Sampling Rate = 16Kb/s

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate		16	64	Kb/s	(1)
Supply Current		1.0	3.0	mA	
Logic "1" Input, V_{IH}	3.5			V	(2)
Logic "0" Input, V_{IL}			1.5	V	(2)
Logic "1" Output, V_{OH}	4.0			V	(3)
Logic "0" Output, V_{OL}			0.4	V	(3)
Clock Duty Cycle	30		70	%	
Audio Input Voltage		0.5	1.2	Vrms	(4)
Audio Output Voltage		0.5	1.2	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-2.0		+2.0	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant		0.94		mS	(9)
Resolution		0.1		%	(10)
Min. Step Size		0.2		%	(11)
Signal/Noise Ratio: Audio Input 1.2 V_{RMS} @ 250Hz	25			dB	
Quieting Pattern Amplitude		10		mV P-P	(12)
$\overline{AGC}$ Threshold		0.5		F.S.	(13)
Clamping Threshold		0.75		F.S.	(14)

NOTES

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge. See Figure 3.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive two TTL LS loads.
4. Recommended voice input range for best voice performance.
5. May be used for side-tone in encode mode.
6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.
7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.
8. Unloaded, for linear signals.
9. Note that filter time constants are inversely proportional to clock rate.
10. Minimum quantization voltage level expressed as a percentage of supply voltage.
11. The minimum step size between levels is twice the resolution.
12. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
13. A logic "0" will appear at the $\overline{AGC}$ output pin when the recovered signal reaches one-half of full-scale value (positive or negative).
14. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

FIG. 1. Illustrates the frequency response of the HC-55564 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering. A suitable filter is illustrated in FIG. 2

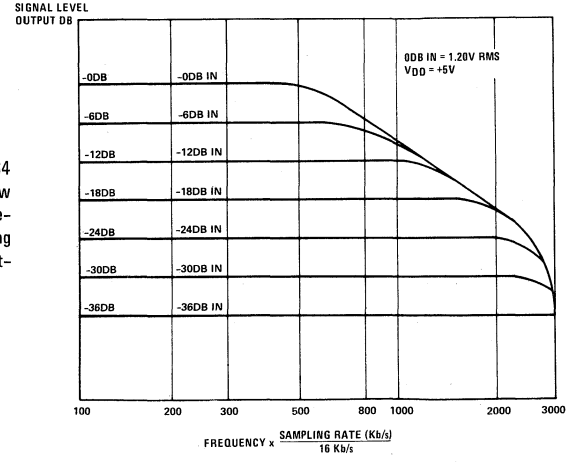
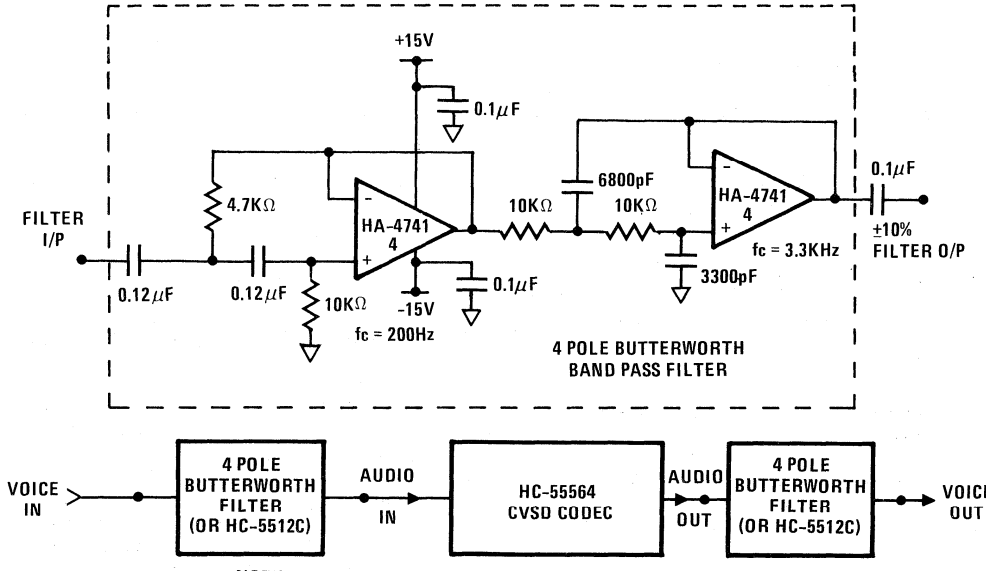


Figure 1 – Transfer Function for CVSD at 16KB

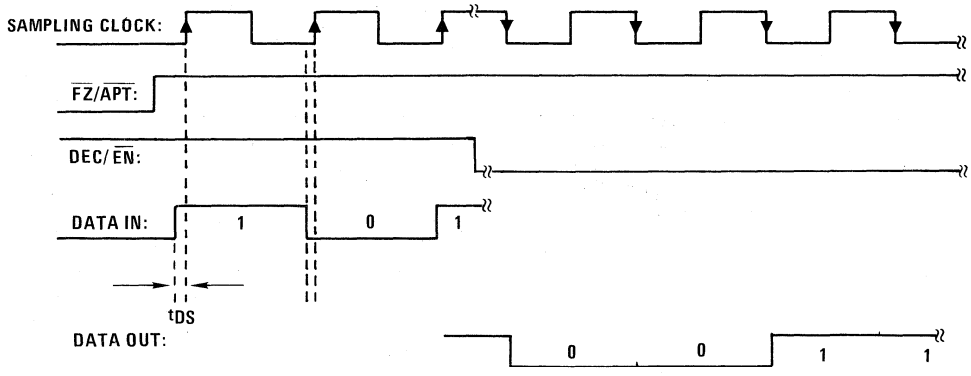
TYPICAL CVSD INPUT AND OUTPUT FILTER



NOTE: The HC-5512C filter is a cost-effective replacement of discrete component filters for this application.

Figure 2 – Filtering CVSD Input and Output Signals

TIMING WAVEFORMS



tDS: DATA SET UP TIME, 100ns TYPICAL

Figure 3 – CVSD Timing Diagram

HARRIS

ADVANCE

HF-10

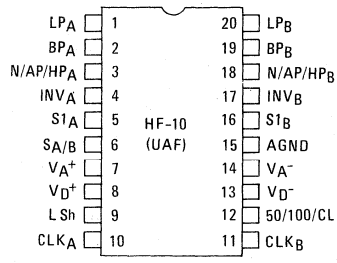
Universal Active Filter

FEATURES

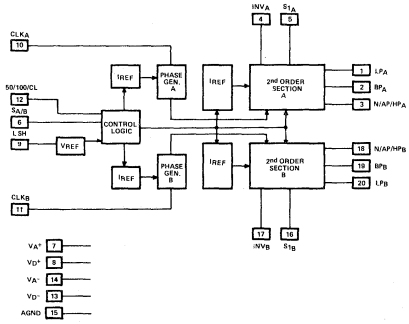
- LOW COST
- 20-PIN 0.3" WIDE DIP
- EASY TO USE
- CLOCK TO CENTER FREQUENCY RATIO ACCURACY ±2%
- FILTER CUTOFF FREQUENCY STABILITY DIRECTLY DEPENDENT ON EXTERNAL CLOCK QUALITY
- SEPARATE HIGHPASS (OR NOTCH OR ALLPASS), BANDPASS, LOWPASS OUTPUTS
- f_0 x Q RANGE UP TO 50 kHz MINIMUM
- OPERATES TO 10 kHz
- SPECIFICATIONS GUARANTEED FOR T_A FROM -55°C to +125°C

PINOUT

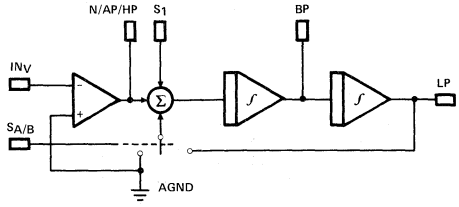
TOP VIEW DIP



SYSTEM BLOCK DIAGRAM



FILTER BLOCK DIAGRAM



DESCRIPTION

The HF-10 consists of two fully independent second order switched capacitor filter sections. Each second order section is a modified state-variable filter. In each section there are three operational amplifiers and an additional "summing node". The extra summing node is a direct benefit of the switched capacitor design approach. This provides increased versatility as compared to the classical continuous-time active filter. The transfer function of each section is tailored by the users choice of feedback configuration, external resistor values, and external clock rate.

The HF-10 topology is very useful since it produces three different, but related, transfer functions simultaneously. Each transfer function has the same pole locations but different zero locations. One of the outputs is either a notch, all-pass, or high-pass signal, depending on the feedback configuration chosen by the user; the other outputs are band-pass and low-pass signals. The center frequency of the complex pole pair, f_0, is determined by the external clock frequency and the state of "50/100/CL" input. This value can also be scaled by a function of the external resistor values, depending on the feedback configuration. The other important filter characteristics, such as gain, Q, etc. are determined by functions of external resistor values. Any of the classical filter configurations (Butterworth, Bessel, Cauer, Chebyshev, etc.) can be realized.

The second order sections can be used separately with the constraint that the clock input for each section be driven by signals of the same level (i.e., either TTL or CMOS logic levels), and that the two clock signals share the same digital ground. If it is desired that a fourth order function be realized, the two sections can be cascaded. The "L Sh" (level shift) input is used in conjunction with the clock inputs to allow compatibility with either TTL or CMOS clock levels.

The HF-10 can be powered-down by connecting the "50/100/CL" input to V_D-. This disables the reference current generators for the operational amplifiers and the clock level shifters.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6.5 Volts	Storage Temperature	150°C
Power Dissipation	300mW	Lead Temperature (Soldering, 10 Sec.)	300°C
Operating Temperature	-55°C to +125°C	Output Loading	$R_{LOAD} \geq 3.5K\Omega$ $C_{LOAD} \leq 25pF$

ELECTRICAL CHARACTERISTICS (COMPLETE FILTER) $\pm 4.5V < V_S < \pm 5.5V$, $-55°C < T_A < +125°C$, Refer to Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_0 X Q< 50 kHz	50		10K	Hz
Clock to Center Frequency Ratio					
$f_{CLK}/f_0 = 50$	Pin 12 = V_D^+, Q = 10 f_0 XQ< 50kHz			±2%	
$f_{CLK}/f_0 = 100$	Pin 12 = AGND, Q = 10 f_0 XQ< 50kHz			±2%	
Q Range	f_0 XQ< 50kHz	0.5		100	
Q Accuracy (Q Deviation from An Ideal Continuous Filter)					
$f_{CLK}/f_0 = 50$	Pin 12 = V_D^+, f_0< 5kHz f_0 XQ< 50kHz			±4%	
$f_{CLK}/f_0 = 100$	Pin 12 = AGND, f_0< 5kHz f_0 XQ< 50kHz			±3%	
f_0 -Q Product		50K			Hz
f_0 Temperature Coefficient					
$f_{CLK}/f_0 = 50$	Pin 12 = V_D^+, f_0 XQ< 50kHz External Clock Temperature Independent			±100	ppm/°C
$f_{CLK}/f_0 = 100$	Pin 12 = AGND, f_0 XQ< 50kHz External Clock Temperature Independent			±100	ppm/°C
Q Temperature Coefficient	f_0 XQ< 50kHz, Q Settling Resistors Temperature Independent			±500	ppm/°C
DC Low-Pass Gain Accuracy	$R_1 = R_2 = 10K\Omega$			±0.2	dB
Crosstalk	INV_A = 0dBm @ 1kHz INV_B = 0V		-50		dB
Clock Feedthrough				10	mV
Maximum Clock Frequency				1.024	MHz
Power Supply Current			8	13	mA
Standby Current	Pin 12 = V_A^-				

ELECTRICAL CHARACTERISTICS (INTERNAL OPERATIONAL AMPLIFIERS)

$\pm 4.5V < V_S < \pm 5.5V$, $-55°C < T_A < +125°C$, Refer to Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Swing (Pins 1,2, 3, 18, 19, 20)	R_{LOAD} = 3.5KΩ	±3.5			V
DC Gain					
R_{LOAD} = 3.5KΩ		80			dB
UNLOADED		110			dB
Output Short Circuit Current					
SOURCE			3		mA
SINK			1.5		mA
Op Amp Gain-BW Product		2.5	3.8		MHz
Op Amp Slew Rate			15		V/μs
Power Supply Rejection Ratio (PSRR)	DC Only	40			dB

PIN ASSIGNMENTS

SYMBOL	DESCRIPTION
LP, BP, N/ AP/HP	These are the low-pass, band-pass, notch or all-pass or high-pass outputs of each second order section. These pins have static discharge protection.
INV	This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.
S1	S1 is a signal input pin used in the allpass filter configurations. The pin has a static discharge protection.
$S_{A/B}$	It activates a switch connecting one of the inputs of the filter's second summer either to analog ground ($S_{A/B}$ low to V_A^-) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A^+). This allows flexibility in the various modes of operation of the I.C. $S_{A/B}$ is protected against static discharge.
V_A^+, V_D^+	Analog positive supply and digital positive supply. These pins are internally connected through the I.C. substrate and therefore, V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
V_A^-, V_D^-	Analog and digital negative supply respectively. The same comments for V_A^+, V_D^+ apply here.
L Sh	Level shift pin; it accomodates various clock levels with dual or single supply operation. With dual ±5V supplies, the HF-10 can be driven with CMOS clock levels (±5V) and the "L Sh" pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used and TTL clock levels, derived from 0V to 5V supply, are used, the "L Sh" pin should be tied to the system ground. For single supply operation (0V and 10V); the V_D^- and V_A^- pins should be connected to the system ground, the AGND pin should be biased at 5V, and the "L Sh" pin should also be tied to the system ground. This will accomodate both CMOS and TTL clock levels. The "L Sh" pin is protected against static discharge.
CLK (A or B)	Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (L Sh) pin description discusses how to accomodate their levels. The duty cycle of the clock should preferably be close to 50%, especially when clock frequencies above 200kHz are used. This allows the maximum time for the op amps to settle, yielding optimum filter operation. These pins are protected against static discharge.
50/100/CL	By tying the pin to V_D^+, a 50:1 clock to filter center frequency operation is obtained. Tying the pin at mid-supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When the pin is tied to V_D^-, a simple current limiting circuit is triggered to limit the overall supply current. The filtering action is then aborted. The 50/100/CL pin is protected against static discharge.
AGND	Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid-supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin, so a "clean" ground is mandatory. The AGND pin is protected against static discharge.

TYPICAL FILTER CONFIGURATION

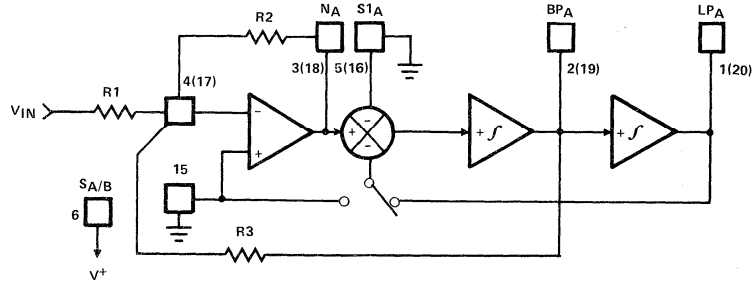


Figure 1

ANALOG

Quality & Reliability

9

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Harris Quality and Reliability

Harris Takes the Total Approach to Quality

Quality and reliability do not occur by accident in microcircuit manufacturing. They can be achieved only as a result of precise design, capable manufacturing methods, carefully controlled production processes and accurate screening and testing. Quality and reliability must be totally designed and built into the product. They are not characteristics that can be added after manufacture. They must be part and parcel of the flow from the original design through final assembly and test.

The major steps affecting microcircuit reliability and quality are:

- Initial circuit selection and design.
- Selection of package materials and design.
- Die layout and geometry.
- Raw material inspection and QC.
- Wafer/die production process and controls.
- Die/package assembly and controls.
- Screening and test procedures.

Harris Standard Flows

Harris Semiconductor offers a variety of standard product flows which cover the myriad of application environments our customers experience. These flows run the gambet of low cost commercial parts to fully qualified JAN microcircuits. All of these grades have one thing in common. They result from meticulous attention to quality, starting with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers. The standard flows offered are:

Dash 5 – Electrical performance guaranteed from 0°C to +75°C.

Dash 7 – Dash 5 plus 96 hours of burn-in to reduce infant mortality risk in customer applications.

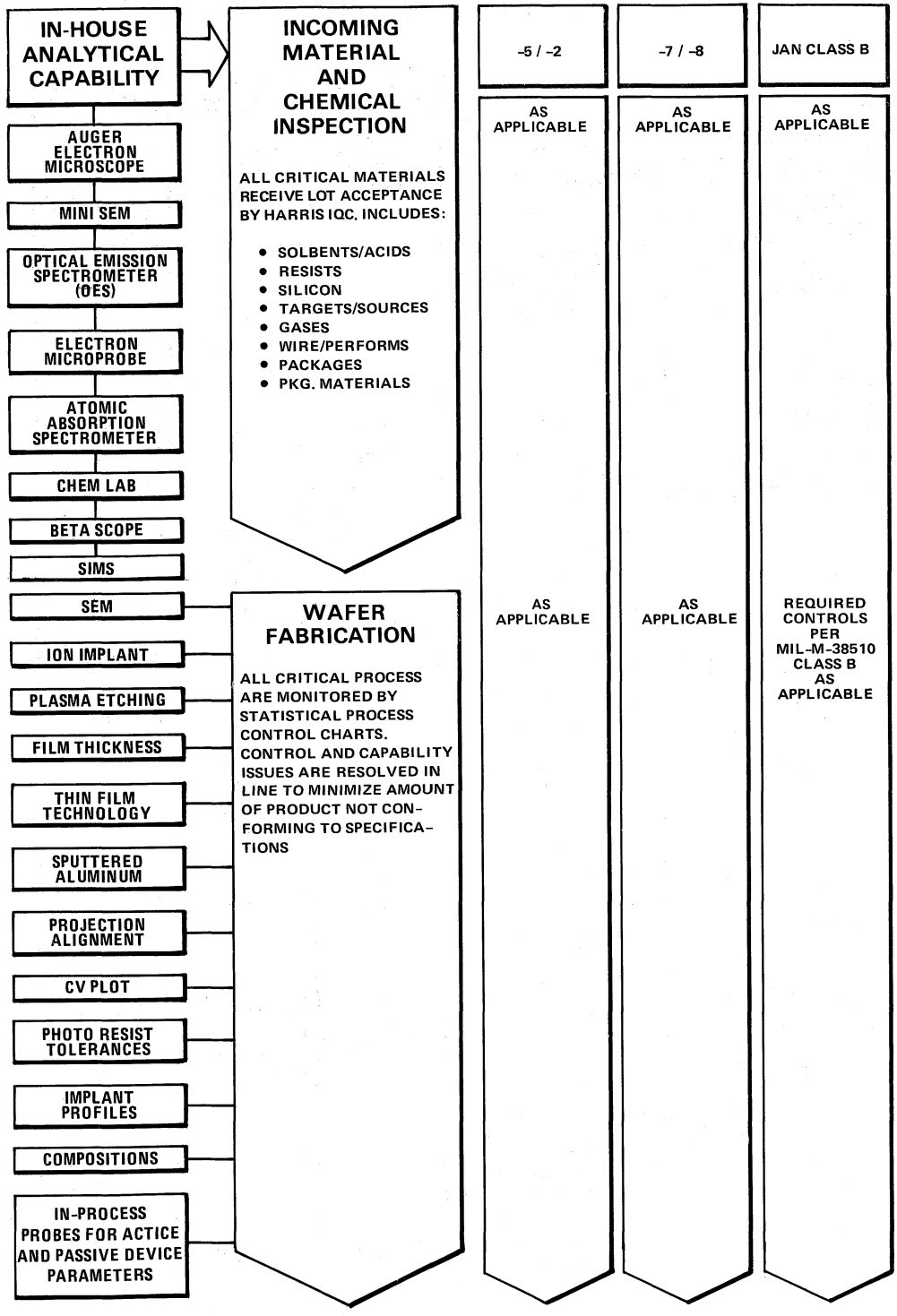
Dash 2 – Electrical performance guaranteed from -55°C to +125°C.

Dash 8 – Electrical performance guaranteed from -55°C to +125°C plus 160 hours of burn-in with PDA of 5%. 100% preseal visual per Mil Std 883C Method 2010.

JAN
Class B – Fully qualified and certified microcircuit manufactured per Mil M 38510 requirements.

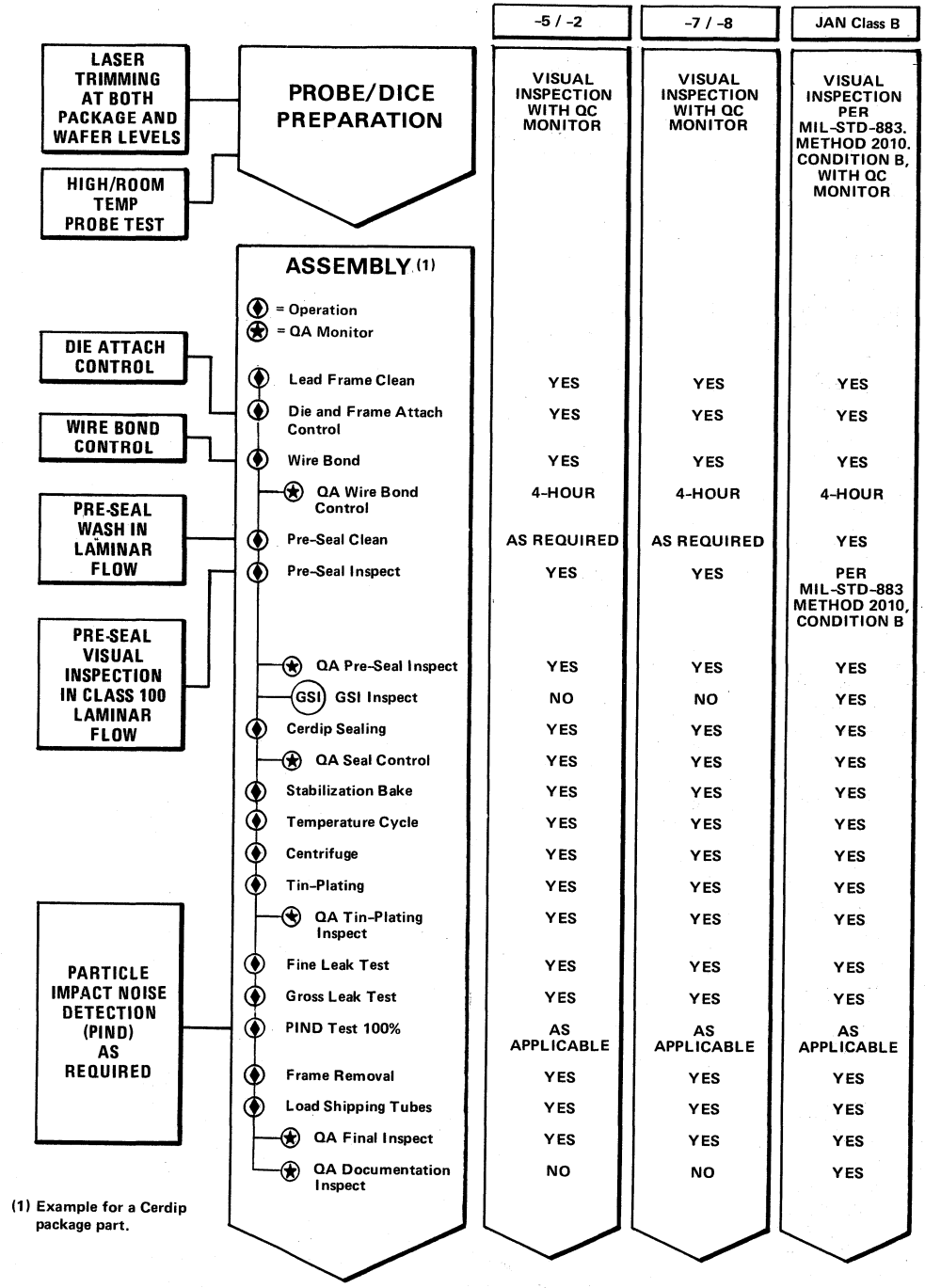
Details of the individual process requirements are contained in the flow charts which follow.

Harris Semiconductor Standard Processing Flows



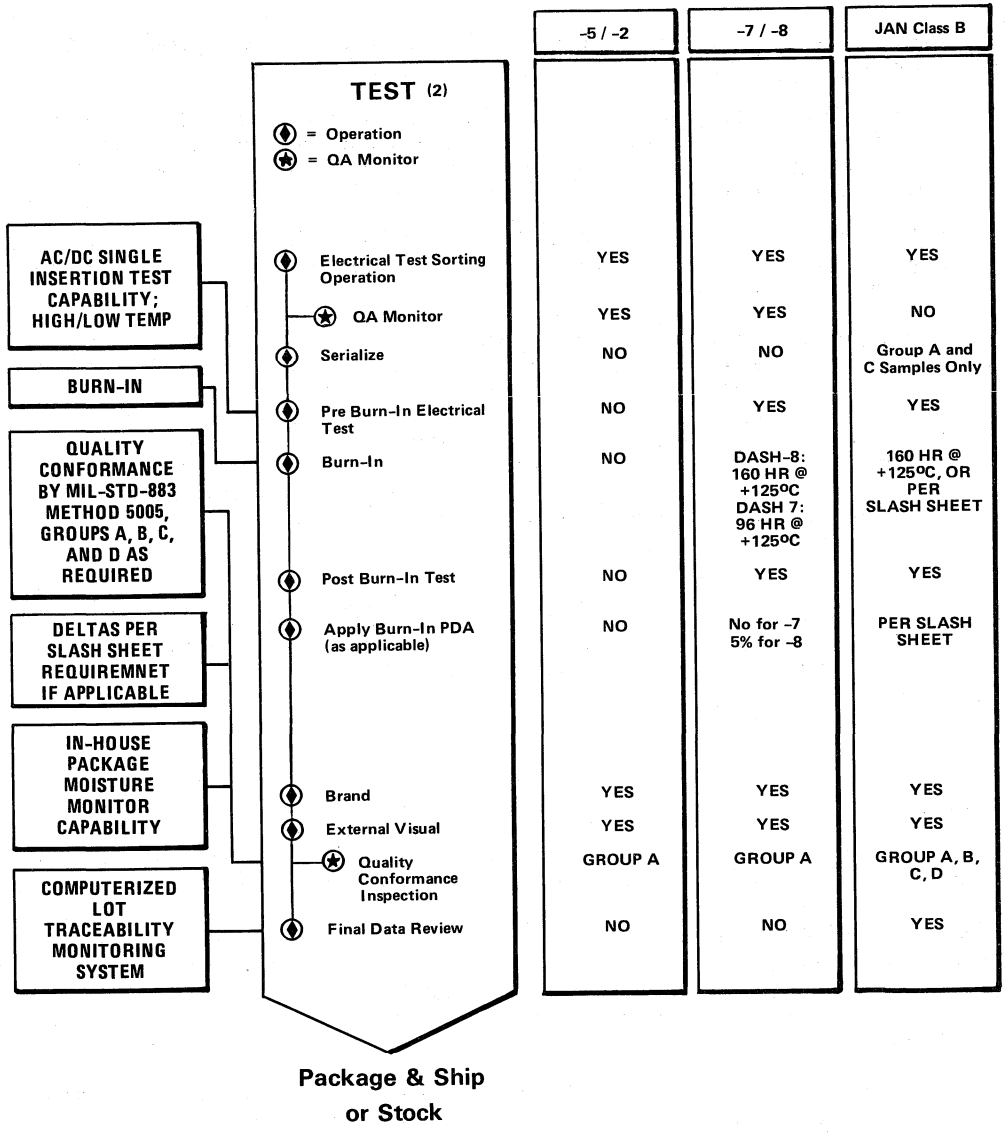
(1) T_A = -55°C to +125°C for all grades except DASH-7 (DASH-7 T_A = 0°C to +75°C)

Harris Semiconductor Standard Processing Flows (continued)



(1) Example for a Cerdip package part.

Harris Semiconductor Standard Processing Flows (continued)



(2) -5 / -7 0°C to +75°C
-2 / -8 / JAN -55°C to +125°C

Advantages of Standard Flows

Wherever feasible, and in accordance with good value engineering practice, the IC user should specify device grades based on one of the five standard Harris manufacturing flows. These are more than adequate for the overwhelming majority of applications and may be utilized quite effectively if the user engineer bases his designs on the standard data book or slash sheet (as applicable) electrical limits.

Some of the more important advantages gained by using standard as opposed to custom flows are as follows:

- Lower cost than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling, and added documentation.
- Faster delivery. The manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- Increased confidence in the devices. A continuing flow of a given product permits the manufacturer to monitor trends which may bear on end-product performance or reliability and to implement corrective action, if necessary.
- Reduction of risk. Since each product is processed independent of specific customer orders, the manufacturer absorbs production variability within its scheduling framework without major impact on deliveries. In a custom flow, a lot failure late in the production cycle can result in significant delays in delivery due to the required recycling time.

Despite the advantages of using standard flows, there are cases where a special or custom flow is mandatory to meet design or other requirements. In such cases, the Harris Marketing groups stand ready to discuss individual customer needs and, where indicated, to accomodate appropriate custom flows.

Quality Beginning to End

There are several significant elements which comprise Harris Semiconductor's approach to quality that don't show on a process flow chart. Some of these are as follows:

INITIAL CIRCUIT SELECTION AND DESIGN

Once operational characteristics and parameter limits have been defined there are many different circuit configurations capable of conforming to them. Harris designers are tasked to choose those which are capable of meeting the required performance specifications with maximum reliability.

Powerful computer aided design (CAD) techniques are applied in developing the original concepts and detailed schematics, with computer modeled circuit simulation used to corroborate projected product performance. Monte Carlo methods, and other simulation techniques are also used, as appropriate to achieve specific objectives.

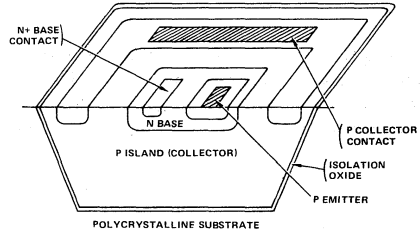
Regardless of the circuit approach selected, high reliability, top performance, and maximum potential yield to the required specifications are the governing criteria.

Individual active device types and component values are selected to provide optimum circuit performance and to minimize sensitivity to parametric changes which may occur with aging or as a result of environmental conditions.

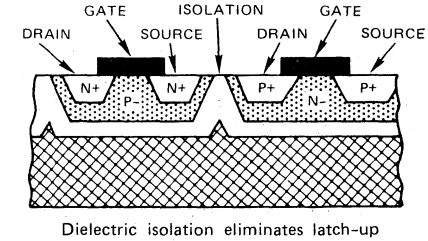
Since most Harris products are sold into military, industrial and commercial end use applications most circuits are designed to meet military temperature range requirements at the outset. This results in more capable products introduced to all segments of the marketplace.

Die Layout and Geometry

Conformance with good layout practice is a must, for consistently reliable devices cannot be assembled from poorly designed chips. Therefore, the IC layout phase at Harris is controlled by ground rules which establish the "do's" and "don'ts" for each manufacturing process. These rules define dimensions and toleranced to insure product immunity to process variations, while maximizing product reliability under worst-case stress conditions. Computerized ground rule software packages are used by the chip designers to assure dimensional adherence of diffusion windows as well as interconnect width and spacing. Automatic checkout procedures confirm that the product conforms to the established ground rules.



Cross-sectional view of high-frequency PNP device formation in the DI process.



Dielectric isolation eliminates latch-up by placing a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

Raw Material Inspection and QC

Acknowledging that Hi-Rel, high performance devices can be manufactured only by using top quality materials, Harris subjects incoming materials, piece parts and supplies to documented tests and inspections. The techniques used are selected for optimum evaluation of the materials checked to ensure full compliance with Harris internal specifications. Close coordination with the suppliers is maintained to assure a reliable supply of quality materials.

Wafer Die Production Process and Controls

Harris has a wide range of state-of-the-art wafer and die processing capabilities, permitting the circuit designer to choose the optimum production technique for each type of device.

Depending on specific design and performance specifications, devices, may be fabricated using either conventional or complementary bipolar, CMOS, combined bipolar and CMOS, NMOS or PMOS construction. Two complementary vertical bipolar processes are available, offering frequency responses two orders of magnitude higher than conventional fabrication techniques.

Regardless of the process involved, statistical process control charts are employed to maximize the visibility of wafer lot variability during production. These charts take the form of $\overline{X}/R$ charts for variables data and $\overline{C}/\overline{p}$ charts for attributes data. Typical process control points include diffusion, thin film, photo resist steps as well as inspection points or electrical device measurements. The goal of the control charts is three fold:

- Isolate and eliminate special causes of variability to preclude the production of wafers with a process which is not operating correctly.
- Define the natural limits of variability in a process to determine its capability in light of engineering expectation.
- Provide a reference baseline for process enhancements or changes to improve capability or reduce cost.

With high reliability an integral part of its manufacturing philosphy, Harris Semiconductor does not have separate production lines for standard and JAN devices. Rather, all Harris devices of a given type are manufactured on the same line. Product grades are selected by the application of screening tests and inspection from the same generic process flows in wafer fab.

Die/Package Assembly and Controls

Each major process operation (mount, bond, seal, trim) is carefully monitored by in-process quality control steps. In addition, many mechanical and environmental tests are implemented during the die/package assembly stage. The specific controls and tests utilized at each step are in strict compliance with the applicable standards for the device reliability class designation.

Burn-In

100% burn-in is a screening procedure used when applicable to detect devices subject to infant mortality failure modes. Biases are applied to simulate worst-case operational conditions, permitting the identification and elimination of marginal units.

The applied voltage levels, operational state, temperature and test period vary with the type of device and reliability class, as governed by the applicable standards. Electrical test of the device is performed both prior to and after the burn-in period.

Electrical Screening and Test Procedures

While many factors are critical in the production of I. C. devices, the electrical screening and test procedures, are critical to matching product performance to customer need. All products receive 100% electrical test per the data sheet requirements for each product type. In addition product lots received a battery of QA inspections and tests to assure compliance with Harris production standards.

Reliability Assessment and Enhancement

At Harris, realibility assurance is a dynamic program with the primary and ultimate goal of securing full product performance throughout its usage life. Each manufacturing phase from original design to final packaging is subject to continuous review, analysis, and evaluation, with modifications introduced as needed to improve product performance and reliability. There are three important sources of reliability data:

1. Initial qualification
2. Add on life
3. Field failure history

New Products/Processes/Packages

Two requirements are imposed on the product development phase of new circuits and processes. First is the use of proper process methodology, design techniques, and layout practices. New designs are reviewed throughout the course of their development for conformance to the constraints defined by process ground rules. These rules document the results of years of experimentation and experience and reflect a relatively conservative approach to process capability and technology. Second is demonstration of reliability performance of a new product or process through a series of stress tests designed to accelerate typical failure mechanisms in integrated circuits. Qualification requirements are illustrated in Table I for a variety of product/process/package maturity conditions. These tests are executed by the Harris Reliability organization for each new product/package/process before circuits are committed to the marketplace. Failure rate predictions are made based on test results. More importantly, failure analysis results are fed back into design and process engineering organizations to generate corrective action (if applicable) and enhance product performance. Each new product entry must meet minimum failure rate standards to qualify for sale to customers.

"Add On"

An important source of reliability information is performance of established products through extended life testing under worst-case operating conditions. Failure rate predictions for specific products or product types are available on request via Harris Semiconductor Reliability bulletins;

Accelerated life test are utilized to estimate the expected field failure rate of our products. Life tests are conducted periodically on regular production samples. Sample sizes are typically 200 units which are operated at 125°C at nominal supply voltages and with forcing and loading conditions simulating typical application environments. Where possible, operating conditions are structured to provide maximum thermal and electrical acceleration of the natural failure mechanisms found in I. C. devices.

All rejected devices are carefully analyzed and activation energies are assigned based on the observed failure mechanisms. There rates are then computed based on thermal derating factors per the Arrhenius equation. The results are reported in the Harris Reliability bulletins based on derating to +55°C operations and nominal supply conditions. Failure rates are reported at the 60% confidence level and the 95% confidence level.

Finally, life tests are monitored at mid-point intervals to assure that failure rates are decreasing and that no wearout mechanisms are at work.

TABLE 1. TEST MATRIX

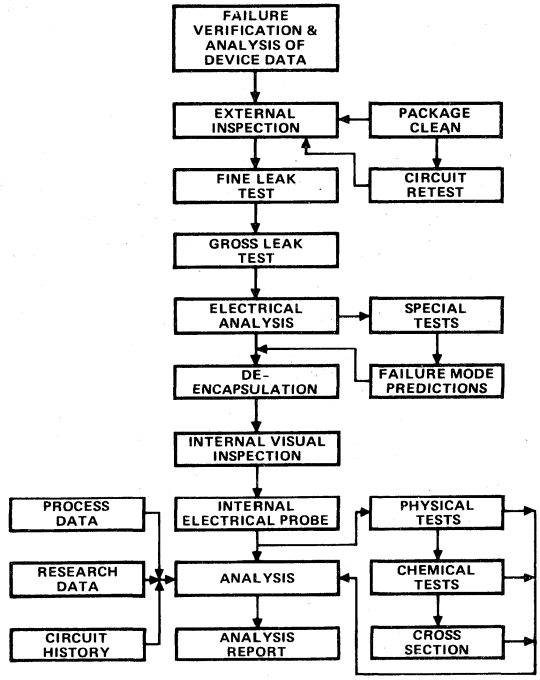
Design Package Process	New New New	New New Est.	New Exist New	New Exist Est.	Exist New New	Exist New Est.	Exist Exist New	Exist Exist Est.
Abuse Tests 20 Units	X	X	X	X	X		X	X
Max. Ratings 20 Units: No Failures	X		X	X	X		X	X
86/86 or Autoclave 50 Units: No Failures	X	X	X		X	X	X	
Constr. Analysis 5 Units: No Failures	X	X	X	X	X	X	X	X
Centrifuge 50 Units: No Failures	X	X			X	X		
Ele. Charac. 20 Units: No Failures	X	X	X	X	X		X	X
ESD Immunity 20 Units: No Failures	X	X	X	X	X		X	X
Fig. Test 20 Units: No Failures	X	X	X	X	X		X	
HTOL Sample Groups	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)
Latch-up 20 Units: No Failures	X	X	X	X	X			
Lead Integrity 20 Units: No Failures	X	X			X	X	X	X
Mech. Charac. 20 Units: No Failures	X	X			X	X		
Mech. Schock 50 Units: No Failures	X	X			X	X		
Moisture Resist 50 Units: No Failures	X	X			X	X		
θja/θjc 20 Units	X	X			X	X		
Solvent Resistance 4 Units: No Failures	X	X			X	X		
Solderability 20 Units: No Failures	X	X			X	X		
Temperature Cycling 50 Units: No Failures	X	X			X	X		
Thermal Shock 50 Units: No Failures	X	X			X	X		
Vibration 50 Units: No Failures	X	X			X	X		

Field Failures

The final source of continued reliability assessment and enhancements is the analysis of defects on products returned by our customer.

An exhaustive analysis of device failures is a requirement of the Harris reliability program. After failure confirmation by electrical test, the device is processed through the standard failure analysis procedure outlined below.

FAILURE ANALYSIS FLOW



Harris and the JAN Program

Harris Semiconductor became an active participant in the JAN program as the first microcircuit manufacturer to JAN-qualify a PROM, receiving a QPL-2 qualification in 1972 and the higher level QPL-1 qualification in 1974 for the military version of the HPROM-0512, as defined by MIL-M-38510, Slash Sheet 201. Since this initial effort, Harris has received JAN line certification for generic HM-76XX PROM family. In early 1980, Harris received JAN certification for additional production lines supplying dielectrically isolated (DI) operational amplifiers, analog switches, analog multiplexers, and junction isolated op amps.

Harris will continue to pursue further line certification and part qualification efforts, offering users an ever-expanding line for JAN-qualified devices.

JAN - Qualified Devices

TYPE	FUNCTION	MIL-M-38510/	QPL-2
HA2-2600	High Performance Operational Amplifier	12202BGC	Now Qualified
HA2-2620	Very Wide Band, Uncompensated Op Amp	12203BGC	Now Qualified
HA2-2500	Precision High Slew Rate Op Amp	12204BGC	Now Qualified
HA2-2510	High Slew Rate Op Amp	12205BGC	Now Qualified
HA2-2520	High Slew Rate Uncompensated Op Amp	12206BGC	Now Qualified
HA1-4741	Quad Operational Amp	11003BCB	Now Qualified

Burn-In Circuit Index

		DRAWING NUMBER
HA-OP07	Precision Operational Amplifier	22
HA-1608	+10V Adjustable Voltage Reference	1
HA-2400/04/05	PRAM, Four Channel Operational Amplifiers	2
HA-2420/25	Fast Sample and Hold Operational Amplifiers	3
HA-2420 (LCC)	Fast Sample and Hold Operational Amplifiers	4
HA-2500/02/05	Precision High Slew Rate Operational Amplifiers	5
HA-2510/12/15	High Slew Rate Operational Amplifiers	5
HA-2520/22/25	Uncompensated High Slew Rate Operational Amplifiers	5
HA-2539	Very High Slew Rate Wideband Operational Amplifiers	6
HA-2540	Wideband, Fast Settling Operational Amplifiers	7
HA-2600/02/05	Wideband, High Impedance Operational Amplifiers	5
HA-2620/22/25	Very Wideband, Uncompensated Operational Amplifiers	5
HA-2630/35	High Performance Current Booster	8
HA-2640/45	High Voltage Operational Amplifiers	9
HA-2650/55	Dual High Performance Operational Amplifiers	10, 11
HA-2720/25	Wide Range Programmable Operational Amplifiers	12
HA-2730/35	Wide Range Dual Programmable Operational Amplifiers	13
HA-2740	Quad Programmable Operational Amplifiers	14
HA-4600/02/05	High Performance Quad Operational Amplifiers	15
HA-4620/22/25	Wideband, High Performance Quad Operational Amplifiers	16
HA-4640	High Temperature Quad Operational Amplifier	15
HA-4741	Quad Operational Amplifier	15
HA-4900/02/05	Precision Quad Comparators	17
HA-5033	Video Buffer	18
HA-5062	Low Power, JFET Input Operational Amplifier	11, 19
HA-5064	Low Power, JFET Input Quad Operational Amplifier	15
HA-5082	JFET Input Operational Amplifier	11, 19
HA-5084	JFET Input Quad Operational Amplifier	15
HA-5100/05	Wideband, JFET Input Operational Amplifiers	20
HA-5102	Low Noise, High Performance Operational Amplifiers	11, 19
HA-5104	Low Noise, High Performance Operational Amplifiers	15
HA-5110/15	Wideband, JFET Input, Uncompensated Operational Amplifiers	20
HA-5112	Low Noise, High Performance Operational Amplifiers	21
HA-5114	Low Noise, High Performance Operational Amplifiers	16
HA-5130/35	Precision Operational Amplifiers	22
HA-5141	Ultra-Low Operational Amplifier	22
HA-5142	Ultra-Low Power Operational Amplifier	11, 19
HA-5144	Ultra-Low Power Operational Amplifier	15
HA-5160/62	Wideband, JFET Input, High Slew Rate, Uncompensated Operational Amplifiers	23
HA-5170	Precision JFET Input Operational Amplifier	22
HA-5180	Low Bias Current, Low Power JFET Input Operational Amplifier	22
HA-5190/95	Wideband, Fast Settling Operational Amplifiers	7, 24
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier	25
HA-23551	Triple Current Sense Latch	26
HC-5502	SLIC-LC Subscriber Line Interface Circuit	27
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HC-5504	SLIC-LC Subscriber Line Interface Circuit	28
HC-5512/HC-5512A	PCM Monolithic Filter	29
HC-5512C	PCM or CVSD Monolithic Filter	29
HC-55564	All-Digital Continuously Variable Slope Delta Demodulator (CVSD)	30
HI-200	Dual SPST CMOS Analog Switch	31, 32
HI-201	Quad SPST CMOS Analog Switch	33
HI-201HS	High Speed Quad SPST CMOS Analog Switch	33
HI-300	Dual SPST CMOS Analog Switch	34
HI-301	SPDT CMOS Analog Switch	34
HI-302	Dual DPST CMOS Analog Switch	34
HI-303	Dual SPDT CMOS Analog Switch	35
HI-304	Dual SPST CMOS Analog Switch	35
HI-305	SPDT CMOS Analog Switch	35

Burn-In Circuit Index (Continued)

		DRAWING NUMBER
HI-306	Dual DPST CMOS Analog Switch	35
HI-307	Dual SPDT CMOS Analog Switch	35
HI-381	Dual SPST CMOS Analog Switch	36
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HI-387	SPDT CMOS Analog Switch	36
HI-390	Dual SPDT CMOS Analog Switch	37
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers	38
HI-506A/507A	16 Channel CMOS Analog Multiplexers with Overvoltage Protection	38
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HI-506A/507A (LCC)	16 Channel CMOS Analog Multiplexers with Overvoltage Protection	39
HI-506L/507L	Single 16/Differential 8 Channel CMOS Analog Multiplexers with Latches and Overvoltage Protection	40
HI-508/508A	8 Channel Single-Ended Multiplexer	41
HI-508/508A (LCC)	8 Channel Single-Ended Multiplexer	42
HI-508L/509L	Single 8/Differential 4 Channel CMOS Analog Multiplexers with Latches and Overvoltage Protection	43
HI-509/509A	4 Channel Differential Multiplexers	44
HI-509/509A (LCC)	4 Channel Differential Multiplexers	45
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	46
HI-516 (LCC)	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	47
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	48
HI-524	4 Channel Video Multiplexer	49
HI-539	Monolithic, Four Channel, Low Level, Differential Multiplexer	44
HI-562A	12 Bit High Speed Monolithic Digital-to-Analog Converter	50
HI-562A (LCC)	12 Bit High Speed Monolithic Digital-to-Analog Converter	51
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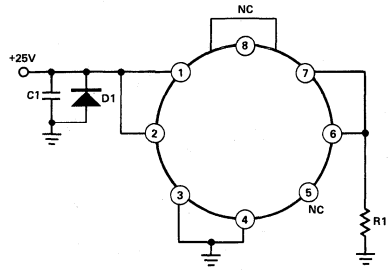
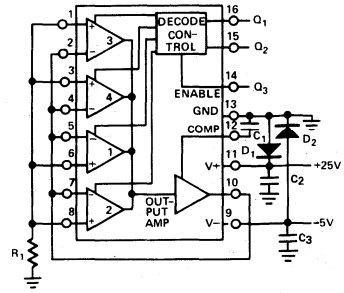
1 HA-1608



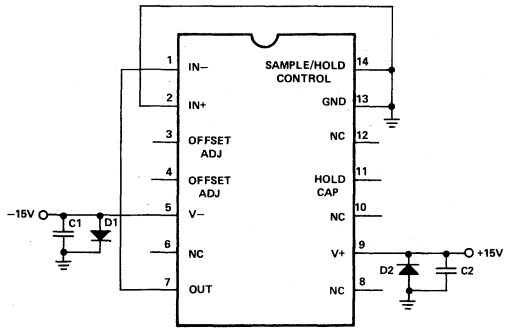
NOTES:
$R_1 = 1K\Omega$
$C_1 = 0.01\ \mu F$
$D_1 = IN4002$

2 HA-2400/04/05



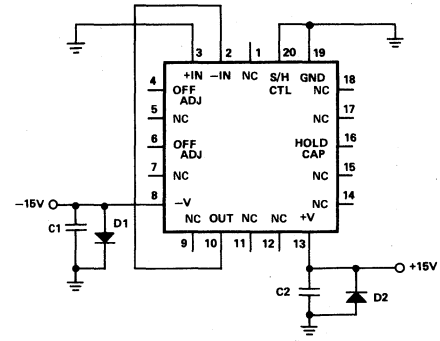
NOTES:
TA = +125°C
R1 = 100kΩ
C1 = 910pF, 50V
D1, D2 = IN4002
C2 = C3 = 0.1 μF
Freq., Q1 = 100kHz, Q2 = 50kHz, Q3 = 25kHz

3 HA-2420/25



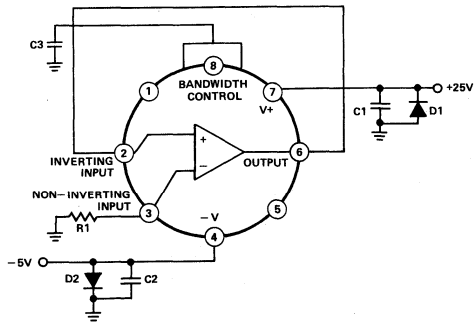
NOTES:
C1, C2 = .01 μF
D1, D2 = IN4002

4 HA-2420 (LCC)



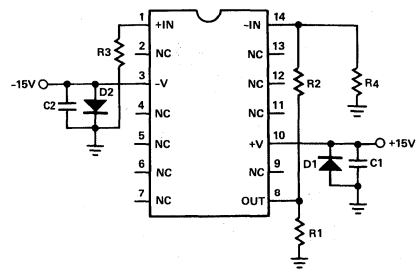
NOTES:
C1, C2 = .01 μF
D1, D2 = IN4002

5 HA-2500/02/05, HA-2510/12/15, HA-2520/22/25, HA-2600/02/05, HA-2620/22/25, LM 118/318



NOTES:
R1 = 1MΩ, ±5%, ¼ or ½ Watt
C1 = C2 = C3 = 0.01 μF
D1 = D2 = IN4002

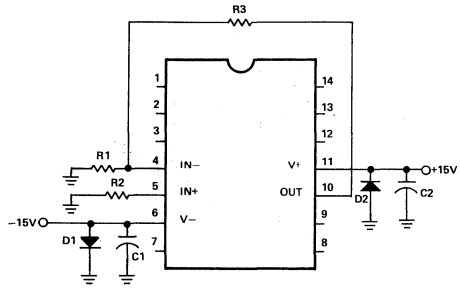
6 HA-2539



NOTES:
R1 = R3 = 1kΩ, ±5%
R2 = 10kΩ, ±5%
C1 = C2 = 0.01 μF (One per socket)
D1 = D2 = IN4002 (one per board)
R4 = 2KΩ

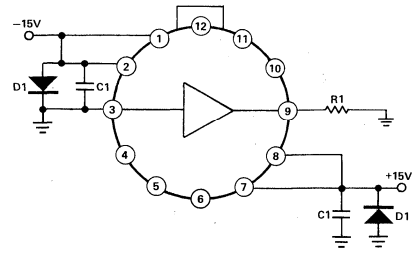
9 QUALITY & RELIABILITY

7 HA-2540, HA-5190/95



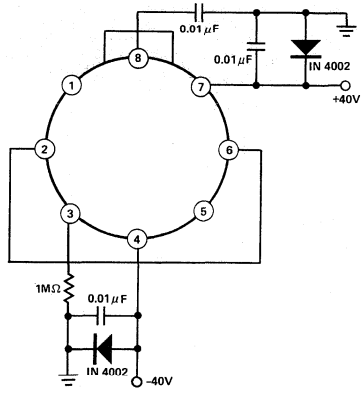
NOTES:
R1, R2: 1KΩ, ¼ or ½ Watt, 5%
R3: 10kΩ, ¼ or ½ Watt, 5%
C1, C2: 0.1μF
D1, D2: IN4002

8 HA-2630/35

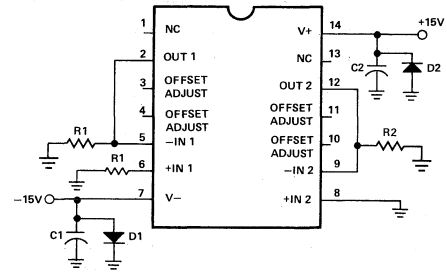


NOTES:
R1 = 2kΩ
C1 = 0.01 μF
D1 = IN4002

9 HA-2640/45, LM-143/343

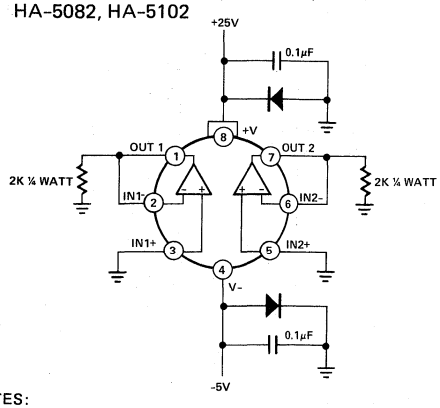


10 HA-2650/55



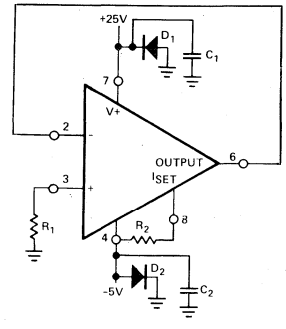
NOTES:
R1, R2: 2KΩ, ¼ or½ Watt, 5%
C1, C2: 0.1 μF
D1, D2: IN4002

11 HA-2650/55, HA-5142, HA-5062, HA-5082, HA-5102



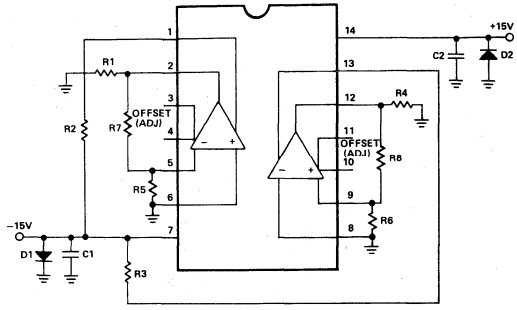
NOTES:
Resistors = 2kΩ, ±10%, ¼ Watt
Capacitors = 0.01 to 0.1 μF, Nonelectrolytic

12 HA-2720/25



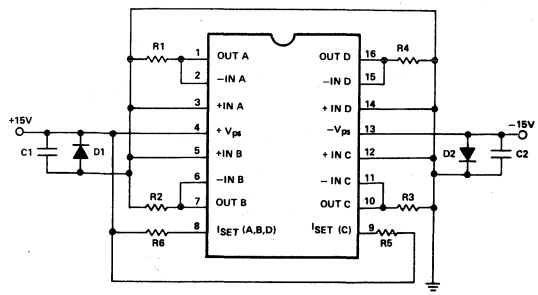
NOTES:
TA = +125°C
C1, C2 = 0.01 to 0.1 μF
R1 = 1MΩ, R2 = 2MΩ

13 HA-2730/35



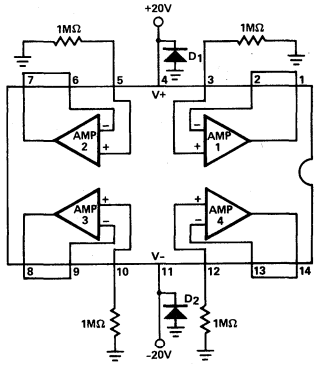
NOTES:
R1 + R4 = 5kΩ
R2 + R3 = 2M
C1 + C2 = .01 to .1 μF
D1 + D2 = IN4002 or Similar
R7, R8 = 10KΩ
R5, R6 = 1KΩ

14 HA-2740



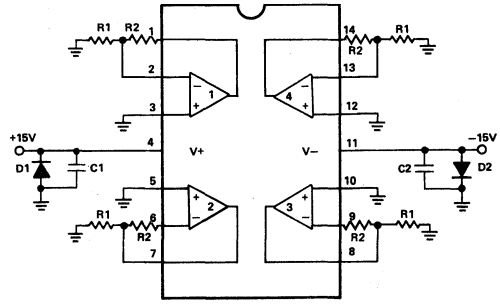
NOTES:
C1, C2 = 0.01 μF
D1, D2 = IN4002
R1, R2, R3, R4 = 2kΩ, ½ or ¼ Watt, 5%
R5, R6 = 2MΩ, ½ or ¼ Watt, 5%

15 HA-4600/02/05, HA-4640, HA-4741, HA-5064, HA-5084, HA-5104, HA-5144, LF 147



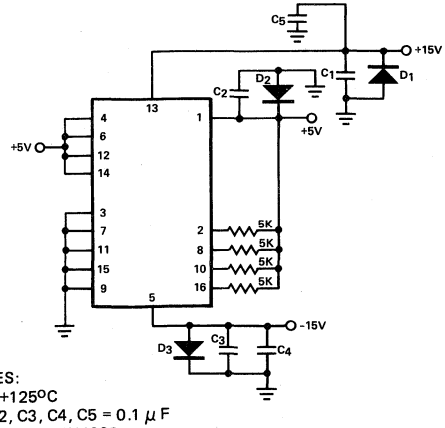
NOTES:
TA = +125°C
D1, D2 = IN4002

16 HA-4620/22/25, HA-5114



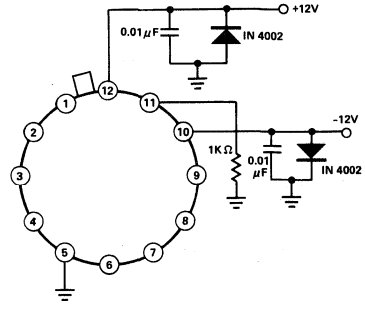
NOTES:
C1 = C2 = 0.01 μF
D1 = D2 = IN4002
R1 = 10KΩ, ±5% ¼W
R2 = 1KΩ, ±5%, ¼W

17 HA-4900/02/05



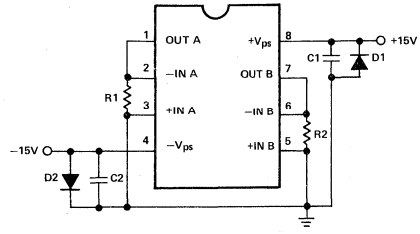
NOTES:
TA = +125°C
C1, C2, C3, C4, C5 = 0.1 μF
D1, D2, D3 = IN4002

18 HA-5033



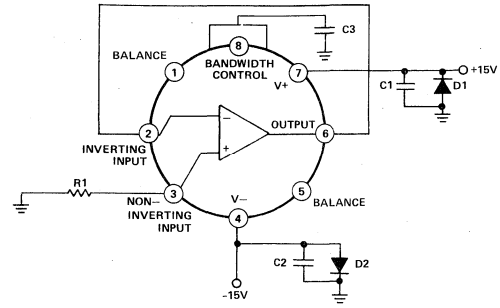
9 QUALITY & RELIABILITY

19 HA-5062, HA-5082, HA-5102 HA-5142, LF 353



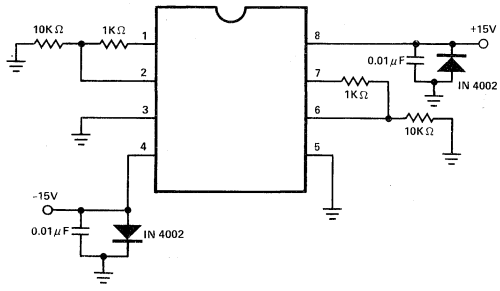
NOTES:
C1, C2 = 0.01μF
D1, D2 = IN4002
R1, R2 = 2kΩ, ⅛ or ¼ Watt, 5%

20 HA-5100/05, HA-5110/15

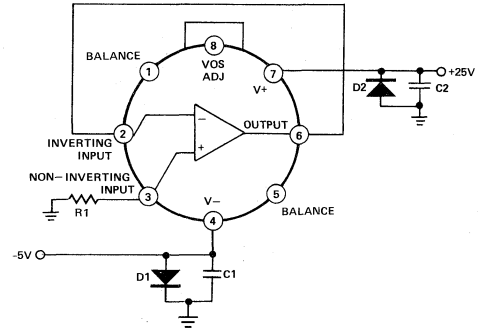


NOTES:
R1 = 1MΩ, ±5%, ¼ or ½ Watt
C3 = 0.01 μF
C1 = C2 = 0.1 μF
D1 = D2 = IN4002

21 HA-5112

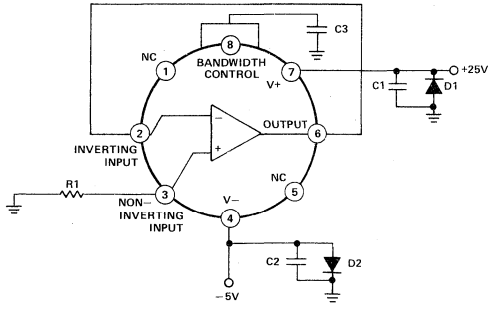


22 HA-5130/35, HA-5141, HA-5170 HA-5180, HA-0P07



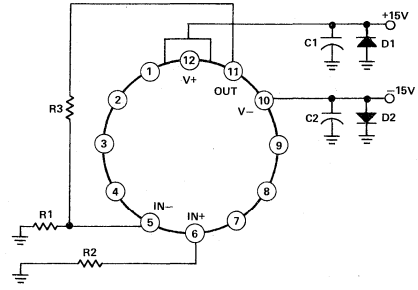
NOTES:
R1 = 1MΩ, 5%, ¼ or ½ Watt
C1, C2 = .01 μF
D1, D2 = IN4002

23 HA-5160/62



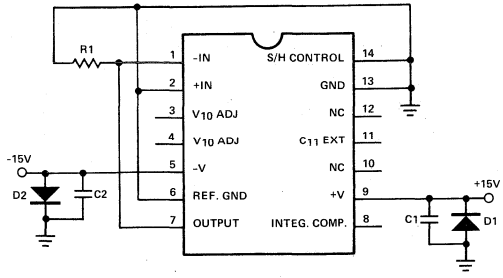
NOTES:
R1 = 1MΩ, ±5%, ¼ or ½ Watt
C1 = C2 = 0.01 μF
C3 = 0.01 μF

24 HA-5190/95



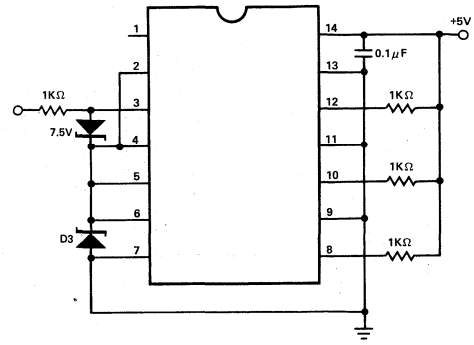
NOTES:
R1, R2: 1kΩ, ¼ or ½ Watt, 5%
R3: 10kΩ, ¼ or ½ Watt, 5%
C1, C2: 0.1μF
D1, D2: IN4002

25 HA-5320

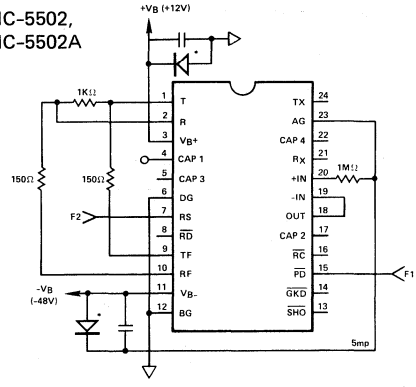


NOTES:
R1 = 10KΩ
D1 =D2 = IN4002
C1 = C2 = 0.01 μF

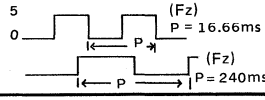
26 HA-23551



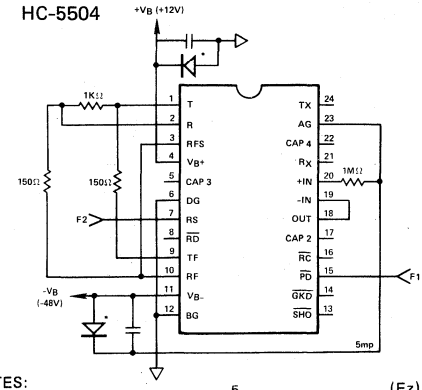
27 HC-5502, HC-5502A



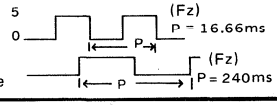
NOTES:
All Resistors ±10%
All Pin not specified leave open
F1 = 60 Hz, 0-5V Square Wave
F2 = 1/240 Hz 0-5V Square Wave



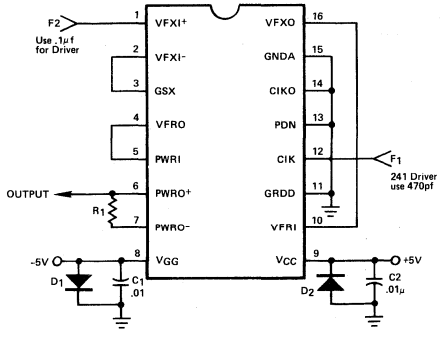
28 HC-5504



NOTES:
All Resistors ±10%
All Pin not specified leave open
F1 = 60 Hz, 0-5V Square Wave
F2 = 1/240 Hz, 0-5V Square Wave

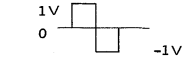


29 HC-5512, HC-5512A, HC-5512C

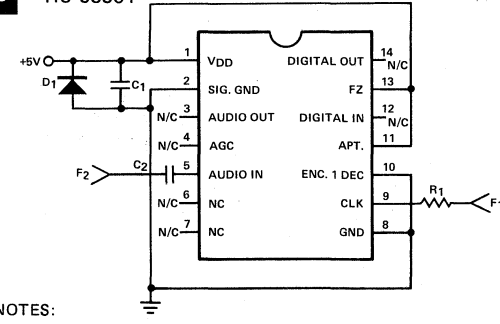


NOTES:
F1 = TTL, 50% Duty Cycle
F1 = 100 KHz
F2 = 2.0V p-p @≅100 Hz,
C1, C2 = .01 μf

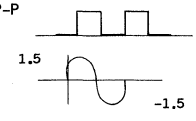
D1, D2 = IN4002
R1 = 600Ω



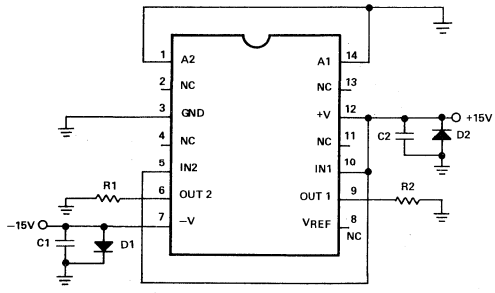
30 HC-55564



NOTES:
F1 - 16kHz , TTL Levels, 50% Duty Cycle, Square Wave
F2≃200 Hz (approximate), 3V, P-P
Sine wave (or triangular wave)
C1 = .01 μf
C2 = .1 μf
D1 = IN4002
R1 = 10KΩ ±5Ω , ¼Watt

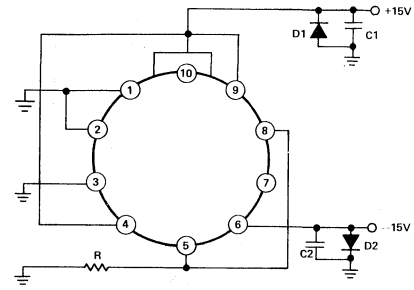


31 HI-200



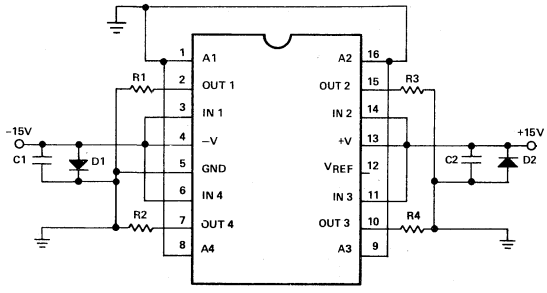
NOTES:
R1, R2 = 1kΩ
C1, C2 = .01 μF
D1, D2 = IN4002

32 HI-200



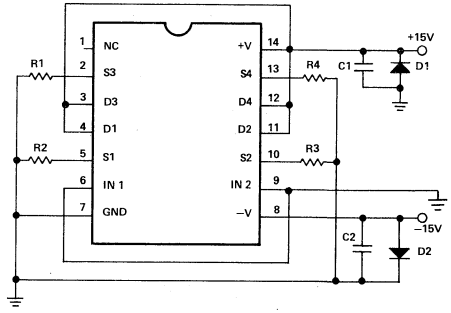
NOTES:
C1 = C2 = 0.01 μF
R = 10KΩ ±5%, ¼ or ½ Watt
D1 = D2 = IN4002

33 HI-201, HI-201 HS



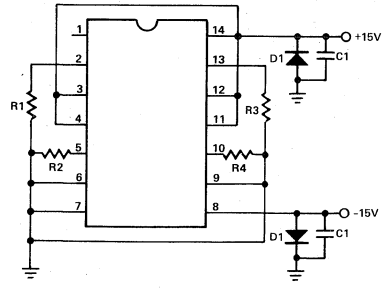
NOTES:
R1, R2, R3, R4 = 10kΩ, 5%, ¼ or ½ Watt
C1, C2 = .01μF
D1, D2 = IN4002

34 HI-300, HI-301, HI-302



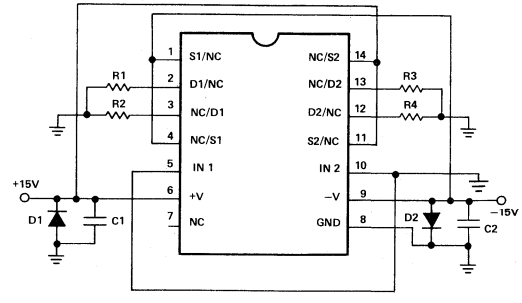
NOTES:
R1, R2, R3, R4 – 10kΩ, 5%, ¼ or ½ Watt
C1, C2 = .01μF
D1, D2 = IN4002

35 HI-303, HI-304, HI-305, HI-306, HI-307



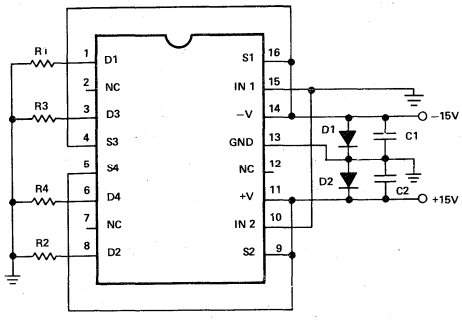
NOTES:
R1 to R4 = 10KΩ
C1 = 0.01 μF
D1 = IN4002

36 HI-381, HI-387



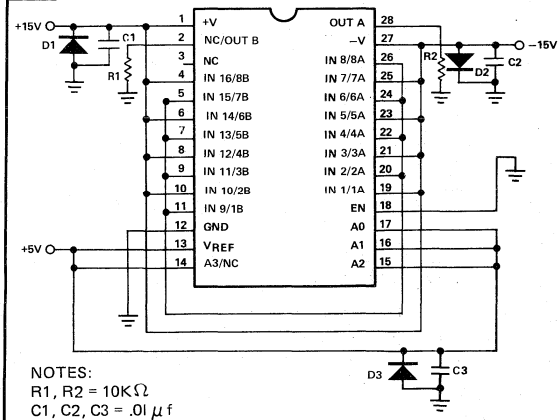
NOTES:
R1 – R4 = 10kΩ, ±5%, ¼ or ½ Watt
C1 – C2 = .01μF
D1 – D2 = IN4002

37 HI-384, HI-390



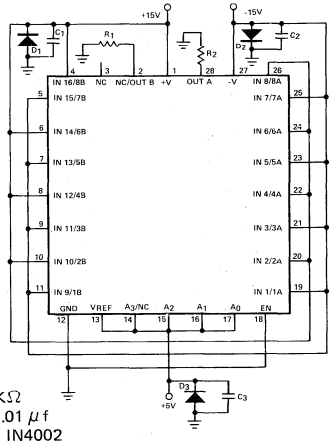
NOTES:
R1 – R4 = 10kΩ, ±5%, ¼ or ½ Watt
C1 – C2 = .01μF
D1 – D2 = IN4002

38 HI-506/507, HI-506A/507A



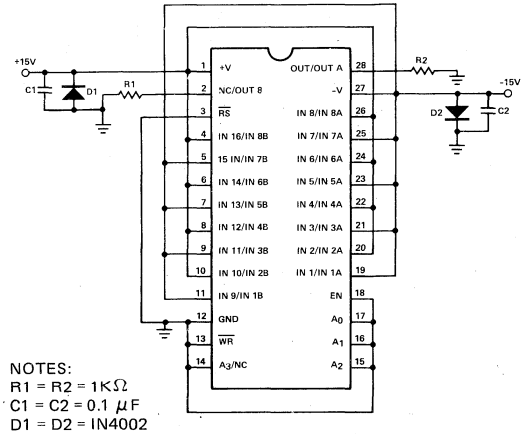
NOTES:
R1, R2 = 10KΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

39 HI-506/507 (LCC), HI-506A/507A (LCC)



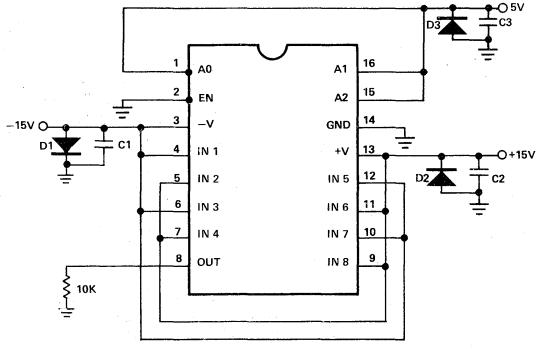
NOTES:
R1, R2 = 10KΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

40 HI-506L/507L



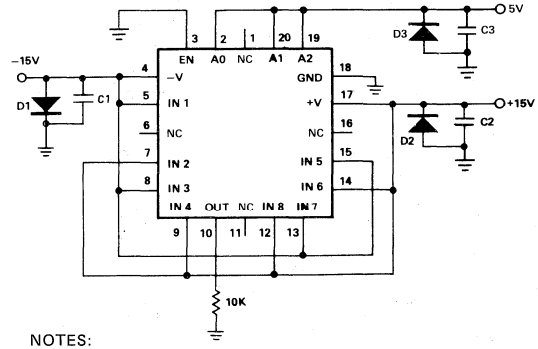
NOTES:
R1 = R2 = 1KΩ
C1 = C2 = 0.1 μF
D1 = D2 = IN4002

41 HI-508/508A



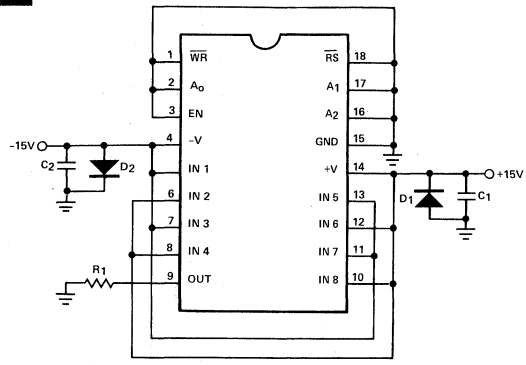
NOTES:
R1 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

42 HI-508/508A (LCC)



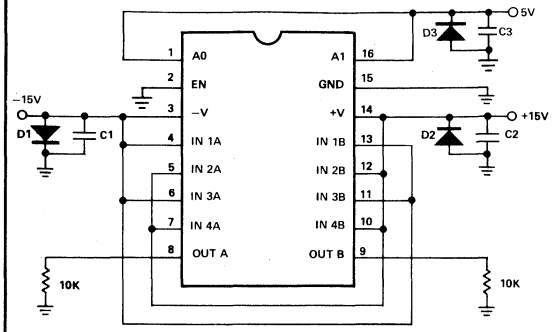
NOTES:
R1 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

43 HI-508L/509L



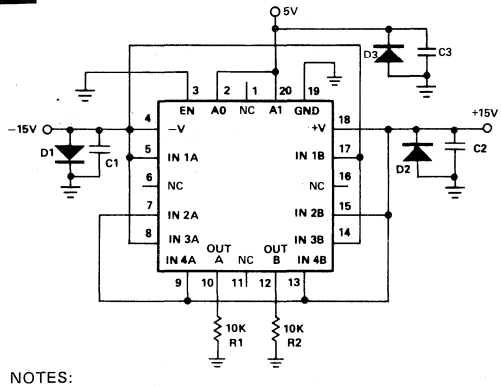
NOTES:
R1 = 1KΩ
C1 = C2 = 0.1 μF
D1 = D2 = IN4002

44 HI-509/509A, HI-539



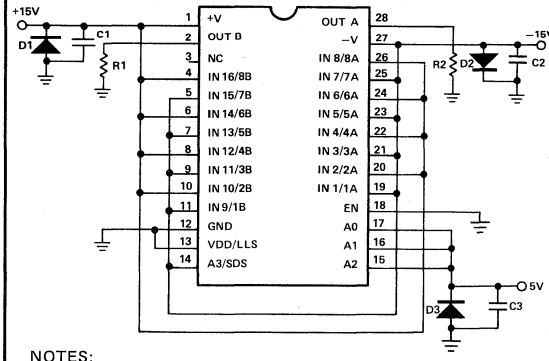
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

45 HI-509/509A (LCC)



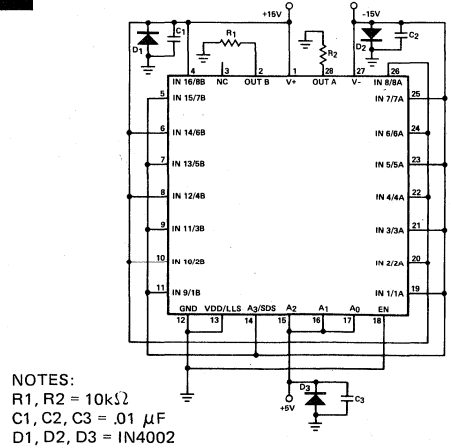
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

46 HI-516



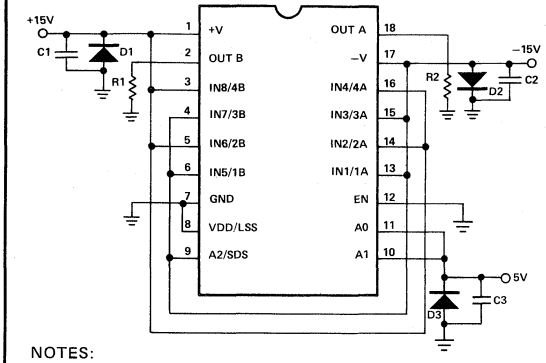
NOTES:
R1, R2 = 10kΩ
D1, D2, D3 = IN4002
C1, C2, C3 = .01 μF

47 HI-516 (LCC)



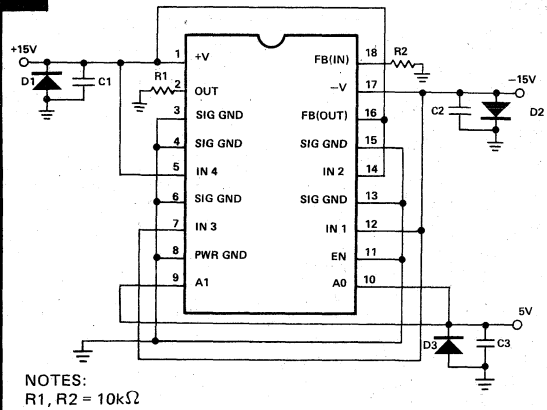
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

48 HI-518



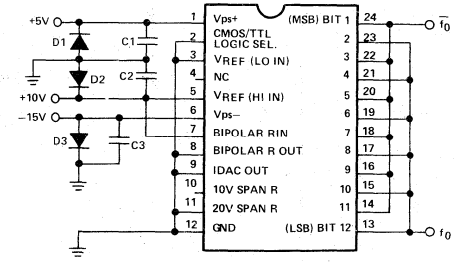
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

49 HI-524



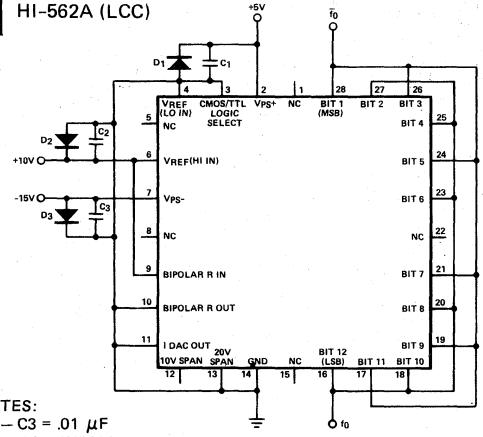
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

50 HI-562A



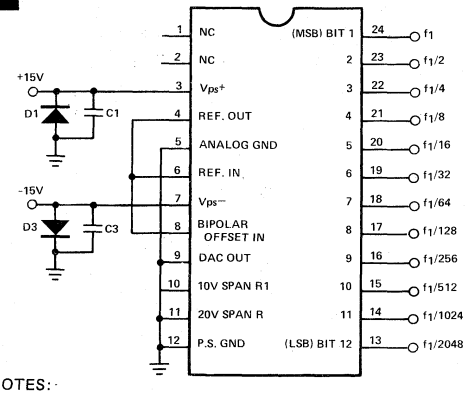
NOTES:
C1 – C3 = .01 μF
D1 – D3 = IN4002
f_0 = 100 KHz, 50% Duty Cycle

51 HI-562A (LCC)



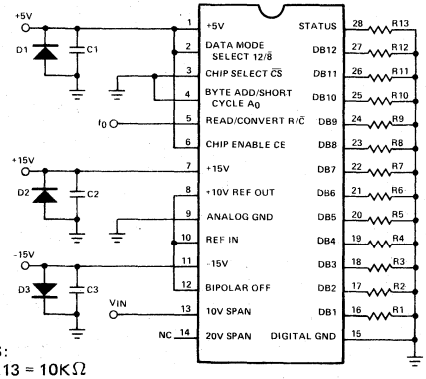
NOTES:
C1 – C3 = .01 μF
D1 – D3 = IN4002
f_0 = 100 KHz, 50% Duty Cycle

52 HI-565A



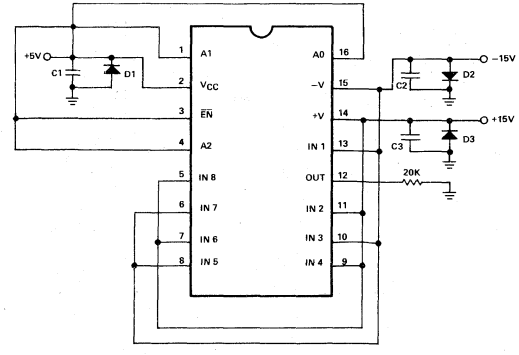
NOTES:
C1 – C3 = .01 μf
D1 – D3 = IN4002
f_1 = 100 KHz

53 HI-574A/674A



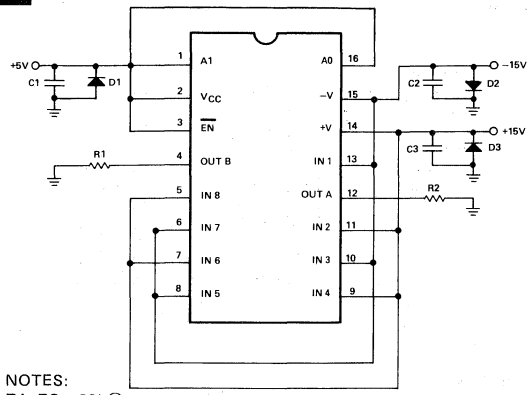
NOTES:
R1 – R13 = 10KΩ
C1 – C3 = 0.1 μF
D1 – D3 = IN4002
V_{IN} = Triangle Wave Form, +5V to -5V. 1KHz
f_0 = 10 KHZ, 90% Duty Cycle, 0V to 5V

54 HI-1818A



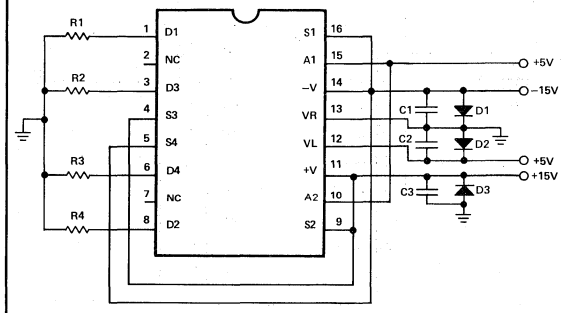
NOTES:
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002

55 HI-1828A



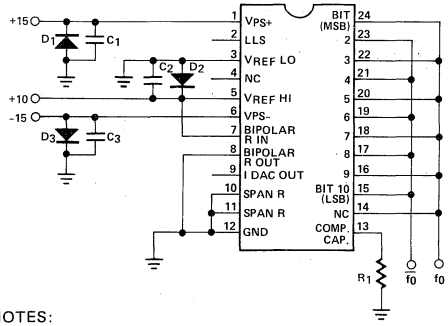
NOTES:
R1, R2 = 20kΩ
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002

56 HI-5040 – HI-5051



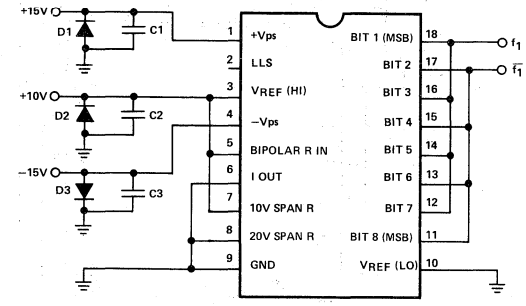
NOTES:
R1 – R4 = 10kΩ, 5%, ¼ or ½ Watt
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
f1 = 100kHz, 50% Duty Cycle
(For Static Configuration Tie Inputs (Pins 10, 15) to +5V)

57 HI-5610



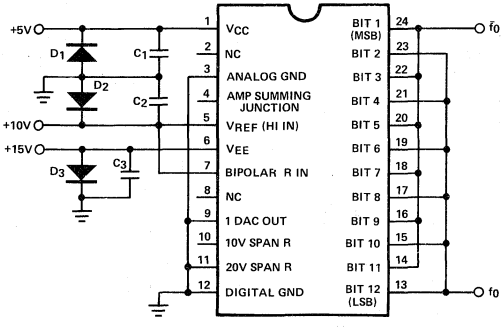
NOTES:
R1 = 50kΩ
D2, D3, D1 = IN4002
C2, C3, C1 = 0.01 μF
f_O = 1KHz, 50% Duty Cycle

58 HI-5618A/5618B



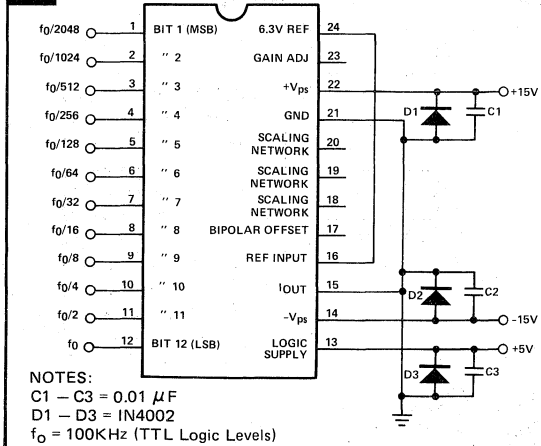
NOTES:
D1 – D3 = IN4002 or Similar
C1 – C3 = .1 μF
f1= 100 KHz, TTL Level, 50% Duty Cycle

59 HI-5660/5660A



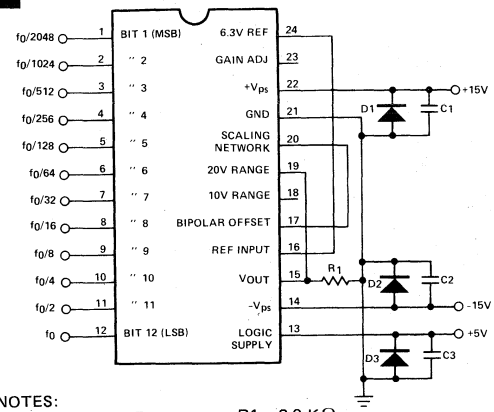
NOTES:
C1 – C3 = .01μf
D1 – D3 = IN4002
f_O = 100 KHz, 50% Duty Cycle

60 HI-5687 (I)



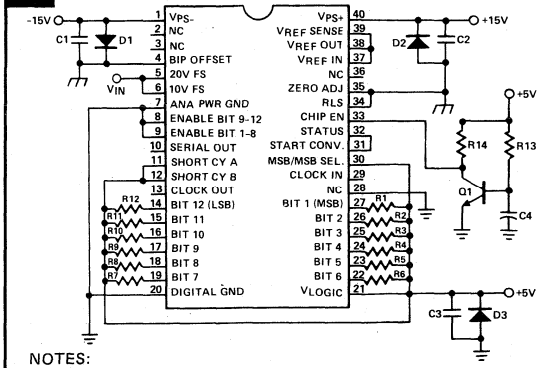
NOTES:
C1 – C3 = 0.01 μF
D1 – D3 = IN4002
f_O = 100KHz (TTL Logic Levels)

61 HI-5687 (V)



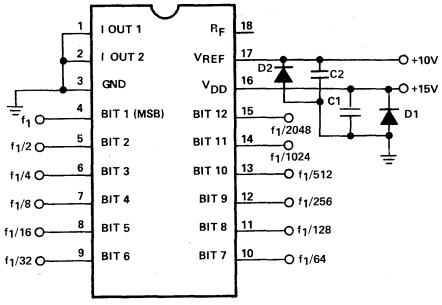
NOTES:
C1 — C3 = 0.01 μF
D1 — D3 = IN4002
R1 = 2.0 KΩ
f_O = 100 KHz, (TTL Logic Level)

62 HI-5712/5712A



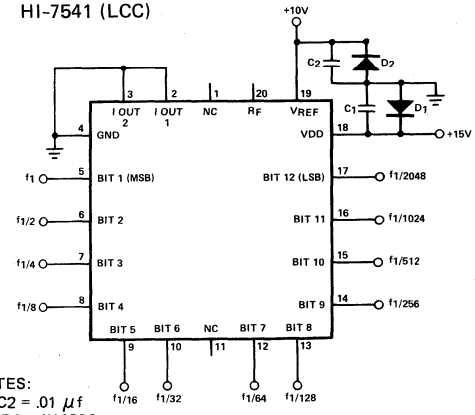
NOTES:
R1 — R12 = 4kΩ
R13 = 10kΩ
R14 = 1kΩ
C1, C2, C3 = .01μF
C4 = 100μF
D1, D2, D3 = IN4002
VIN = 1kHz Triangular Wave, ±5V
Q1 = 2N2222

63 HI-7541



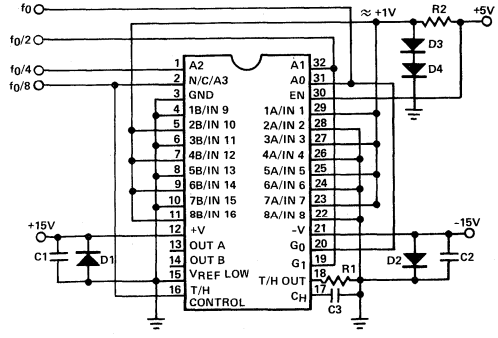
NOTES:
C1, C2 = .01 μf, D1, D2 = IN4002
f1 = 100kHz
Square Wave, TTL Level (0-5V)

64 HI-7541 (LCC)



NOTES:
C1, C2 = .01 μf
D1, D2 = IN4002
f1 = 100kHz
Square Wave, TTL Level (0-5V)

65 HI-5900/5901



NOTES:
C1, C2 = .01 μf
D1 — D4 = IN4002
f_O = 10KHz
R1 = 2K
R2 = 1K

9 QUALITY & RELIABILITY

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* Not Available at time of printing

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509	A simple comparator using the HA-2620	Performance characteristics, application schematics, output parameter control methods.	10-12
514	The HA-2400 PRAM four channel operational amplifier	HA-2400 Programmable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).	10-13
515	Operational amplifier stability: input capacitance considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.	10-20
517	Applications of a Monolithic Sample and Hold/Gated Op Amp	General Sample and Hold information and fourteen specific applications, including filtered Sample & Hold, DAC De-Glitcher, Integrate-Hold-Reset, Gated Op Amp, etc.	10-22
519	Operational amplifiers noise prediction	Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise predicition techniques, typical spot noise curves, popcorn noise discussion.	10-32
520	CMOS analog multiplexers and switches application considerations	Switch selection criteria, datasheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications, alternatives to CMOS switches and multiplexers.	10-39
521	Getting the most out of CMOS devices for analog switching jobs	CMOS versus bipolar device performances, over voltage and channel interaction conditions, JI technology and latch-up, floating-body JI technology, fool-proof CMOS analog multiplexer, other DI benefits.	10-48
522	Digital to Analog Converter Terminology	Explains DAC terminology, Resolution Gain Error, Offset Error, Linearity Error, Differential Linearity Error, Drift, Settling Time, etc.	10-55
524	Digital to Analog Converter High Speed ADC applications	The use of High Speed DAC's in tracking, servo, and successive approximation Analog to Digital Converters. Design ideas for Data Acquisition Systems.	10-58
525	HA-5190/5195 fast settling operational amplifier	Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.	10-61
526	HA-5190/5195 video applications	Video applications, video response tests, S/N ratio measurements, power supply requirements, temperature considerations, design hints, prototyping tips, RF AGC amplifier, DC gain controlled video amplifier.	10-65
527	Applying the HI-5900 Analog Data Acquisition Signal Processor	Describes use of the HI-5900 Signal Processor. Includes a description of the input Multiplexer, Programmable Gain Instrumentation Amplifier, and the Track and Hold Amplifier, plus a Data Acquisition System application.	10-70
528	Interfacing Microprocessor and Microcomputers with HI-5712/5722 High Performance Analog-to-Digital Converter	Description of the HI-5712, plus detailed connections for operation with various Microprocessors and Microcomputers.	10-74
529	Microprocessor Interface methods for High-Speed Data Acquisition Systems	Applications for the HI-5712 and HI-5900/5901. Data Acquisition Systems, Microprocessor interfacing and a software flowchart.	10-79

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533	A monolithic subscriber line interface circuit	Functional description and pin descriptions of PBX SLICS.	10-93
534	Additional information on the HI-300 series	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation and schematics, single supply operation, charge injection, power supplies conditions and protective circuitry.	10-99
535	Design Considerations for a Data Acquisition System (DAS).	A collection of guidelines for the design of a Data Acquisition System. Includes Signal Conditioning, Transducers, Single-Ended vs. Differential Signal Paths, Low Level Signals, Filters, Programmable Gain Amplifiers, Sampling Rate, and computer interfacing.	10-104
536	An accurate method for measuring Settling Time of High Speed D/A Converters	Describes a reliable measurement technique, based on use of a high performance comparator.	10-111
538	Monolithic Sample/Hold combines speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of error sources, and HA-5320 applications.	10-118
539	A Monolithic 16 Bit D/A Converter	Detailed description of the HI-DAC16 D-A Converter, chip photo and schematic, plus applications and interface considerations.	10-125
540	HA-5170 precision low noise J-FET input operational amplifier	Internal design and technology, J-FET noise discussion, trimming of offset voltage, single Op Amp instrumentation amplifier, sine wave oscillator, high impedance transducers interface, current source/sink and current sense circuits.	10-130
541	Using HA-2539 very high slew-rate wideband operational amplifier	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme and DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.	10-134
542	Using the HV-1000 Induction Motor Energy Saver	What is an IMES? IMES application; HV-1000 algorithm; load anticipation; basic circuit application of HV-1000; measuring power savings; handling precautions and reliability.	10-138
543	New high speed switch offers sub 50ns switching times	Application enhancement using the HI-201HS, high speed multiplexers, high speed sample and hold, analog switch and Op Amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.	10-147
545	New Multiplexers Simplify System Design	Description and applications for the Harris HI-50XL family of latched, overvoltage protected multiplexers.	10-154
547	HC-5512C PCM Filter cleans up CVSD CODEC signals	Description of application of PCM Filter as an I/O filter for the CVSD.	*
548	Balancing and matching the HC-550X SLIC	Describes and illustrates balance and matching circuitry synthesis for SLICs used with/without complex line impedance.	*
549	SLIC Application Note by P.G. Phillips	Complete description of device functionality and applications of SLIC.	*
607	Delta modulation for voice transmission	Introduction to delta modulation coding technique, 4 general applications, including digital transmission encryption, voice scrambling, and audio delay. Also CVSD evaluation guidelines.	10-162

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APPLICATION NOTE 508

TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

BY G. G. MILER

The offset voltage of the amplifier under test (A.U.T.) is measured as follows:

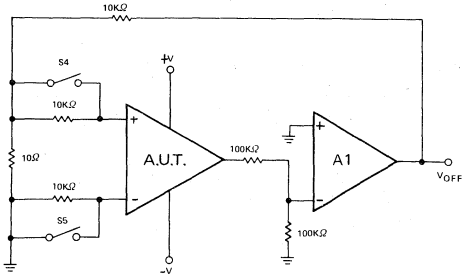
1. Set + and –V to the desired supply voltage and close S4 and S5.
2. Measure the voltage at V_{OFF}.

The offset voltage is equal to (V_{OFF}) (10^{-3}). The feedback amplifier, A1, drives the input of the A.U.T. so that the output is at ground reference, V_{OFF} is driven to 1000 times the voltage necessary to compensate for the offset voltage.

The bias current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and measure V_{OFF2}.
3. The plus input current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.
4. Close S4 and open S5 and measure V_{OFF4}.
5. The minus input current is equal to ($V_{OFF4} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASUREMENT OF OFFSET VOLTAGE, BIAS CURRENT, AND OFFSET CURRENT 10KΩ

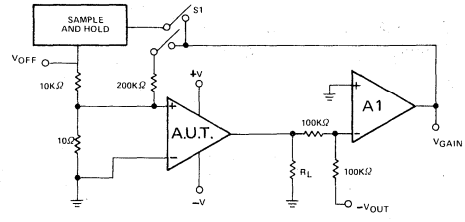


The bias current is equal to the average of the plus and minus input currents.

The input offset current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and S5 and measure V_{OFF2}.
3. The offset current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASURING OPEN LOOP VOLTAGE GAIN



The open loop voltage gain is measured as follows:

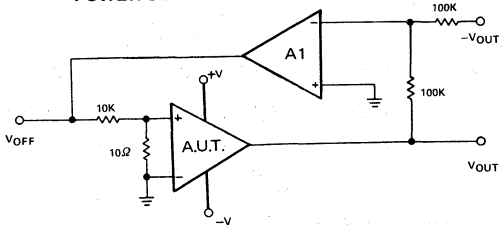
1. Set the +V and -V supply voltages to the desired value and set $-V_{OUT}$ to ground.
2. Close S1 so that the sample and hold will null the offset voltage.
3. S1 can be opened when the circuit stabilizes. The sample and hold will maintain the voltage which nulls the offset voltage.
4. Set $-V_{OUT}$ to the desired output voltage, $-V_4$ and measure V_{GAIN4}.
5. Set $-V_{OUT}$ to another output voltage, –V5 and measure V_{GAIN5}.

6. The gain is equal to

$$\left[\frac{V4 - V5}{V_{GAIN4} - V_{GAIN5}}\right] \times 20{,}000.$$

$-V_{OUT}$ can be first set to zero and then to −10 volts. This gives the gain in the plus direction. The gain in the minus direction can be determined by using zero and +10 volts. The average gain can be determined by using output voltages of −10 and +10 volts.

TEST CIRCUITS FOR MEASUREMENT OF COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO



Common Mode Rejection Ratio:

1. Set +V to +20 VDC, -V to -10 VDC, V_{OUT} +5 VDC by applying -5 VDC to $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC, -V to -20 VDC, V_{OUT} to -5 VDC by applying +5 VDC to $-V_{OUT}$.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.

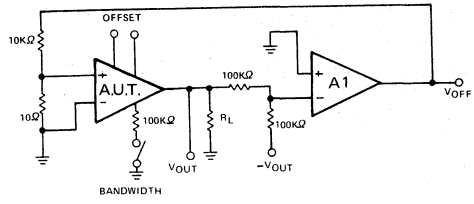
The +1.0 volt limit corresponds to a rejection ratio of 80 dB.

Power Supply Rejection Ratio:

1. Set +V to +20 VDC, -V to 15 VDC, V_{OUT} to ground by grounding $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.
5. Set +V to +15 VDC, -V to -10 VDC.
6. Measure V_{OFF6}.
7. Set -V to -20 VDC.
8. Measure $| V_{OFF6} - V_{OFF8} |$ <1.0 VDC.

The ±1.0 volt limit corresponds to a rejection ratio of 80 dB.

TEST CIRCUITS FOR MEASURING OUTPUT VOLTAGE/CURRENT, POWER DISSIPATION, AND CONTINUITY CHECKS

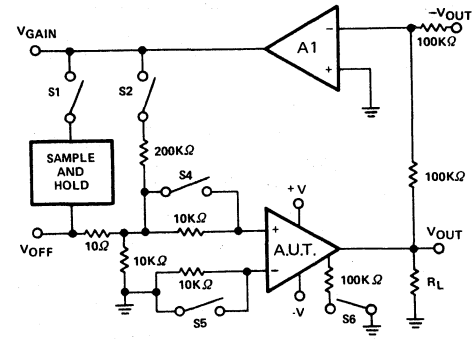


The output voltage/current is measured by connecting a load resistor, R_L, to the output of the A.U.T. The value of R_L is chosen to yield an output current which is the minimum acceptable output current at the desired output voltage. The amplifier under test is programed to a voltage greater than the desired output voltage by applying an equal but opposite polarity voltage to $=V_{OUT}$. The output voltage, V_{OUT}, is measured to see if it reaches the desired output voltage. This test is performed driving the output positive and driving the output negative.

The power dissipation is measured by driving the output voltage to zero by grounding $-V_{OUT}$ and measuring the current in one of the power supply leads.

The continuity of the bandwidth control point is checked by applying −5V to $-V_{OUT}$ and grounding the bandwidth control point through a 100K resistor. V_{OUT} should be less than one volt. There is a known relationship between the voltage at the bandwidth control point and the output voltage, V_{OUT}. This relationship depends on the device type. The continuity of the offset control points is determined by measuring the voltage at these points. These voltages will be slightly less than the positive supply voltage for the HA-2600 and the HA-2500.

SIMPLIFIED SCHEMATIC OF THE COMPLETE D.C. TEST CIRCUIT FOR OPERATIONAL AMPLIFIERS



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APPLICATION NOTE 509

A SIMPLE COMPARATOR USING THE HA-2620

BY G. G. MILER

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

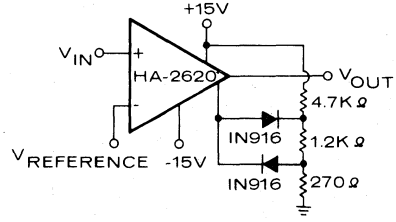


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

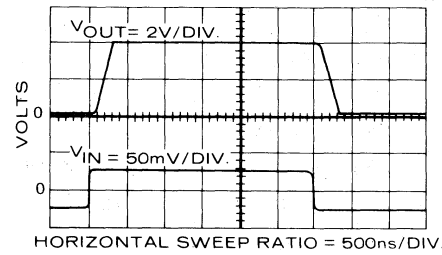


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

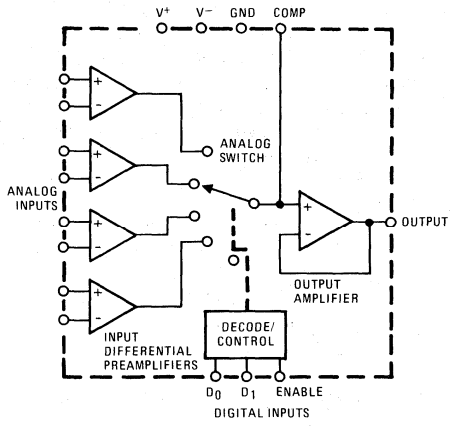
APPLICATION NOTE 514

THE HA-2400 PRAM FOUR CHANNEL OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

CIRCUIT CONNECTIONS

These inputs control the selection of the amplifier input channels in accordance with the truth table below:

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $\quad +2.0V \geq H \geq +5.0V$

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

COMPENSATION

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A.C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

GAIN, VOLTS/VOLT		C_{COMP}	BANDWIDTH (TYPICAL)	SLEW RATE (TYPICAL)
NON-INVERTING	INVERTING	pF	(-3dB), MHz	VOLTS/μs
1	-	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40÷GAIN	50

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

APPLICATIONS

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

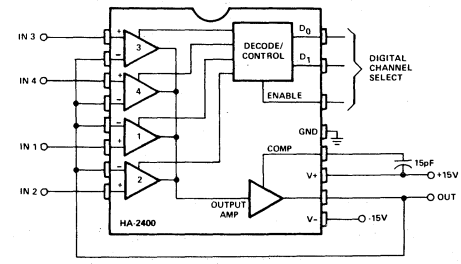
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

APPLICATION NO. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (–) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

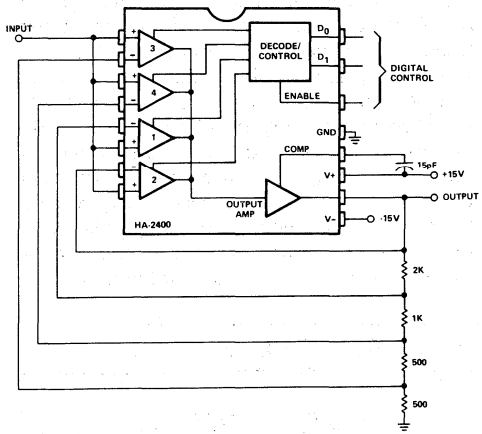
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

APPLICATION NO. 2



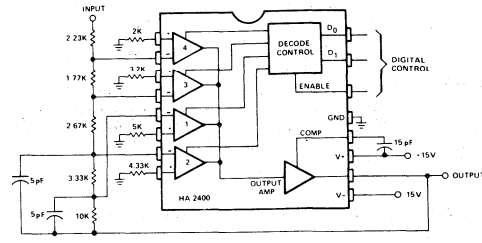
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

APPLICATION NO. 3

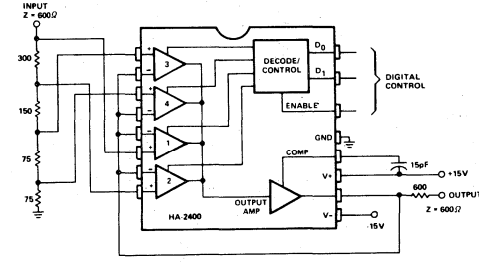


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, –1, –2, –4 or –8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

APPLICATION NO. 4

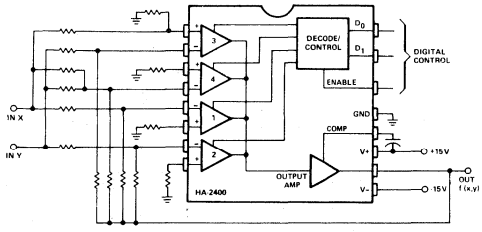


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

APPLICATION NO. 5

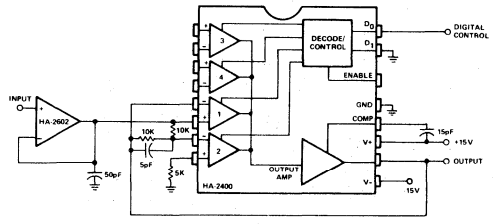


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

APPLICATION NO. 6

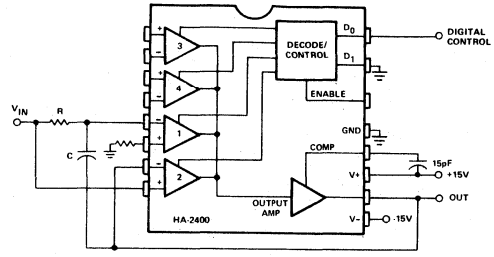


PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D.C. output being proportional to the phase difference, with zero volts at $\pm 90^{o}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

APPLICATION NO. 7

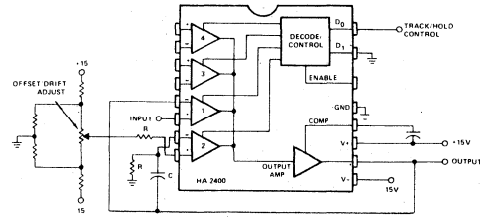


INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D.C. input. Many variations are possible, such as programmable time constant integrators.

APPLICATION NO. 8



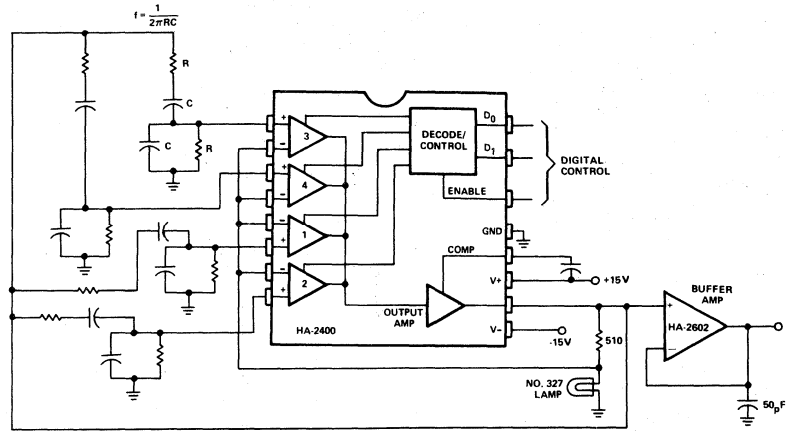
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

APPLICATION NO. 9

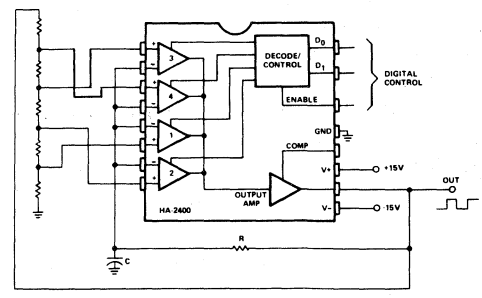


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

APPLICATION NO. 10



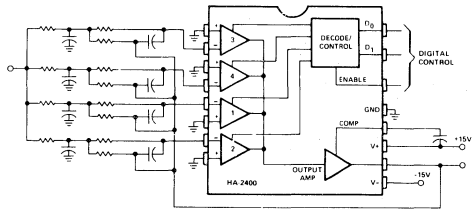
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

APPLICATION NO. 11



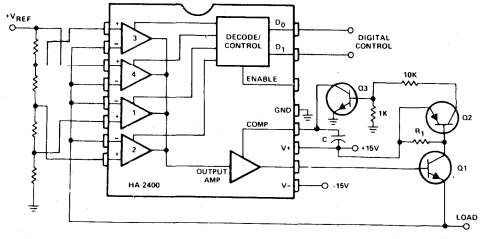
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

APPLICATION NO. 12

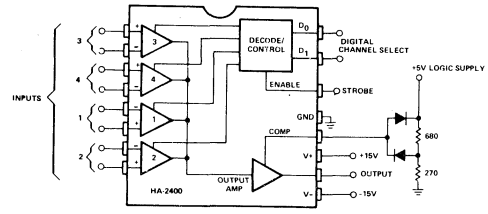


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

APPLICATION NO. 13



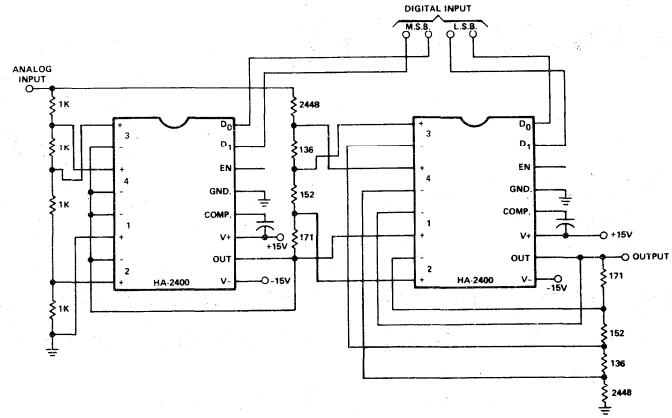
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

APPLICATION NO. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

MORE CHALLENGES

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

FEEDBACK

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

HARRIS

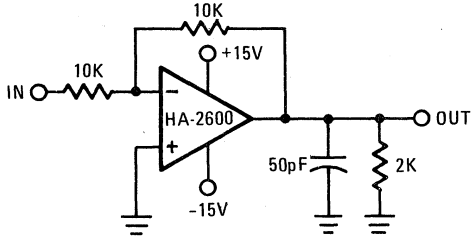
APPLICATION NOTE 515

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

BY DON JONES

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



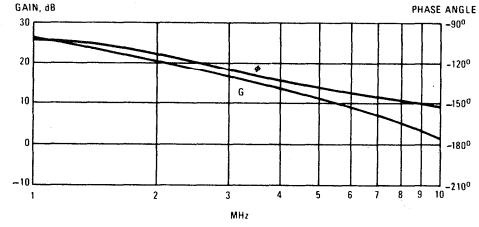
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

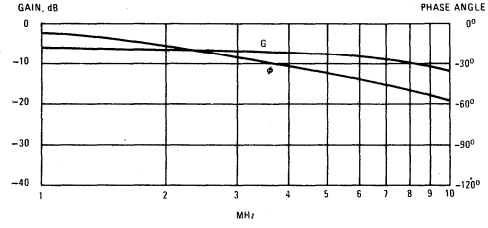
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

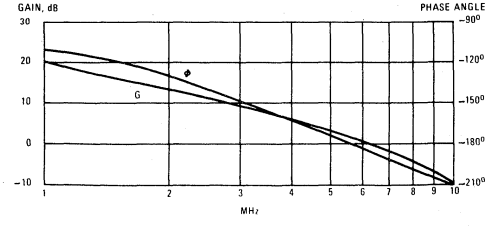
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:

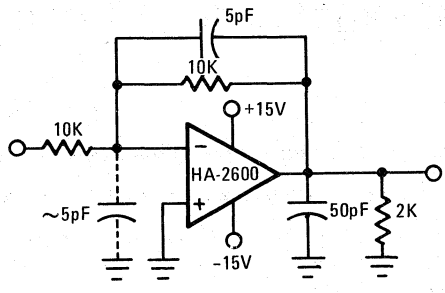


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



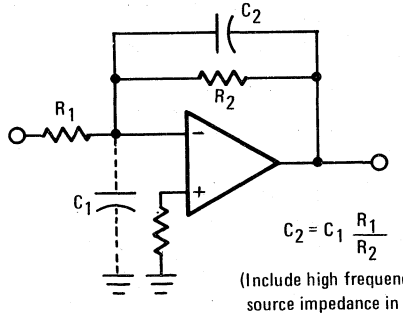
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

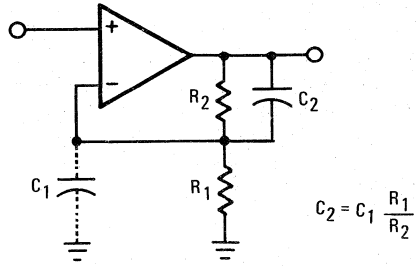


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

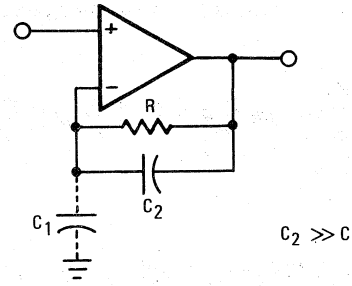
The general scheme for compensation of various circuit types is shown below:



INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

HARRIS

APPLICATION NOTE 517

APPLICATIONS OF A MONOLITHIC SAMPLE-AND-HOLD/GATED OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

The sample-and-hold or track-and-hold function is very widely used in linear systems. Until recently, this function was available only in modular or hybrid circuits; or perhaps most frequently the circuit was constructed by the user from an analog switch, a capacitor, and a very low bias current operational amplifier.

A high quality sample-and-hold circuit must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold, particularly the user built variety, involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate; a combination satisfied by only a few available amplifiers.

THE HA-2420/2425

The HA-2420/2425 is the first complete monolithic sample-and-hold integrated circuit. A functional diagram is shown in Figure 1.

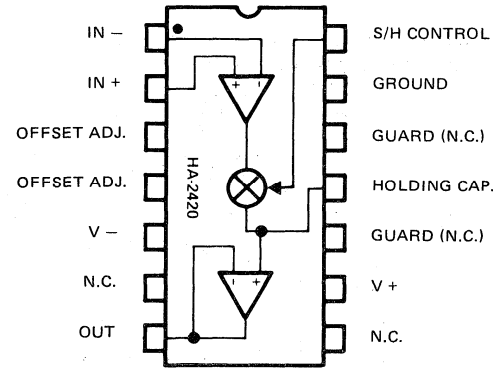


Figure 1 – HA-2420/2425 Functional Diagram

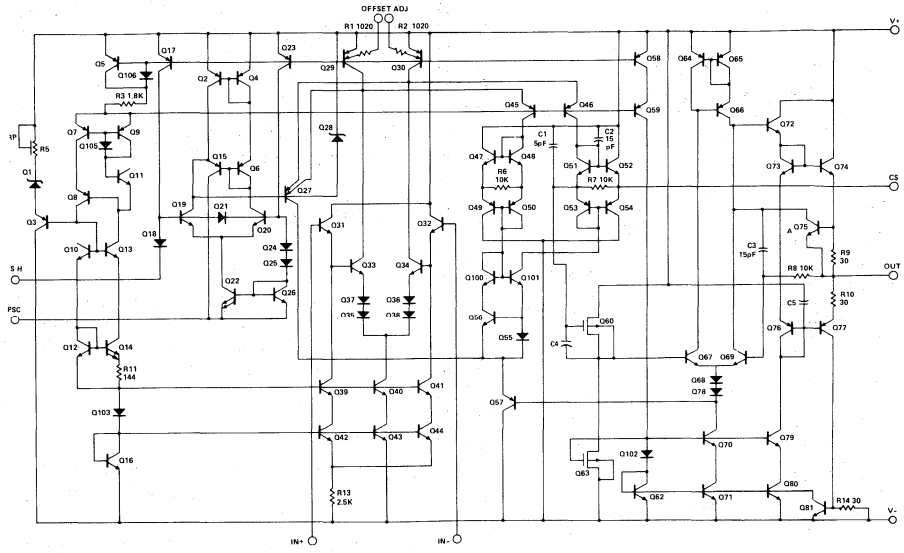
The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage

drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The schematic of the HA-2420 is in Figure 2. During sampling (S/H control LOW) the signal path through the input amplifier stage starts at Q31-34, through Q45 and Q46, and then to the holding capacitor terminal through Q51-54. The output follower amplifier has its input at MOSFET Q60.

HA-2420/2425
Sample-and-Hold



NOTE: 1. Unless otherwise specified resistance values are in OHMS, capacitance values are in picofarads.

Figure 2

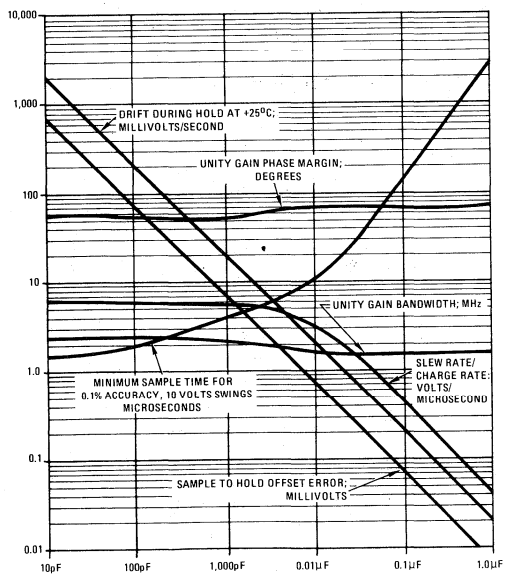


Figure 3 – Holding Capacitor, C_H

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE

In the "hold" mode, the S/H control is HIGH, so Q21 conducts, turning on Q27 which diverts the signal away from Q45 and Q46, and passes the signal to V - through Q57. Q57 also forces Q51-54 to ride up and down with the output signal, so there is virtually zero potential between these transistor bases and the voltage on C_H; completely eliminating leakage from C_H back into the input amplifier.

SAMPLE-AND-HOLD APPLICATIONS

A number of basic applications are shown on the following pages. The device is exceptionally versatile, since it can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the timing capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the

charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. The graph in Figure 3 shows these tradeoffs. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

Guard Ring Layout (Bottom View)

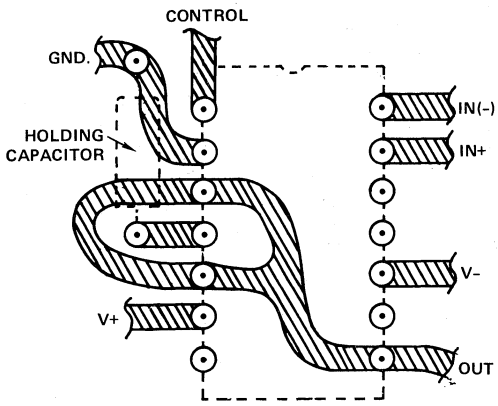


Figure 4

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. Since the output voltage is nearly equal to the voltage on C_H, the output line may be used as a guard line surrounding the line to C_H. Then, since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4.

GATED OPERATIONAL AMPLIFIER APPLICATIONS

An operational amplifier with a highly efficient analog switch in series with its output is a very useful building block for linear systems. The amplifier can be connected in any of the conventional op amp feedback configurations.

With the switch closed, the circuit behaves as a conventional op amp with excellent bandwidth, slew rate, high output current capability, and is able to drive capacitive loads with good stability. With the switch open, the output node is an almost perfect open circuit.

The output buffer amplifier has extremely high input impedance and exceptionally low bias current, but is not particularly well suited for D.C. applications outside an overall feedback loop, since its offset voltage may be quite high.

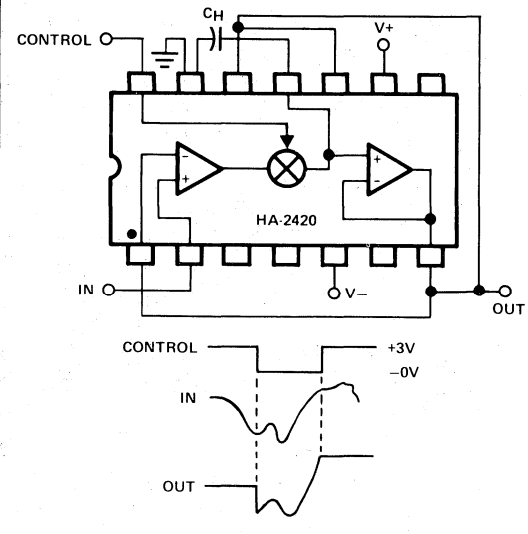
A number of possible gated amplifier applications are suggested in the following section.

APPLICATION NO. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; and the output will hold the level present at the instant the switch is opened. In sample-and-hold opera-

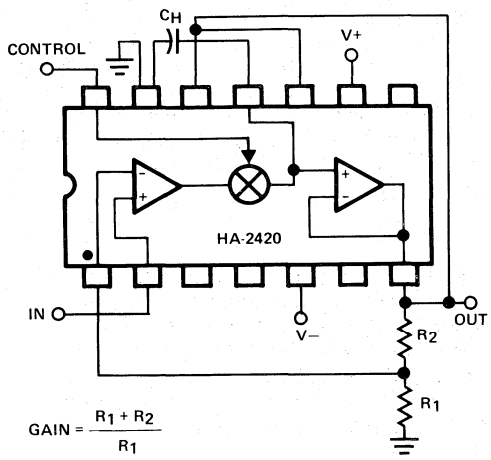
Basic Track-and-Hold/Sample-and-Hold



tion, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

APPLICATION NO. 2

Sample-and-Hold With Gain



This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which the HA-2420 may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

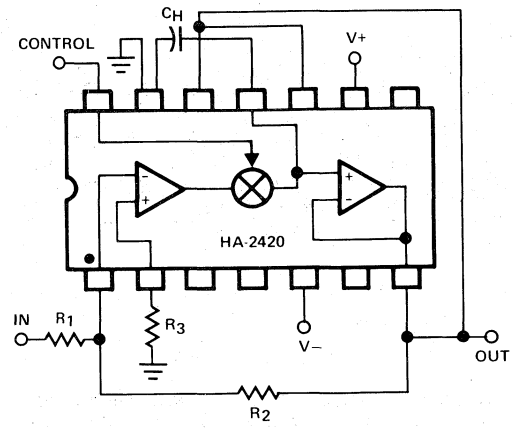
In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or – 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

APPLICATION NO. 3

This illustrates another application in which the hookup versatility of the HA-2400 often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be:

$$\frac{Vin\ Ro}{R_1 + R_2 + R_0}$$

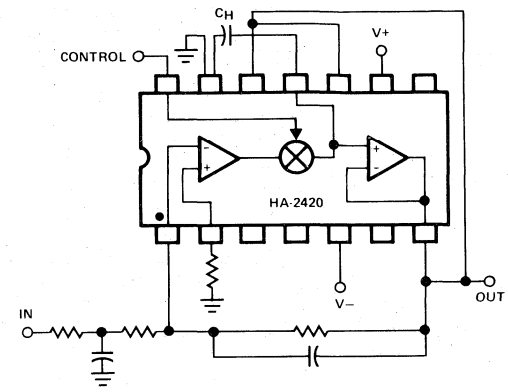
Inverting Sample-and-Hold



APPLICATION NO. 4

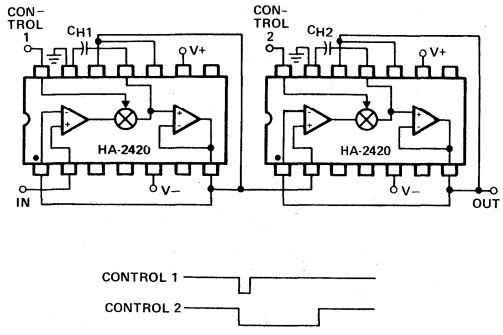
It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

Filtered Sample-and-Hold



APPLICATION NO. 5

Cascaded Sample-and-Hold

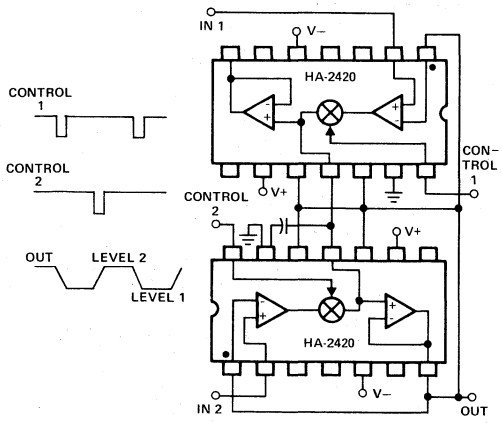


Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

APPLICATION NO. 6

Two or more S/H circuits may share a common holding capacitor and output as shown. The only limit to the number of devices to be

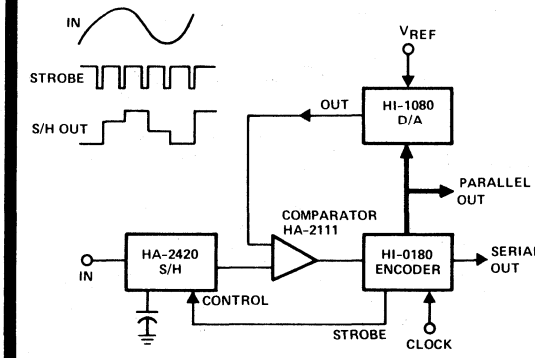
Multiplexed Sample-and-Hold



multiplexed is that the leakage currents of all devices add together, which increases drift during holding.

APPLICATION NO. 7

A/D Converter

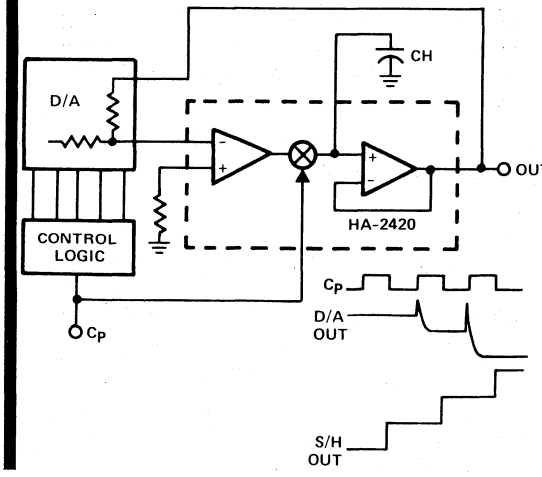


Certain analog to digital converters such as the successive approximation type require that the input signal be a steady D.C. level during the conversion cycle. The HA-2420 is ideal for holding the signal steady during conversion; and also functions as a buffer amplifier for the input signal, adding gain, inversion, etc., if required.

The system illustrated is a complete 8 bit successive approximation converter requiring only four I.C. packages and capable of up to 40,000 conversions per second. Interconnection details are shown on the HI-0180 data sheet.

APPLICATION NO. 8

De-Glitcher



The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which momentarily goes in the wrong direction when the digital input address is changed.

In the illustration, the HA-2420 does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

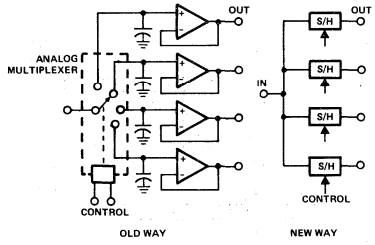
The HA-2420 may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

APPLICATION NO. 9

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject

De-Multiplexer

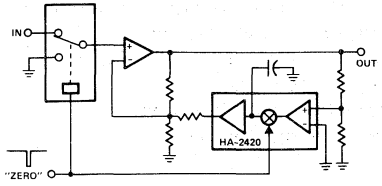


to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

Use of the HA-2420 greatly diminishes all of these problems.

APPLICATION NO. 10

Automatic Offset Zeroing



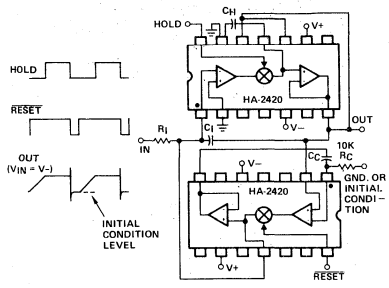
This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

APPLICATION NO.11

Integrate-Hold-Reset



This circuit accurately computes the functions,

$$V_o = \int_{T_1}^{T_2} V_{in}\, dt$$

and holds the answer for further processing.

Resetting circuits for integrators have always been a practical design problem. The reset circuit must produce an extremely low leakage current across the integrating capacitor, and must produce a very low offset voltage when turned on. The circuit illustrated has excellent results since the leakage at the switch node is exceptionally low. R_C and C_C prevent oscillations during reset and their product should be at least 0.02 times R_I X C_I.

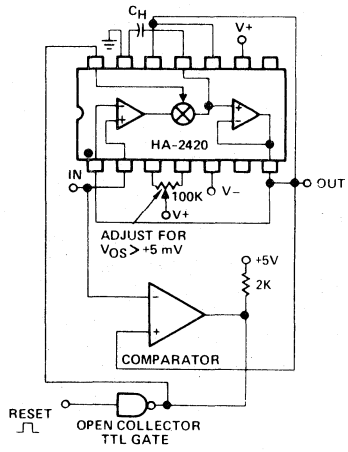
For the simpler integrate and reset function without a hold, substitute an ordinary operational amplifier for the upper device.

APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

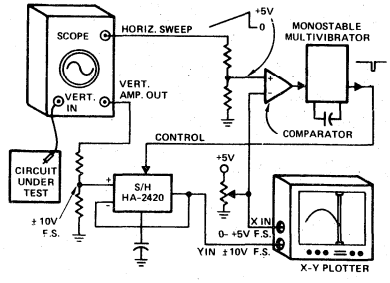
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.



The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques



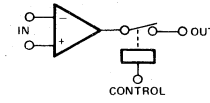
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

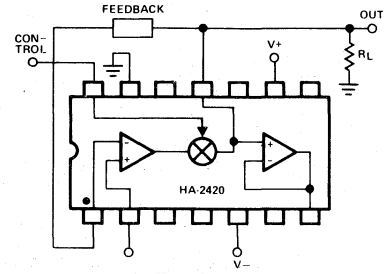
This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier



EQUIVALENT CIRCUIT



The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

Analog Multiplexer Element
Gated Oscillator
Precision Timing Circuit
Chopper Type Modulator/Demodulator
Crosspoint Switch Element
Reset or Initial Conditions Switch
Gated Comparator
Automatic Calibration Switch
Gated Voltage Regulator

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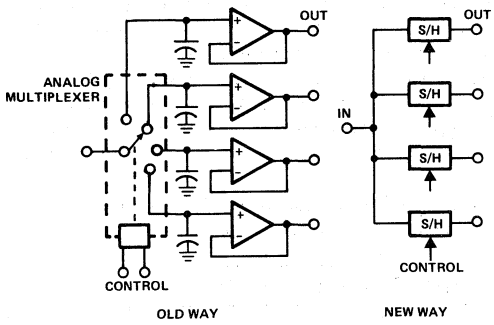

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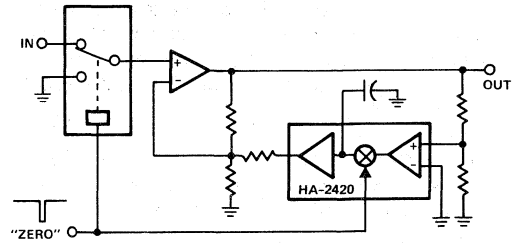

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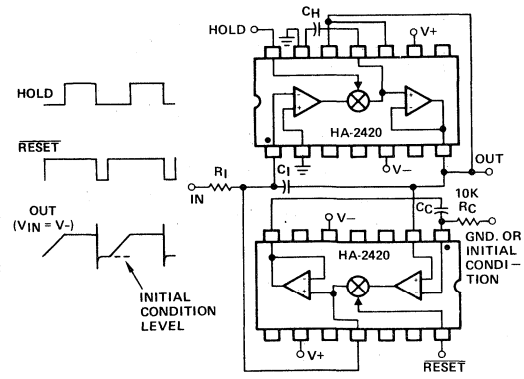
APPLICATION NO.11

Integrate-Hold-Reset



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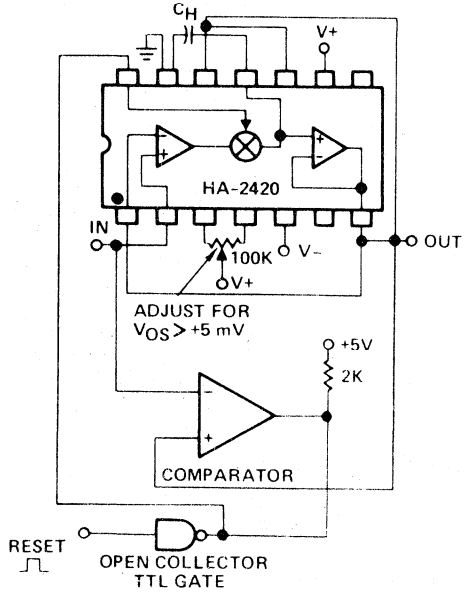
APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

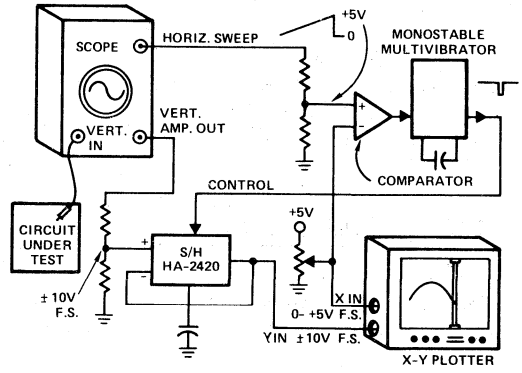
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.



The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques



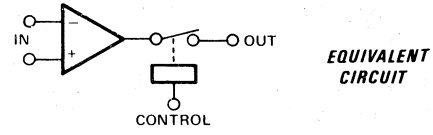
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

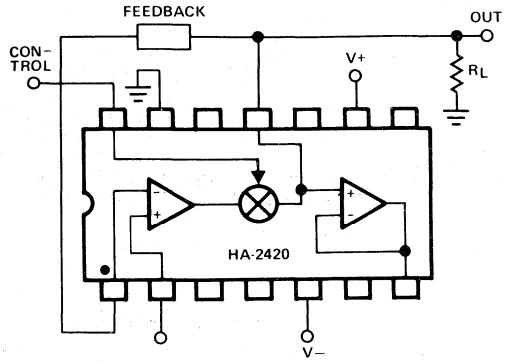
To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier





The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

Analog Multiplexer Element
Gated Oscillator
Precision Timing Circuit
Chopper Type Modulator/Demodulator
Crosspoint Switch Element
Reset or Initial Conditions Switch
Gated Comparator
Automatic Calibration Switch
Gated Voltage Regulator

HARRIS

APPLICATION NOTE 519

OPERATIONAL AMPLIFIER NOISE PREDICTION

BY RICHARD WHITEHEAD

INTRODUCTION

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

THE NOISE MODEL

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g}$$ where,

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.23 \times 10^{-23}$ joules/°K; $T = 300°K$ (27°C) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R^2$

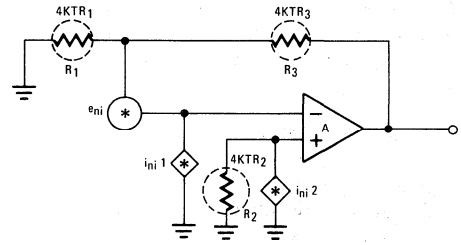


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f1}^{f2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R2}{R1}\right)$ regardless of which input is normally driven.

PROCEDURE FOR COMPUTING TOTAL OUTPUT NOISE

1. Refer to the voltage noise curves for the amplifier to be used. If the R_g value in the application is close to the R_g value in one of the curves, skip directly to step 6, using that curve for values of E_{ni}^2. If not, go to step 2.

2. Enter values of e_{ni}^2 in line (a) of the table below from the curve labeled "$R_g = 0\,\Omega$".

3. From the current noise curves for the

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

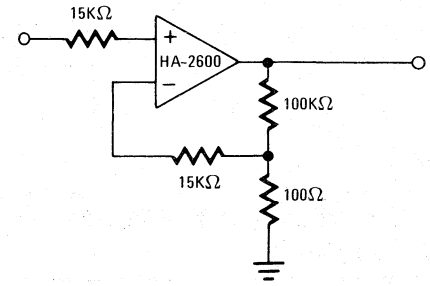
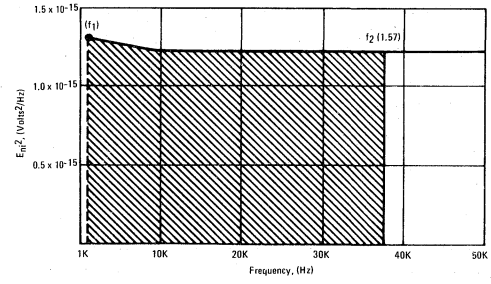


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} $Volts^2$; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

ACTUAL MEASUREMENTS FOR COMPARISON

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

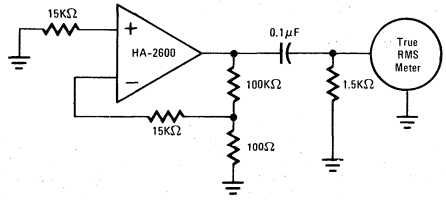


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 microvolts RMS as compared to the calculated value of 6.7 microvolts RMS.

ACQUIRING THE DATA FOR CALCULATIONS

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A DISCUSSION ON "POPCORN" NOISE

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random – an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

REFERENCES

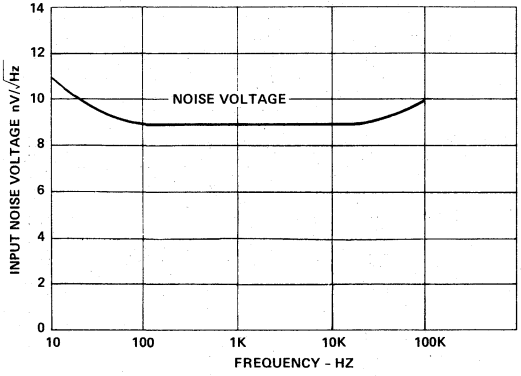
Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

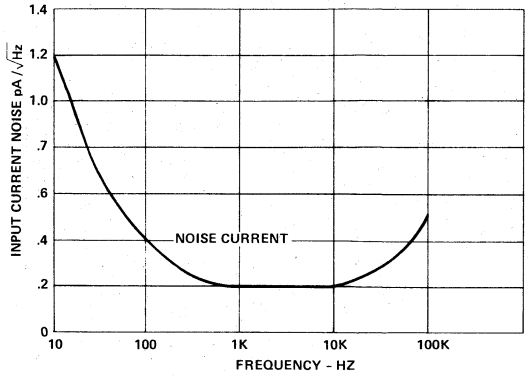
TYPICAL SPOT NOISE CURVES

Unless Otherwise Noted:
$V_S = \pm 15V$ $T_A = +25^oC$

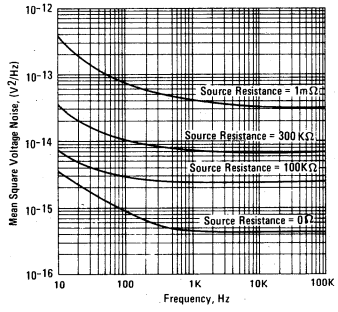
Curve 1
HA-5130/35 INPUT NOISE VOLTAGE



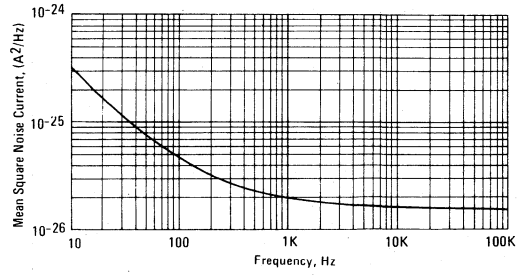
Curve 1A
HA-5130/35 INPUT NOISE CURRENT



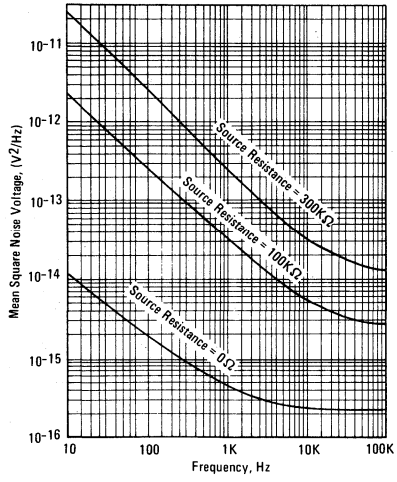
Curve 2
HA-2400 INPUT NOISE VOLTAGE



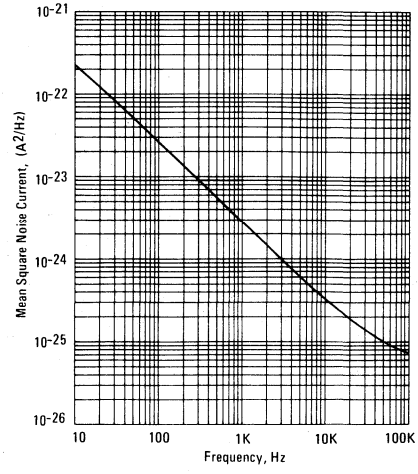
Curve 2A
HA-2400 INPUT NOISE CURRENT



Curve 3
HA-2500/2510/2520 INPUT NOISE VOLTAGE



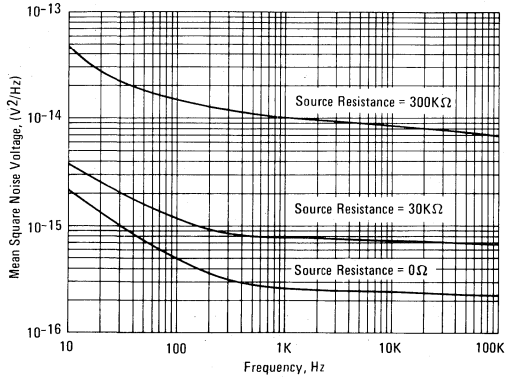
Curve 3A
HA-2500/2510/2520 INPUT NOISE CURRENT



TYPICAL SPOT NOISE CURVES (continued)

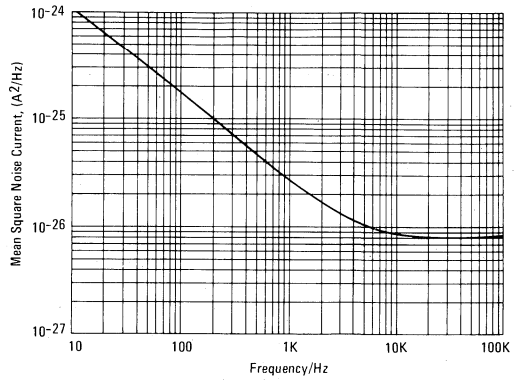
Curve 4

HA-2600/2620 INPUT NOISE VOLTAGE



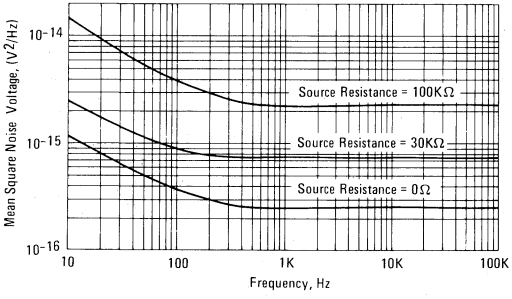
Curve 4A

HA-2600/2620 INPUT NOISE CURRENT



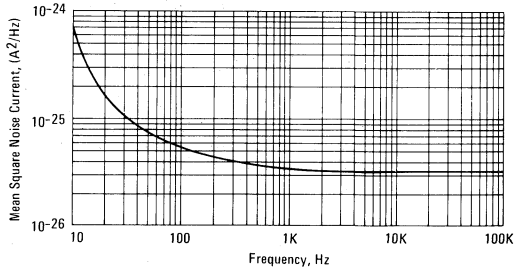
Curve 5

HA-2640/2645 INPUT VOLTAGE NOISE ($V_S = \pm 30V$)



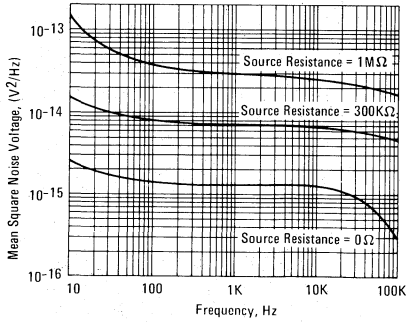
Curve 5A

HA-2640/45 INPUT NOISE CURRENT ($V_S = \pm 30V$)



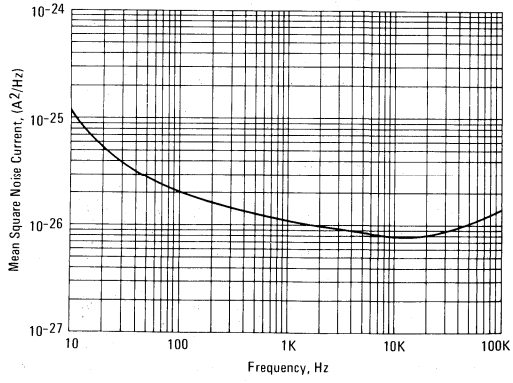
Curve 6

HA-2700 INPUT NOISE VOLTAGE



Curve 6A

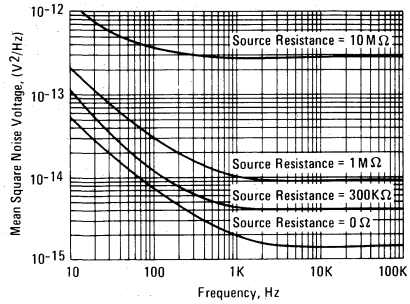
HA-2700 INPUT NOISE CURRENT



TYPICAL SPOT NOISE CURVES (continued)

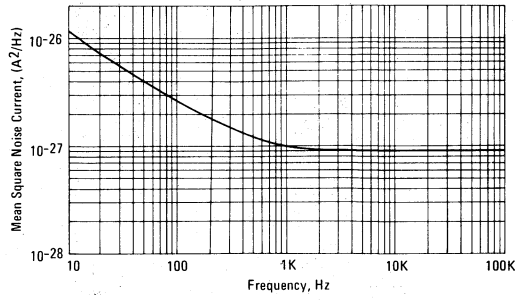
Curve 7

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 1μA)



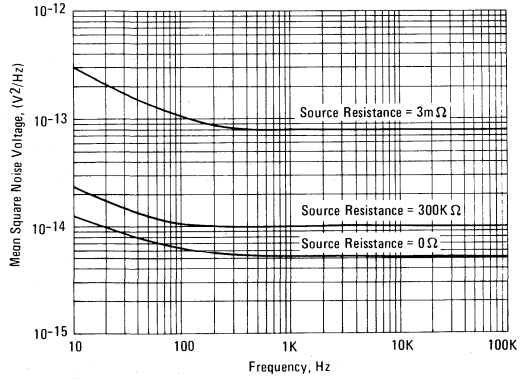
Curve 7A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 1μA)



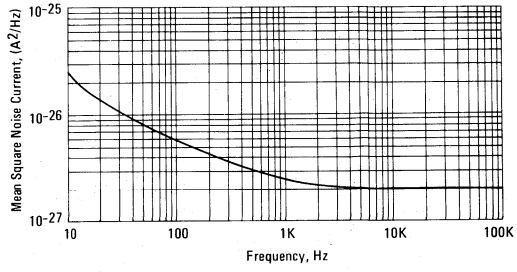
Curve 8

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 10μA)



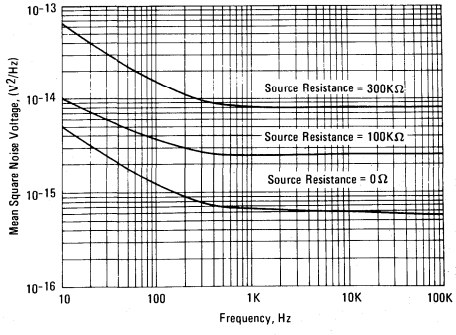
Curve 8A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 10μA)



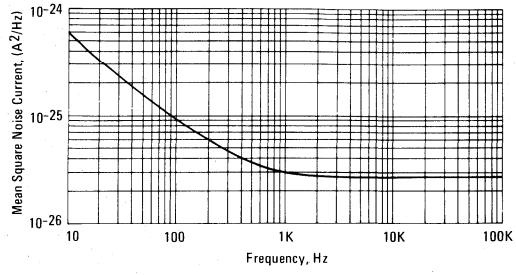
Curve 9

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 100μA)



Curve 9A

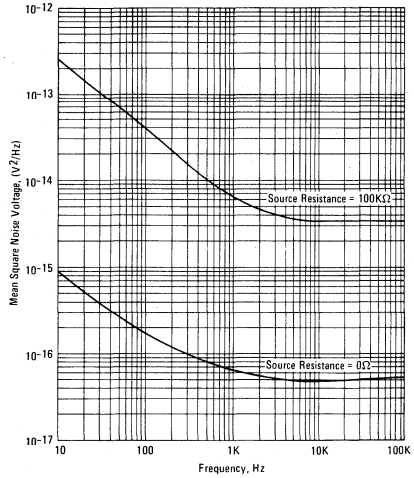
HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 100μA)



TYPICAL SPOT NOISE CURVES (continued)

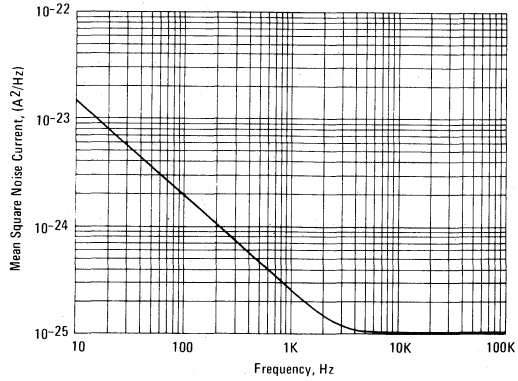
Curve 10

HA-4602/4605 INPUT NOISE VOLTAGE



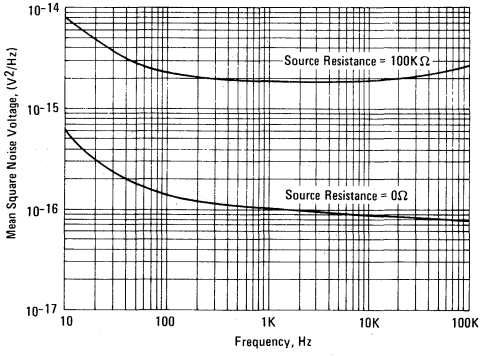
Curve 10A

HA-4602/4605 INPUT NOISE CURRENT



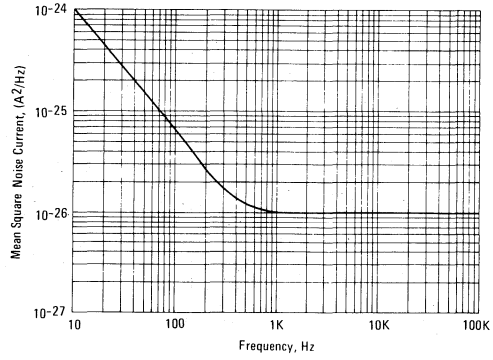
Curve 11

HA-4741 INPUT NOISE VOLTAGE

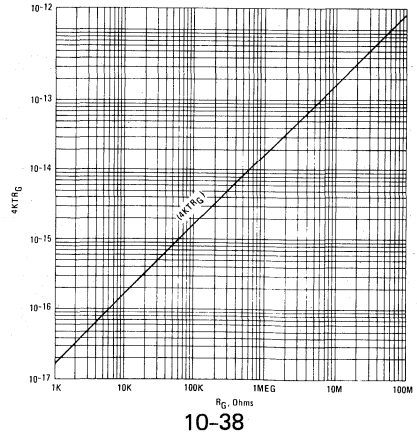


Curve 11A

HA-4741 INPUT NOISE CURRENT



Curve 12



HARRIS

APPLICATION NOTE 520

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

BY DON JONES

INTRODUCTION

This paper is a mixed collection of answers to questions most frequently asked about CMOS analog multiplexers and switches. It covers selection criteria, parameter definitions, handling and design precautions, typical applications, and special topics such as transient considerations and R.F. switching. Some other devices which perform analog switching functions in particular applications are also discussed.

As a complement to this paper, the article, "Getting the Most Out of CMOS Devices for Analog Switching Jobs" by Ernie Thibodeaux, Electronics, December 25, 1975 is recommended reading for any analog CMOS user (reprinted in Application Note 521). This discusses the different CMOS processes used by various manufacturers, showing the performance trade-offs and particularly the different failure modes which may be encountered.

CHOOSING THE RIGHT DEVICE

A. MULTIPLEXERS: PROTECTED OR UNPROTECTED?

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A are designed for failure-proof operation in a common class of applications: any system in which the analog input signal lines originate external to the equipment. This includes most data acquisition, telemetry, and process control systems. Overvoltage protection is necessary because the signal lines are commonly subject to a number of potentially destructive situations.

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A.C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Harris protected type multiplexers will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 1000 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

Conventional CMOS multiplexers can be protected against overvoltage destruction by external resistor-diode networks to limit input current to a safe level, but it is difficult to prevent another phenomenon with overvoltage; normally-off switching elements will tend to switch on, due to parasitic bipolar transistors in the CMOS structure, so the overvoltage spike will appear at the multiplexer output. The Harris internal protection circuits eliminate the problem by automatically shutting off the parasitic transistor during overvoltage conditions.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

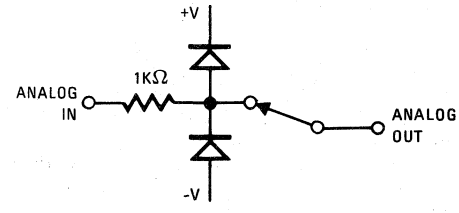


Figure 1

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions—ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 Volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. WHICH SWITCH TO SWITCH TO?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is a low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the IH-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 Volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: R(ohms) $\geq$ (V_{IN} -V_{SUPPLY}) x 50 where V_{IN} is the maximum expected input voltage. All digital inputs do have overvoltage/static charge protection.

DATA SHEET DEFINITIONS

A. ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions—conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, ANALOG SIGNAL RANGE

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown—this is not true for some other manufacturers' devices.

C. R_{ON}, ON RESISTANCE

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temp.) and to a lesser degree with signal voltage and current.

D. I_S(OFF), I_D(OFF), I_D(ON): LEAKAGE CURRENTS

Currents measured under conditions illustrated on data sheet. Harris prefers to guarantee only worst-case high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatably on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about .001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, I_D(ON) has the most effect, creating a voltage offset across the closed switch equal to I_D(ON) x R_{ON}.

E. V_{AL}, V_{AH}; INPUT THRESHOLDS

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" address inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, INPUT LEAKAGE CURRENT

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices, there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; ACCESS TIME

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, BREAK-BEFORE-MAKE DELAY

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF$, $C_D(ON)$ INPUT/OUTPUT CAPACITANCE

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, DRAIN TO SOURCE CAPACITANCE

The equivalent capacitance shunting an open switch.

K. OFF ISOLATION

The proportion of a high frequency signal applied to an open switch input appearing at the output: off isolation = 20 log $\frac{V_{IN.}}{V_{OUT}}$. This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, DIGITAL INPUT CAPACITANCE

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, POWER DISSIPATION: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

CARE AND FEEDING OF MULTIPLEXERS AND SWITCHES

Dielectrically isolated CMOS I.C.'s require no more care in handling and use than any other semiconductor—bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any I.C.. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the I.C. socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or

device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

DIGITAL INTERFACE

A. REFERENCE CONNECTION

HI-5040 through HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 Volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 Volts.

B. DTL/TTL INTERFACE

One major difference found in comparisons of similar devices from different manufacturers is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from the CMOS input to the +5 Volt supply when driving from TTL/DTL:

1. Interchangeability: allows subsititution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 Volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed I.C.'s; but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

   A 2K ohm resistor connected from the CMOS input to the +5 Volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor—the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS INTERFACE

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. ELECTROMECHANICAL INTERFACE

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).

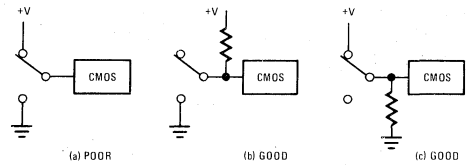


Figure 2

A PRACTICAL MULTIPLEXER APPLICATION

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial

adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. ACCURACY

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x $I_{S(OFF)}$
   b. output offset = R(ON) x ($I_{D(ON)}$ + I bias (S/H))
2. Sample-and-hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0° to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

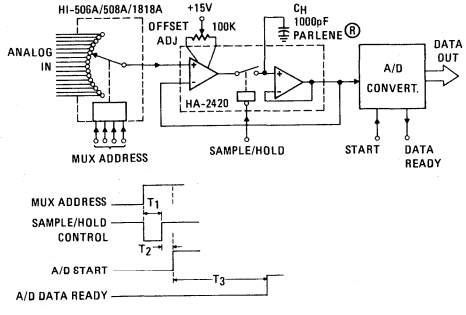


Figure 3

B. TIMING

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.

T_2 is the short interval required for the sample-to-hold transient to settle.

T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ± 10 Volt input range for acquisition/settling times to ½ L.S.B. accuracy:

	T_1	T_2
10 bit:	6μS	1μS
12 bit:	12μS	2μS

The multiplexer, by itself, requires about 2 μs and 9 μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-2600, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of

$$F_S = \frac{1}{N(T_1 + T_2 + T_3)}$$ samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{F_S}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. ADDING CHANNELS

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by

having several tiered levels of multiplexing; where the outputs of a number of MUX's are individually connected to the inputs of another MUX.

D. DIFFERENTIAL MULTIPLEXING

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

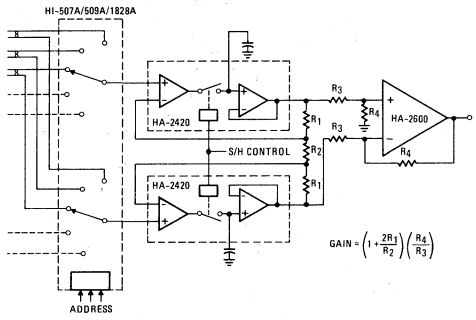


Figure 4

E. DEMULTIPLEXING

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will recreate the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

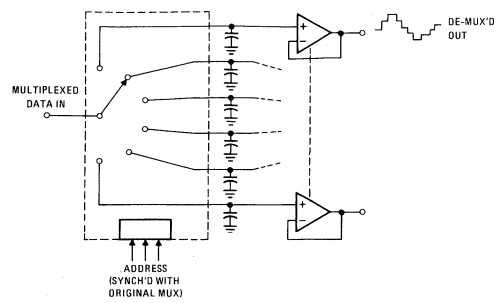


Figure 5

ANALOG SWITCH APPLICATIONS

A. HIGH CURRENT SWITCHING

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous—such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute max. derated power—quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. OP AMP SWITCHING APPLICATIONS

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6 (a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a non-inverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

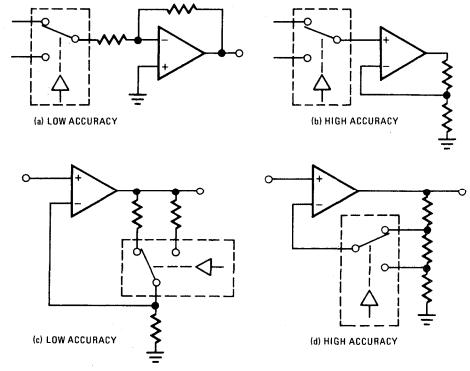


Figure 6

C. SWITCHING SPIKES AND CHARGE INJECTION

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7 (a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7 (b)).

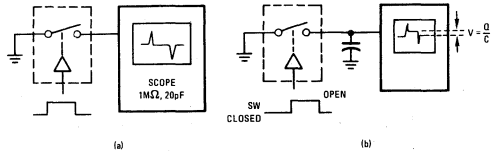


Figure 7

Charge injection is measured in pico Coulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simultaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

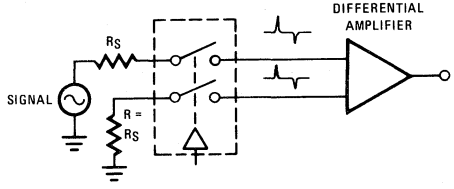


Figure 8

Among the Harris anlog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 pico Coulombs. Transients of the HI-5040 series are several times higher.

D. HIGH FREQUENCY SWITCHING

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

The 30 ohm switch types of the HI-5040 series appear to best meet these requirements, and testing at high frequencies has verified this.

Figure 9 illustrates these circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier stage; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

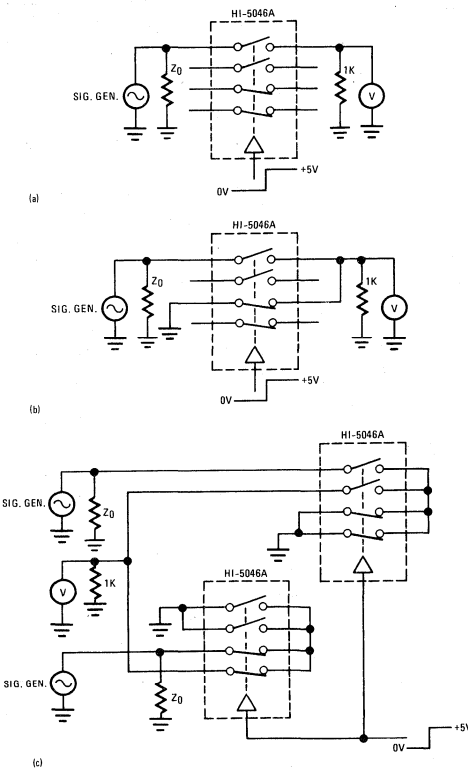


Figure 9

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the

region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which accounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

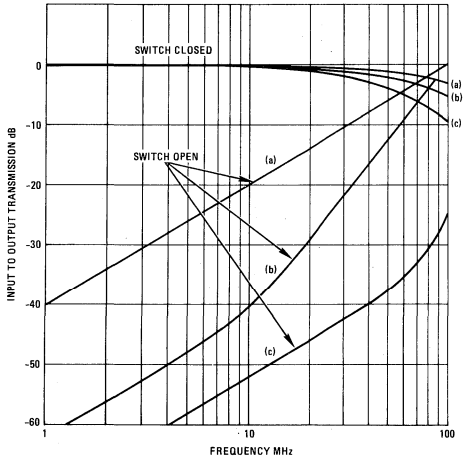


Figure 10

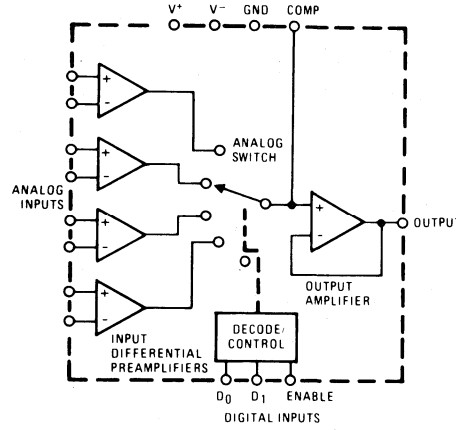
ALTERNATIVES TO CMOS SWITCHES AND MULTIPLEXERS

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

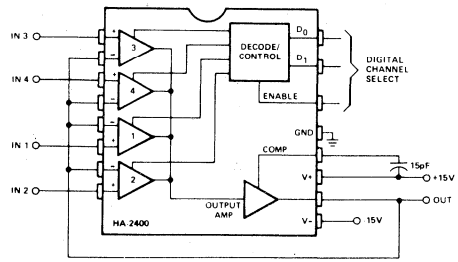
A. THE PRAM, PROGRAMMABLE AMPLIFIER

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel mulitplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 11 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

Figure 11

Advantages over a comparable CMOS multiplexer circuit are as follows:

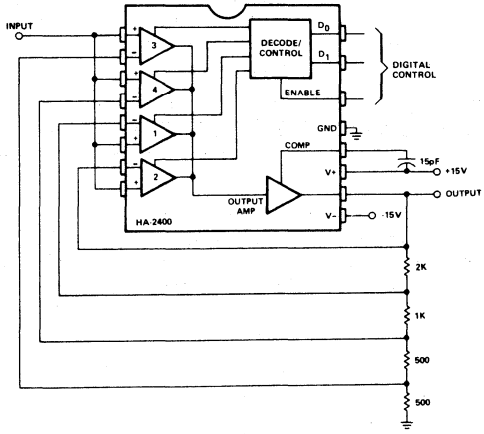
1. High input impedance (10^{12} ohms), low output impedance (< 0.1 ohm) means that ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquisition (1.5μS).

4. Wide bandwidth (8 MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tieing compensation pins together.

Figure 12 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.



AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

Figure 12

B. SAMPLE-AND-HOLD

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 13. Harris Application Note 517 illustrates many other applications.

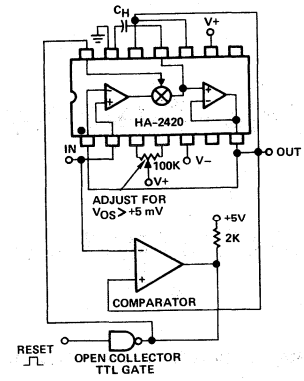


Figure 13

C. PROGRAMMABLE SUPPLY CURRENT OP AMPS

The HA-2720/2725 and HA-2730/2735 (dual amp) are op amps with an extra terminal which is used to control quiescent supply current. These are most generally used in low power systems to optimize the power dissipation vs. bandwidth and slew rate tradeoffs. They can also be used with variable set currents to make linearly variable oscillators, filters, etc. Another application is a switchable op amp as shown in Figure 14.

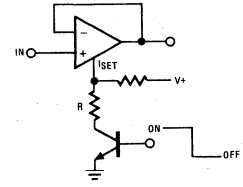


Figure 14

The illustrated transistor could be the output of high voltage open collector gate. The set resistor R is chosen so that the set current is the desired value when the transistor is ON, considering that the voltage at I_{SET} terminal when ON is about 2 forward junction drops ($\sim$ 1.5V) below V+. When the transistor is turned OFF, amplifier input, output, and supply terminals become very high impedance, so that two or more amplifier outputs could alternately be switched to the same point.

Off isolation with a 2,000 ohm load is about -80dB at 10kHz.

D. CHOPPER STABILIZED AMPLIFIER

Analog switches are sometimes used as choppers for amplifying low level D.C. signals with low offset errors. The HA-2900/2905 is a monolithic chopper stabilized amplifier in a TO-99 can. Typical offset drifts are 0.2 μV/°C and 1pA/°C with 5 x 10^8 open loop gain. Harris Application Note 518 describes this device.

HARRIS

APPLICATION NOTE
521

GETTING THE MOST OUT OF C-MOS DEVICES FOR ANALOG SWITCHING JOBS

BY ERNIE THIBODEAUX

INTRODUCTION

Although most designers appreciate the benefits of the complementary-MOS process for digital design, few realize how effective the technology can be for analog switching. C-MOS analog switches, which consume less power than bipolar devices, exhibit no dc offset voltage and can handle signals up to the supply rails. The C-MOS bilateral property furnishes input and output functions, making multiplexing and demultiplexing possible. In addition, the on-resistance of an MOS switch is as low as 30 ohms—a third as much as a bipolar device.

Unfortunately, C-MOS analog switches, which until recently were built with junction isolation, have been difficult to design into analog multiplexers and switches. The devices latched up easily, their C-MOS inputs were destroyed by electrostatic charges, and they literally went up in smoke when confronted with input overvoltage spikes and power-supply transients. To prevent destruction, costly external protective circuits were needed, and, even then, the devices latched up unless the power was turned on and off in a set sequence.

Because latch-up problems limited the use of analog switches so severely, device designers focused a great deal of attention on eliminating the condition. Recently, the success has been noteworthy. Indeed, three new technologies now offer latch-free analog switch operation: latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI).

Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing in-board analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

THE BASIC C-MOS SWITCH

The basic C-MOS transistor (Fig. 1) has parasitic junctions that are reverse-biased during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

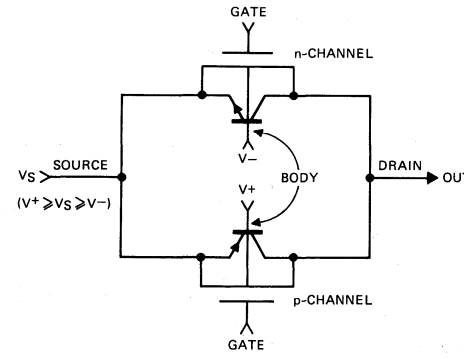


Figure 1. Bad

In the basic C-MOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch

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through the parasitic pnp transistor (Fig. 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition, which is seldom destructive, is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Fig. 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

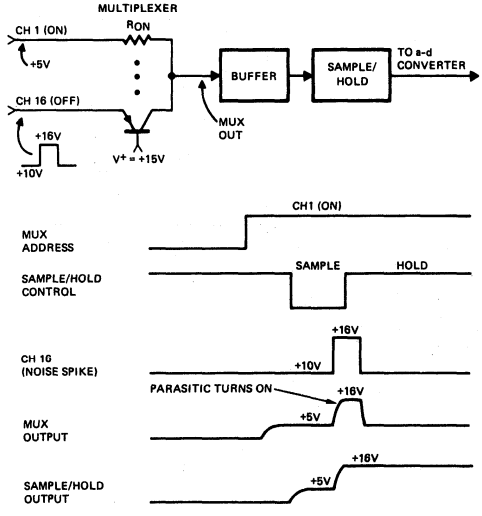

Figure 2. Worse

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Fig. 3) —a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof C-MOS devices.

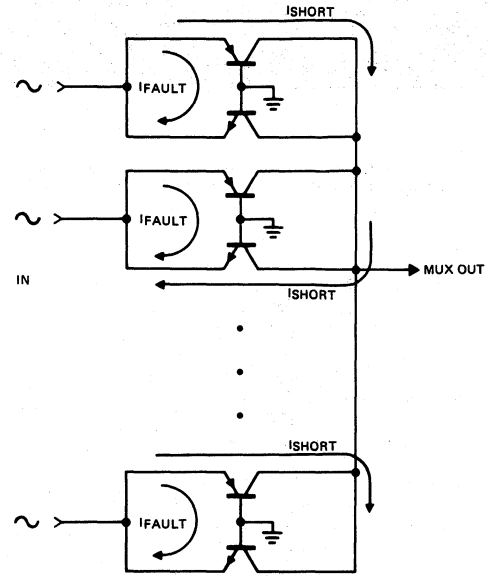

Figure 3. Still Worse

Most serious in CMOS switches is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

CONSIDERING LATCH-PROOF JI TECHNOLOGY

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Fig. 4(a) shows the C-MOS structure along with its parasitic transistors and the equivalent circuit in Fig. 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasi-dual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around the device, as shown in Fig 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the

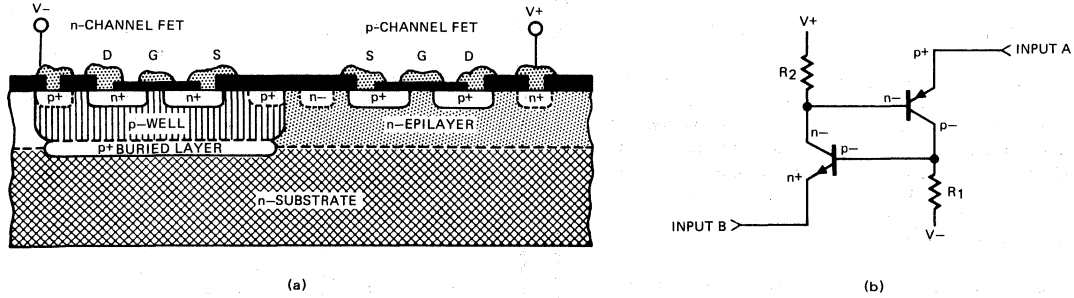

Figure 4. Latch-Proof. Junction-isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

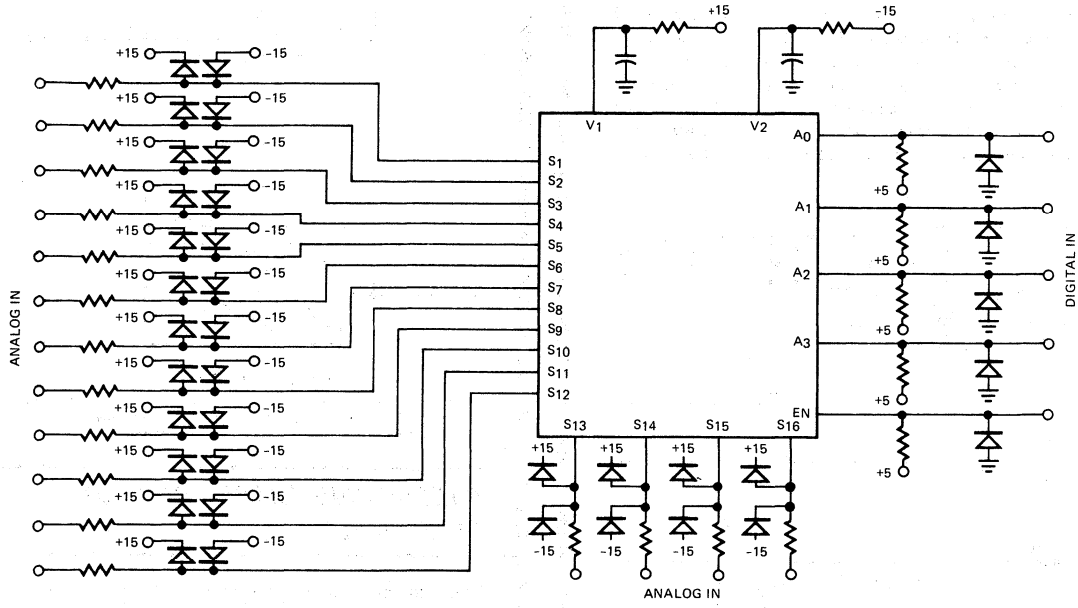

Figure 5. Protection still needed. Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage—much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes—to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements, but they cost about 50 cents each in volume, and the total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

THE FLOATING-BODY JI TECHNOLOGY

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the n-channel switching device. A cross section of this process is similar to that in Fig. 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single -gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

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To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the npn parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessary when using these devices in configurations such as single-pole single-throw, single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ± 15V supplies, as it can with other C-MOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the I_{CEO} of the floating base for the npn is much greater than the I_{CBO} of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms . The dc-offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their dc-offset error is between 0.28 mV and 1 mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Fig. 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has RL = 100 ohms is specified to be -54 decibels, which compares favorable with other types. However, at lower frequencies such as 1 kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low ac impedance of the supply voltage (Fig. 6b).

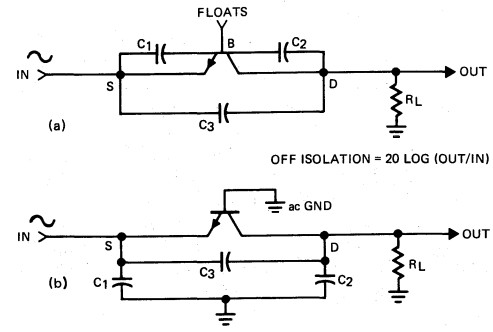

Figure 6. Floating Bodies

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

THE LINEAR DIELECTRIC-ISOLATION TECHNOLOGY

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construction ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Fig. 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer strucures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

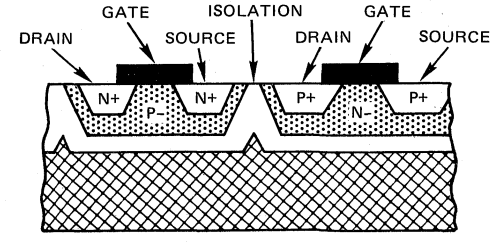

Figure 7. How DI Does It

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCR's.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some potential, or even modulate it. Fig. 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or

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substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the off state, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

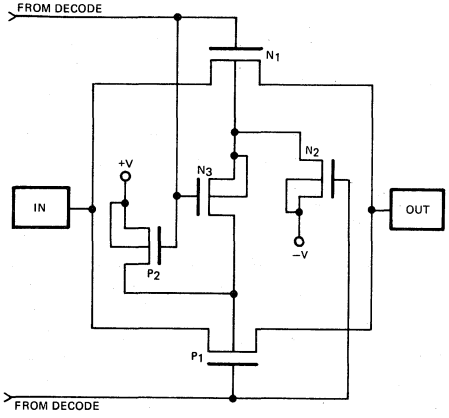

Figure 8. DI Does It

In dielectrically isolated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

DESIGNING A FOOLPROOF C-MOS ANALOG MULTIPLEXER

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Fig. 9) benefits from a combined bipolar/C-MOS technology. The illustrated bipolar section is used to sense an analog overvoltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own protection circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1 while N_3, D_4, D_5, and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

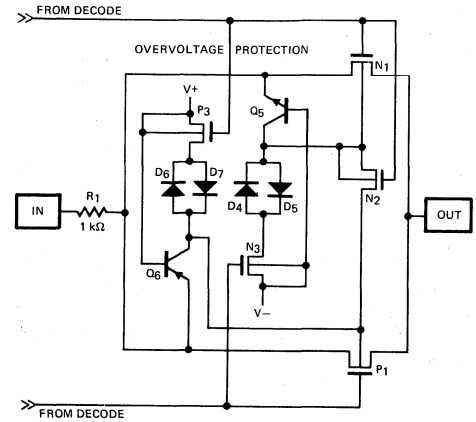

Figure 9. Winning Combination

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A, HI-507A, HI-508A, and HI-509A.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage $V_{CE(SAT)}$ of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D_6 requires an additional forward-voltage drop for conduction through the parasitic junction. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a nominal overvoltage of ±33V, reveals a cross-talk current of only about 5na (Fig. 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts (R_{ON} x 5_{NA})—certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvolt-

age. For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

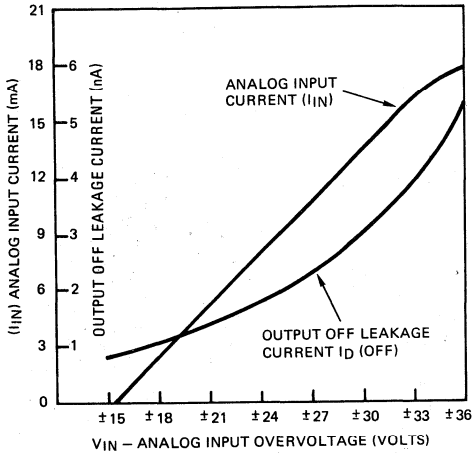

Figure 10. Blocking Cross Talk

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA—an absolute error from channel interaction of only 6 μV.

ADDING BENEFITS

RESULTS OF DIGITAL-INPUT PROTECTION TESTS (20 DIELECTRICALLY ISOLATED UNITS)	
STRESS STEP/VOLTS	FAILURES
500	0
1,000	0
1,500	0
2,000	1
2,500	0
3,000	3
3,500	0
4,000	3

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Fig. 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. The table gives the results of a step-stress analysis performed on 20 units. A total of 80% survived the 3.5 kilovolt level, and only one failed below 2kV.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/C-MOS reference circuit shown in

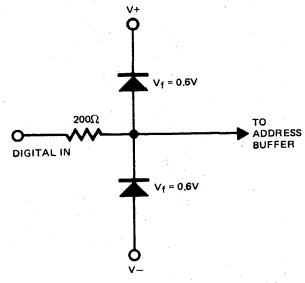

Figure 11. Digital Protection

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

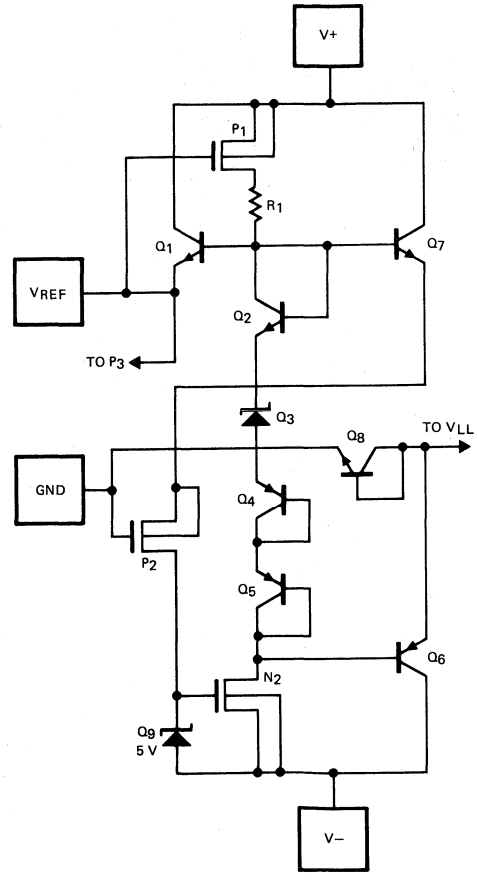

Figure 12. Packing It In

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

Fig. 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

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The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with C-MOS-logic circuits. P_1 turns off when V+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the IC's power-consumption from bipolar to C-MOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data-acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers with ±15V supplies is shown in Fig. 13. The DI device consumes only 100mW at 1 MHz to yield the best speed-power product.

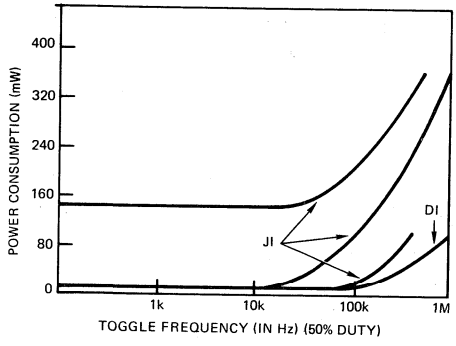

Figure 13. DI Performs

DI devices not only perform well, but do it with less power. Dynamic-power-consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

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APPLICATION NOTE 522

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

BY DICK TI TUNG

INTRODUCTION

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0 + A_{-1}2^{-1} + \ldots + A_{-n}2^{-n}$$

where the coefficients A_i (for $n \geqslant i \geqslant -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

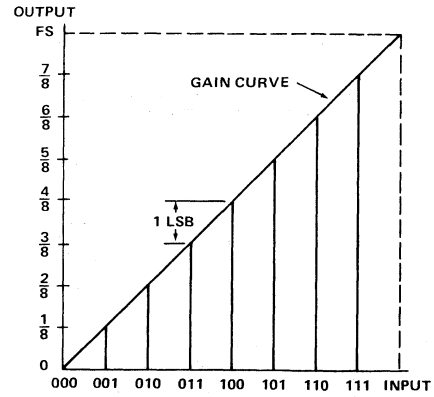

Figure 1 – Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary

code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

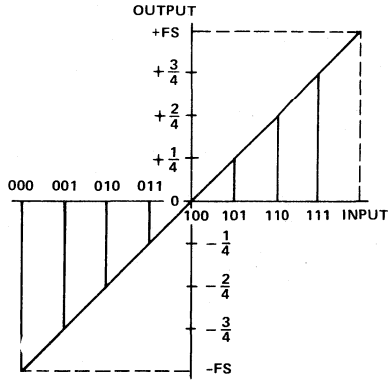

Figure 2 – Ideal Transfer Function Offset Binary (Bipolar)

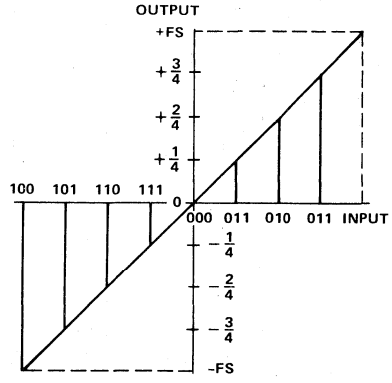

Figure 3 – Ideal Transfer Function Two's Complement (Bipolar)

TERMINOLOGY

Least Significant Bit (LSB) – The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) – The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution – An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy – A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) – A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity – A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ± 1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift – A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) – A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within $^{+}1/2$ LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

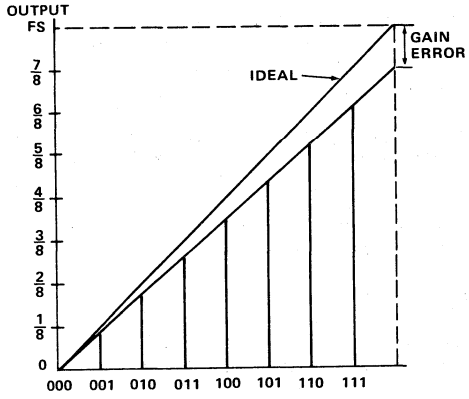

Figure 4 – Gain Error

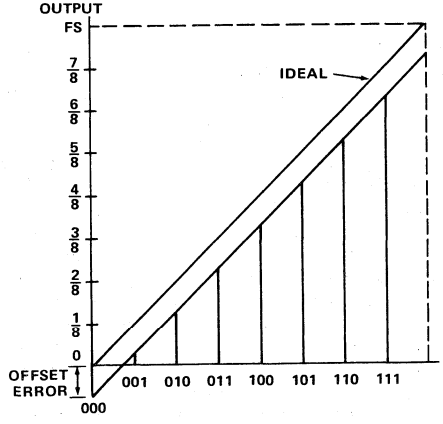

Figure 5 – Offset Error

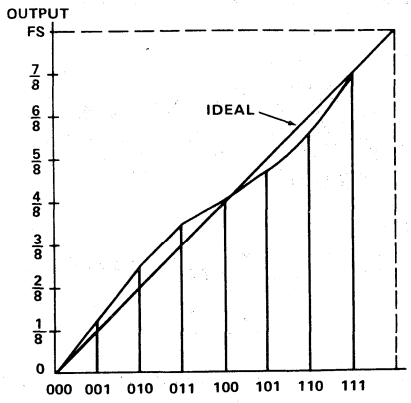

Figure 6 – Linearity Error

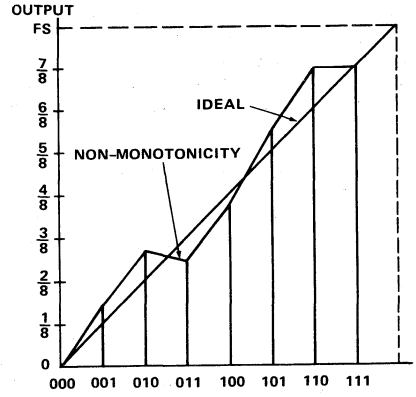

Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ≤ TA ≤ 75°C	-55°C ≤ TA ≤ 125°C
6	$FS/_{64}$	1.5620	15,625	208.3	86.8
7	$FS/_{128}$	0.7812	7.812	104.2	43.4
8	$FS/_{256}$	0.3906	3,906	52.1	21.7
9	$FS/_{512}$	0.1953	1,953	26.0	10.9
10	$FS/_{1024}$	0.0977	977	13.0	5.4
11	$FS/_{2048}$	0.0488	488	6.5	2.7
12	$FS/_{4096}$	0.0244	244	3.3	1.4
13	$FS/_{8192}$	0.0122	122	1.6	0.68
14	$FS/_{16384}$	0.00610	61	0.8	0.34
15	$FS/_{32768}$	0.00305	31	0.4	0.17
16	$FS/_{65536}$	0.00153	15	0.2	0.08

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APPLICATION NOTE
524

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

BY DICK TI TUNG

ANALOG-TO-DIGITAL CONVERTER (ADC)

The uses of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e. 2kΩ for HI-562A, produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within ± 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the ±1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

DATA ACQUISITION SYSTEM

The functional diagram of a 16-channel data acquisition system is shown in Figure 3. Functionally, the outputs of the binary counter are fed to the 16-channel analog multiplexer to serve as the channel select signals, and it is also fed to the 4 line to 16 line digital decoder as address inputs. At the rising edge of the clock pulse, an analog input channel is selected, and the sample and hold circuit (S/H) is set to sample. The duration of the "1" state of the clock pulse should be adjusted such that the output of the S/H would settle to its required accuracy. At the falling edge of the clock pulse, the S/H holds the signal level acquired during the clock "1" state, and with one gate delay time, the ADC commences its conversion. Once the conversion is completed, the $\overline{CC}$ signal from the ADC will enable the decoder to send out a decoded signal to strobe the ADC output into the proper storage register. The duration of the "0" state of the clock pulse should be adjusted to allow the proper data entry to the storage register. The next analog input channel will be acquired for the next clock period, and so on. If a 50kHz clock pulse is used, the data will be refreshed every 320μs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1μs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

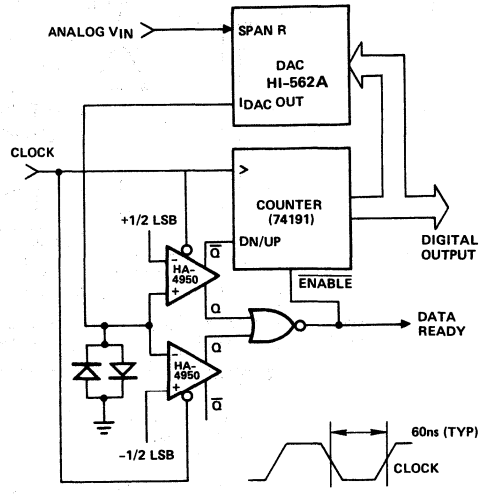


Figure 1. Tracking ADC

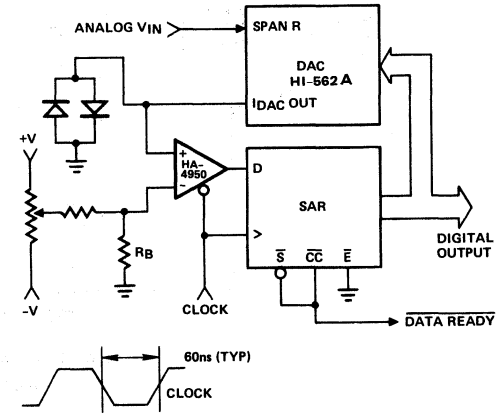


Figure 2. Successive-Approximation ADC

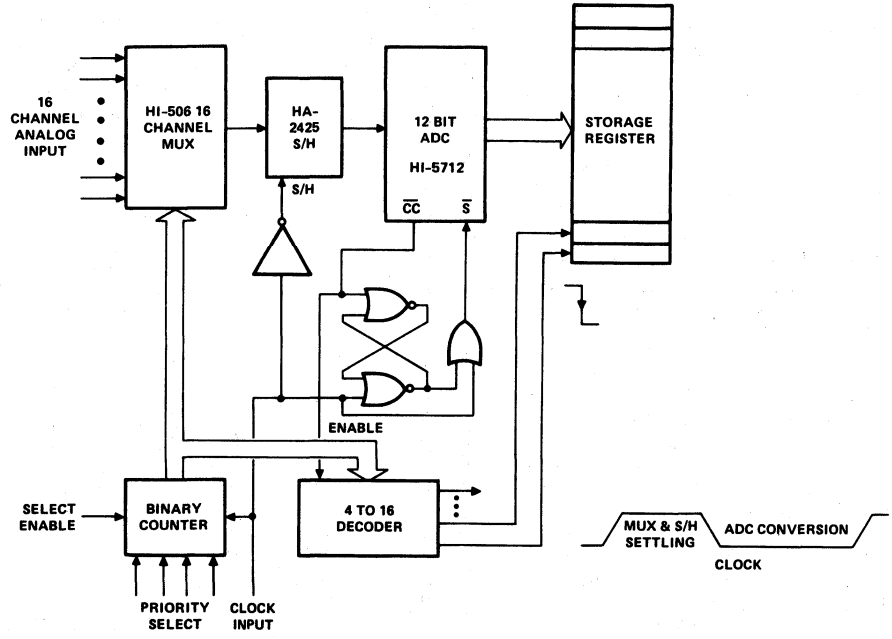


Figure 3. 16 Channel Data Acquisition System

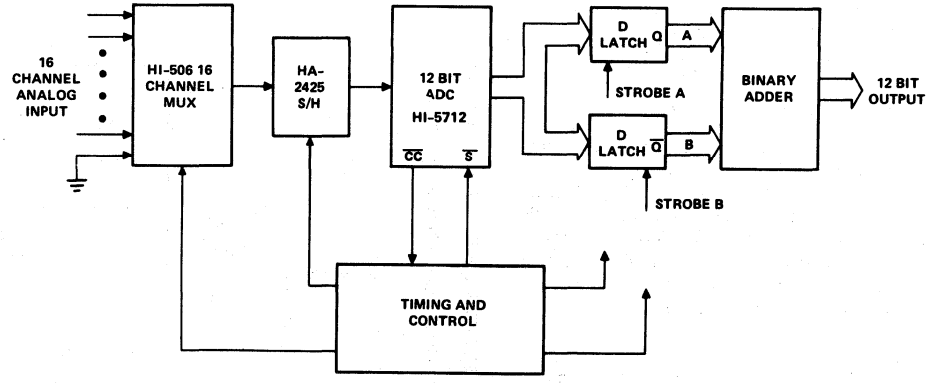


Figure 4. 15 Channel Data Acquisition System with Offset Correction

HARRIS

APPLICATION NOTE 525

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

G. COTREAU, D. JONES,
R. WHITEHEAD

INTRODUCTION

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150mHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

INSIDE THE HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

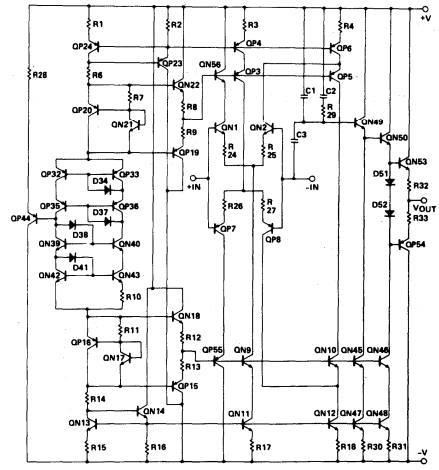


Figure 1. HA-5190/5195 Schematic.

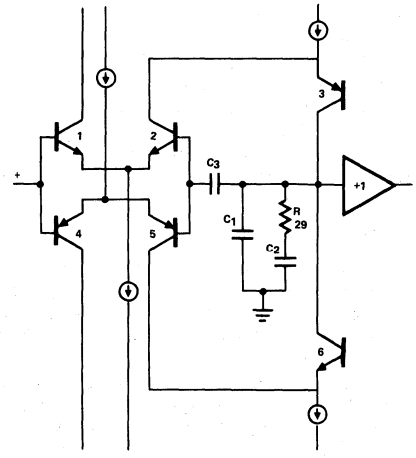


Figure 2. Simplified HA-5190 Schematic.

CONSIDERATIONS FOR PROTOTYPING

When using the HA-5190, high frequency layout techniques are recommended for bread-boarding. The device should be mounted through a ground plane. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

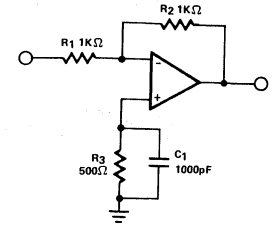
HA-5190/5195 may be used without a heat sink up to +75°C ambient. Above this temperature the power derating is 8.7mW/°C and a heat sink should be used. THERMALLOY model 6007 heat sink is recommended. For temperatures up to +125°C, the thermal resistance of the heat sink should be 30.6°C/W maximum.

FREQUENCY COMPENSATION

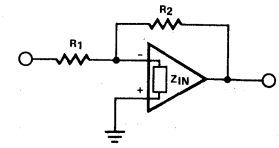
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

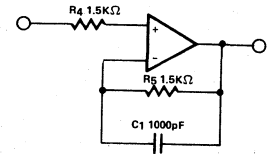
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30mHz small signal bandwidth is practical) by fine tuning component values.



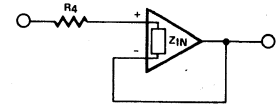
(a) Gain = -1



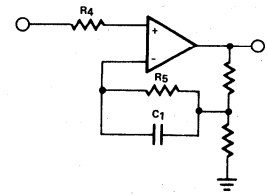
(b) Stabilization using Z_{IN}.



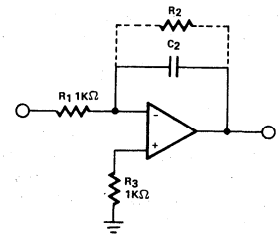
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R_2}{R_1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

SUGGESTED METHODS FOR PERFORMANCE ENHANCEMENT

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

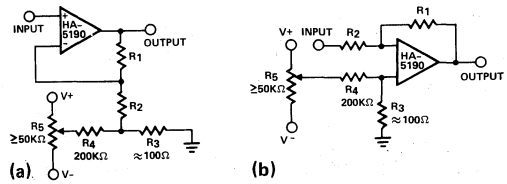
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown A_V = 5) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-2630 can drive 50 ohm coaxial cable with 10 volt peak-to-peak signals at speeds up to 200V/μs.

APPLICATIONS

INTRODUCTION

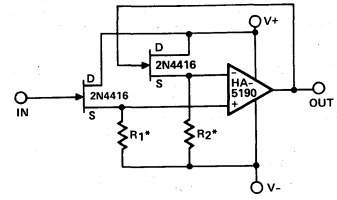
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



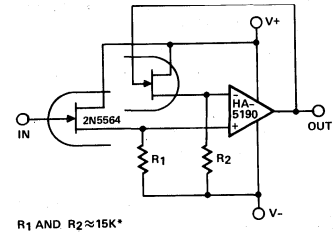
RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

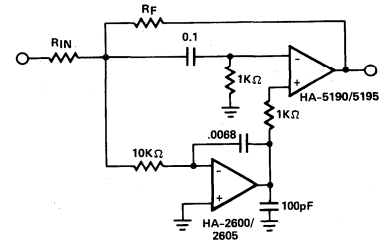
Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.



(b) R_1 AND $R_2 \approx 15K^*$
INPUT FETS ARE MATCHED PAIR 2N5564



(c)

Figure 5. Reducing Input Bias Currents.

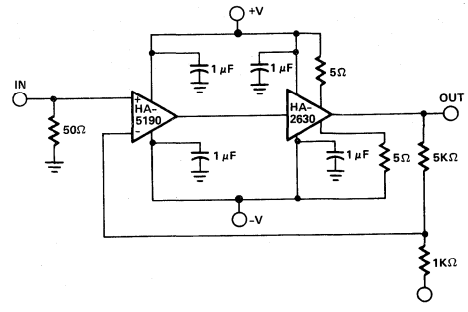


Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

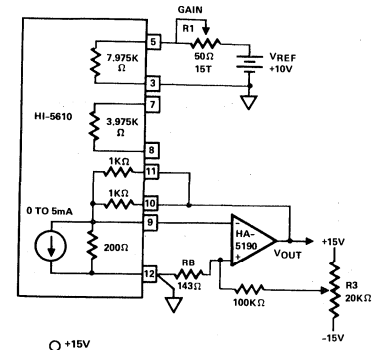
HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

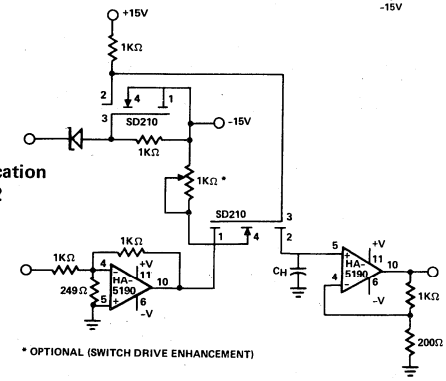
Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

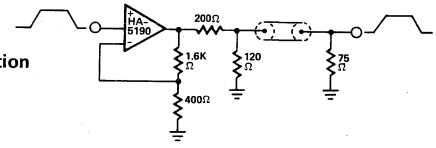
Application 1



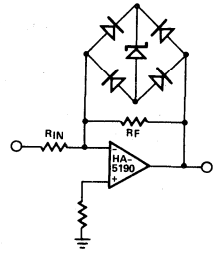
Application 2



Application 3



Application 4



HARRIS

APPLICATION NOTE 526

VIDEO APPLICATIONS HA-5190/5195

L. E. GARNER

INTRODUCTION

Offering superior performance in video and RF circuits, the HA-5190/5195 family can be used effectively in the design of television broadcast studio equipment, test instruments, and monitoring or surveillance TV systems. A very high 200V/μs slew rate, a full power bandwidth of 6.5MHz, and a fast settling time of only 70ns (typ) are but three of the unique characteristics which make these devices ideal for critical wideband video and RF applications. Other features include true differential operation, excellent stability with gains ≥ 5, and complete freedom from latch up, the latter a result of the exclusive HARRIS dielectric isolation process combined with optimized chip design and layout.

The op amp family can be used, typically, as studio tape head, test instrument, and video camera preamplifiers, as buffers, as broadcast relay link repeaters, as coaxial line drivers, and as cable or industrial system video repeater and bridging amplifiers. Extremely versatile, the devices can be operated effectively in AGC and dc gain controlled configurations as well as in fixed gain designs, and are fully capable of driving low impedance loads.

When used in standard video amplifier configurations, the HA-5190/5195 devices easily meet or exceed the performance tolerance specifications of applicable current FCC (NTSC) composite TV signal standards as well as the requirements of EIA Tentative Standard RS-170A.

VIDEO PERFORMANCE

The overall color video performance of the HA 5190/5195 family was confirmed by checking a number of standard devices. Tests were made to determine both video response and signal/noise ratio under typical operating conditions. The basic video amplifier circuit illustrated in Figure 1 was used for the tests, with the actual procedures abstracted from those described in EIA Standard RS-250-B. The general test setup is shown in Figure 2.

VIDEO RESPONSE TESTS

Referring to Figure 1, the test video amplifier comprised an HA5190/5195 op amp, BNC coaxial input jack J1, input level control R1 shunted by impedance matching resistor R2, input series stabilization resistor R3, gain control network R4-Rgain, series output limiting resistor Rs, and BNC coaxial output jack J2. Operational power was supplied by a well regulated and filtered dual line operated power supply.

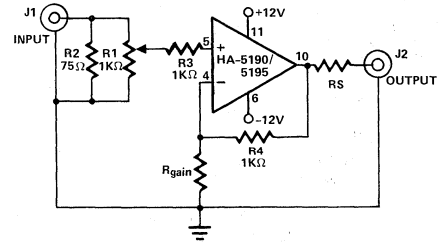


Figure 1–Test Video Amplifier

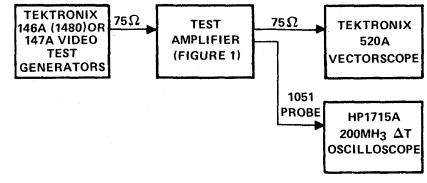


Figure 2–Video Response Test Setup

Initially, standard NTSC and EIA ramp and timing test signals were applied using the Tektronix Models 146A (1480) and 147A video test generators. Amplifier performance was observed and measured at various levels with a Tektronix 520A Vectorscope and HP Model 1715A 200 MHz delta time Oscilloscope. Three of the RS-250-B specified test waveforms used are illustrated in Figure 3, including the (a) ramp linearity, (b) 12.5T and 2T sine-squared pulse and bar, and (c) multiburst signals. With the test signal level maintained at 1.0V p-p, level control R1 was adjusted as needed to establish a 1.0V p-p output signal (at J2) for each gain value. The Vectorscope was used to measure color differential phase and gain, with the Oscilloscope used to check for distortion of the 2T, 12.5T, multiburst and color bar signals. The average test results are summarized in Table A. All measured values were well within applicable specifications.

Table A - Summary of Test Results

NOMINAL GAIN	R_{gain}	R_s	DIFF Φ	DIFF GAIN	2T	12.5T	MULTI	COLOR BARS
1	∞	0	-0.2°	-0.5%	UNM*	UNM*	FLAT	UNM*
2	1k	75Ω	-0.15°	≈0	UNM*	UNM*	FLAT	UNM*
5	251Ω	200Ω	-0.2°	≈0	UNM*	UNM*	FLAT	UNM*
10	110Ω	200Ω	-0.4°	-0.5%	UNM*	UNM*	FLAT	UNM*

*UNM : UNMEASURABLE DISTORTION

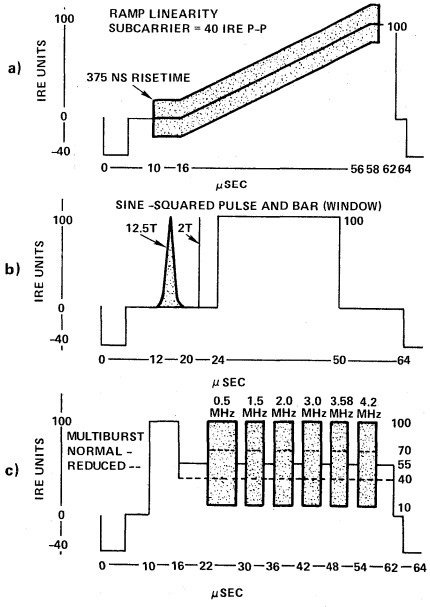


Figure 3—Video Test Signal Waveforms

S/N RATIO

Signal/noise (S/N) ratio measurements were made using the same basic amplifier configuration, but with Rgain fixed at 251Ω, ±1%, and Rs at 200Ω ±5%. The dc power supply terminals were bypassed with a 100 μF tantalum capacitor. A Tektronix 147A NTSC Test Signal Generator was used as a signal source, with output measurements made using a Rhode & Schwartz Video Noise Meter, as diagrammed in Figure 4. The Tektronix 147A was set to deliver a flat field signal at 50 IRE units, with the R&S Video Noise Meter adjusted as follows: (a) 10kHz High pass, (b) Video Bandpass, (c) Subcarrier Trap OFF, (d) Internal Sync, (e) Tilt & Sag Comp OFF.

Under the specified conditions and with level control R1 adjusted to deliver a 1.0V p-p signal at J2, the measured p-p signal/RMS noise ratio averaged 68dB, or well over the minimum value required by applicable standards.

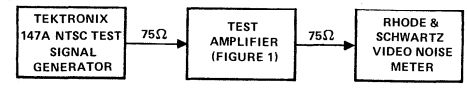


Figure 4—S/N Ratio Test Setup

GENERAL CONSIDERATIONS

Since the HA-5190/5195 devices do not require special treatment, optimum video performance can be achieved by observing standard high frequency design and wiring practices. However, the following suggestions, abstracted in part from HARRIS Application Note 525, should prove helpful when developing practical designs.

POWER SUPPLY REQUIREMENTS

A well-regulated, well-filtered dual dc power source is required for best operation, for the op amps draw moderate currents during normal operation. Although not essential in all applications, it is recommended that the power supply lines be decoupled using 0.01 μF ceramic capacitors to circuit ground, with the capacitors located as near to the amplifier terminals as possible to minimize lead inductances. For optimum performance and operation at specified parameters, the dc power supply should furnish not less than ±10V dc, with higher source voltages (±15V, typically) preferred.

TEMPERATURE CONSIDERATIONS

The HA-5190/5195 devices can be used without heat sinks at ambient temperatures up to 75°C. Under these conditions, the internally generated heat stabilizes device operation and ensures relative immunity

to external temperature variations. At ambients above 75°C, however, the devices should be derated at 8.7mW/°C, with a suitable heat sink, such as a THERMALLOY Model 6007, used to provide adequate heat dissipation. At temperatures up to +125°C, the thermal resistance of the heat sink should be no greater than 30.6°C/W.

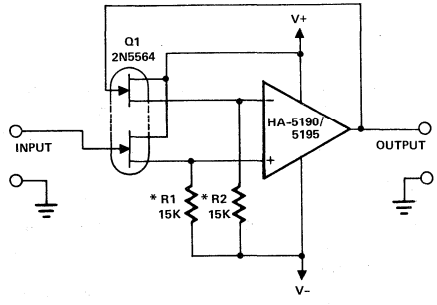
Under some conditions, the internally generated heat can affect other components. Therefore, avoid mounting temperature sensitive devices or components near or directly adjacent to the op amps.

DESIGN HINTS

Except for their exceptional performance specifications, the HA-5190/5195 devices are essentially standard op amps and may be treated as such by the video equipment or system designer. Thus, conventional design techniques may be used when developing specific circuit configurations, as long as maximum ratings are observed and adequate compensation is made for device operational characteristics. For example, the closed loop performance (dc and ac) at gains ≥ 5 depends on both the feedback component ratio and the actual impedance at each amplifier input. Since the devices offer a comparatively low input impedance, feedback network resistor values should be 5k or less (preferably, less than 1k) for optimum high frequency performance.

If the intended video application requires a high input impedance, a FETpreamp stage may be added ahead of the HA-5190/5195 op amp, as shown in Figure 5. Full details and an additional FET input circuit are provided in HARRIS Semiconductor Application Note 525.

Where used, a FET preamp not only raises the effective input impedance from (approximately) 10k to thousands of megohms, but also reduces the input bias current requirement by several orders of magnitude. There is, of course, a trade-off in frequency response, with a FET input stage reducing the effective overall slew rate from 200V/μs to 130V/μs (typically). However, the full power bandwidth with a FET input is more than adequate for all low to mid level video applications.



*Approximate Values

Figure 5– FET Input Circuit

Some video applications may require output currents which exceed the maximum capabilities of the HA-5190/5195 devices. In these cases, the HA-5190/5195 op amps can be teamed with high performance current boosters such as, for example, the HA-2630/2635 devices. A typical cascaded op amp/booster circuit is illustrated in Figure 6. Since the current booster, a unity gain device, has a typical slew rate and bandwidth (Slew rate 500V/μs, BW 8.0MHz) far greater than that of the op amp, the overall frequency performance of the composite amplifier is essentially that of the op amp alone.

To compensate for manufacturing tolerances and ensure optimum performance, the fixed component values used in specific designs should be finalized empirically, using active devices from several production runs.

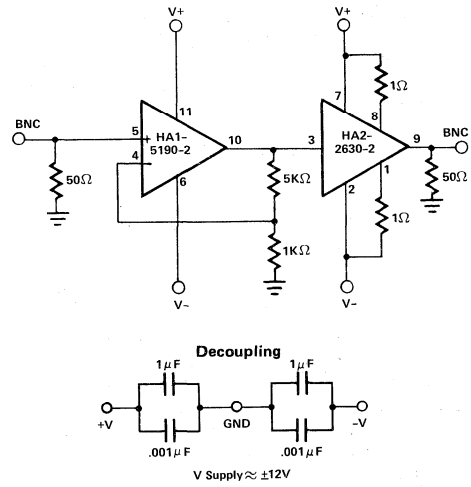


Figure 6–Boosting Output Current

PROTOTYPING TIPS

In accordance with standard engineering practice, new circuit designs should be breadboarded to verify overall operation. Afterwards, a number of preproduction prototypes identical to the planned production design should be assembled and tested using active devices from several production runs. These prototype tests permit optimization of component values and determination of circuit sensitivities to layout and component positioning. Preliminary environmental tests, if required, also may be made using the prototypes.

If IC sockets are used, Teflon types are preferred to minimize distributed capacitances. For the same reason, feedback components should be mounted between Teflon insulated standoffs located as close as practicable to the device pins or socket terminals. For maximum stability, film type resistors are recommended for the feedback networks.

Signal carrying leads should be kept short and direct, of course, to minimize both lead inductances and distributed capacitances. The devices should be mounted through a ground plane cr, if this is impracticable, single point grounding should be used to avoid ground loops.

TYPICAL APPLICATIONS

The test circuit given in Figure 1 may be used as a general purpose video amplifier, although minor changes in component values may be needed to optimize operation for specific requirements. Additional practical circuits are illustrated in Figures 7 and 8.

RF AGC AMPLIFIER

Designed and checked as a buffer for the head preamp of a studio video tape recorder, the circuit shown in Figure 7 functions as a wide band adjustable AGC amplifier. With an effective bandwidth of approximately 10 MHz, it is capable of handling RF input signal frequencies from 3.2 to 10MHz at levels ranging from 40mV up to 3V p-p.

AGC action is achieved by using opto coupler/isolator OCl as part of the gain control feedback loop. In operation, the positive peaks of the amplified output signal drive the OCl LED into a conducting state. Since the resistance of the OCl photosensitive element is inversely proportional to light intensity, the higher the signal level, the lower the feedback resistance to the op amp inverting input and hence the greater the negative feedback, thereby lowering stage gain. Any changes in gain occur smoothly because the inherent memory characteristic of the photoresistor acts to integrate the peak signal inputs. In practice, the stage gain is adjusted automatically to a point where the output signal positive peaks are approximately one diode drop above ground.

GAIN SET control R5 applies a fixed dc bias to the op amp non-inverting input, thus establishing the steady-state zero input signal current through the OCl LED and determining the signal level at which AGC action begins. In experimental tests under large signal conditions (i.e., E_{IN} = 3V p-p), a GAIN SET value of -0.26V provided unity gain, while a value of -1.55V yielded on A_V of 2.7 , with a flat response to 5.0MHz at both levels. Under small signal conditions (i.e., E_{IN} = 40mV), gains from 8 to 50 could be achieved as the GAIN SET value was adjusted from 0.65V to -80mV. At A_V = 8, the frequency response was flat to 5MHz, while at A_V = 80, the response was limited to that of the HA-5190/5195.

The effective AGC range depends on a number of factors, including individual device characteristics, the nature of the RF drive signal, the initial setting for R5, et al. Theoretically, however, the AGC range can be as high as 4000:1 for a perfect op amp, for the OCl photoresistor can vary in value from 1 Megohm with the LED dark to 250Ω with the LED full on.

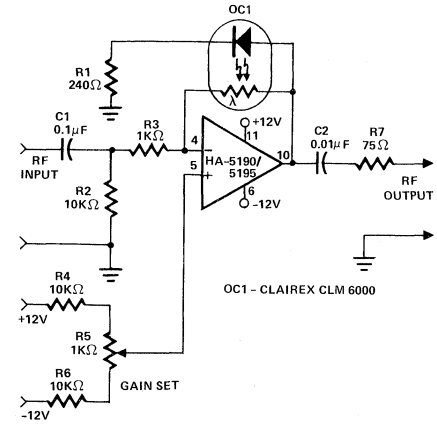


Figure 7–RF AGC Amplifier

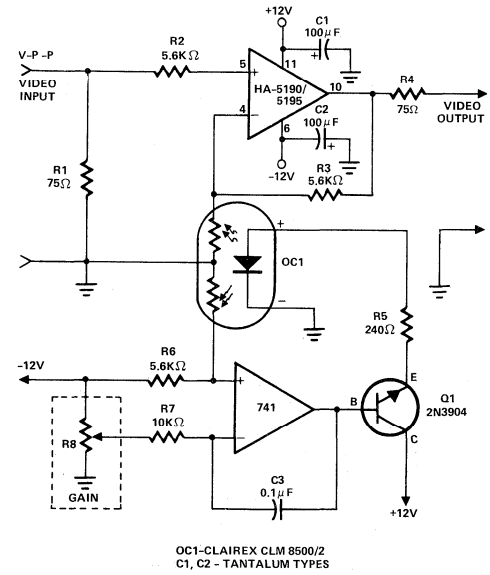


Figure 8–DC Gain Controlled Video Amplifier (Analog Multiplier)

DC GAIN CONTROLLED VIDEO AMPLIFIER

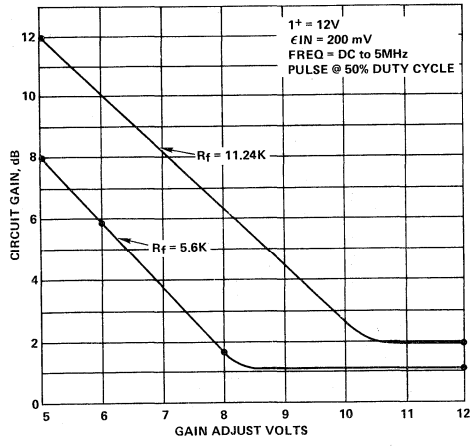
Suitable for use in virtually any application requiring a variable gain wideband or video amplifier, the circuit illustrated in Figure 8 employs a cascaded op amp integrator and transistor buffer (Q1) to drive the amplifier gain control element. Except for a simple modification, the HA-5190/5195 stage is connected as a conventional non-inverting operational amplifier, and includes input and output impedance matching resistors R1 and R4, respectively, series stabilization resistor R2, and power supply bypass capacitors C1 and C2. The circuit differs from standard designs in that the gain control network includes a photoresistor, part of OCl.

Referring to the schematic diagram, opto coupler/isolator OCI contains two matched photoresistors, both activated by a common LED. The effective resistances offered by these devices is inversely proportional to the light emitted by the LED. The greater the current through the LED, then, the more intense its light emission, and the lower the effective values of the photoresistors. One photoresistor is part (with R3) of the HA-5190/5195 gain network, while the other forms a voltage-divider with R6 to control the bias applied to the integrator non-inverting terminal.

In operation, the dc voltage supplied by GAIN control R8 is applied to the integrator inverting input terminal through input resistor R7. Depending on the relative magnitude of the control voltage, the integrator output will either charge or discharge C3. This change in output, amplified by Q1, controls the current supplied to the OCI LED through series limiting resistor R5. This action continues until the voltage applied to the integrator non-inverting input by the R6-photoresistor voltage divider matches the control voltage applied by R8 to the inverting input. At the same time, of course, the ratio of the R3-photoresistor gain network is changing, adjusting the op amp stage gain. As the control (R8) voltage is readjusted, the OCI photo-resistances track these changes, automatically readjusting the op amp gain in accordances with the new control voltage setting.

In experimental tests with typical devices, the amplifier gain could be varied from 12dB to 2dB as the dc control voltage was changed from 5.0 to 10.5Volts. Typical plots of stage gain (A_V) versus control voltage (V) are shown in Figure 9.

Since all temperature sensitive components are inside the integrator feedback loop, the circuit is quite stable with respect to changes in the ambient temperature.



ACKNOWLEDGEMENTS

A. J. Carl Cooper of HARRIS CVS (Consolidated Video Systems), 1255 E. Arques Ave., Sunnyvale, CA. 94086, developed the basic circuits described herein and, in addition, devised and executed the initial evaluation and performance tests.

B. Richard Whitehead and Robert Junkins of HARRIS SEMICONDUCTOR, P.O. Box 883, Melbourne, Fla. 32901, carried out additional confirmation tests of circuit performance and made other significant contributions to this publication.

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1. HA-5190/5195 Wideband, Fast Settling Operational Amplifiers (Harris data brochure)

2. Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier. May 1979.

3. EIA STANDARD RS-170A - Color Television Studio Picture Line Amplifier Output.

4. EIA STANDARD RS5-250-B - Electrical Performance Standards for Television Relay Facilities.

HARRIS

APPLICATION NOTE 527

APPLYING THE HI-5900 ANALOG DATA ACQUISITION SIGNAL PROCESSOR

BY JOHN E. SULLIVAN

INTRODUCTION

The HI-5900 Analog Data Acquisition Signal Processor is a powerful building block for use in a Data Acquisition Subsystem (DAS), or in stand-alone operation. Incorporating a differential analog multiplexer, a programmable gain instrumentation amplifier and track and hold amplifier, the HI-5900 is an ideal signal conditioning element for a wide range of commercial, industrial and military applications.

FUNCTIONAL OPERATION OF THE HI-5900

As illustrated in Figure 1, the HI-5900 incorporates three primary components. An input multiplexer controls selection of the signal to be processed, the programmable gain instrumentation amplifier provides common mode signal rejection and gain while the track and hold amplifier stores the instantaneous signal level for final signal processing. Signal acquisition, including multiplexer, amplifier, and track and hold settling times, is less than 10μs to 0.01% accuracy.

The multiplexer selects one of eight possible differential analog input signals to be processed, or it can be disabled to the high impedance state. All analog input lines have full overvoltage protection and can tolerate inputs up to 20 volts in excess of the power supply voltages for extended periods and transient spikes up to several hundred volts.

Expansion lines, MUX OUT A and MUX OUT B, can be used either to expand the number of input channels or as monitor outputs. The multiplexer exhibits a nominal 2 kilohm ON resistance; therefore, when using MUX OUT A or MUX OUT B as monitor points, a high impedance monitor (> 1 megohm) should be used to minimize loading affects.

Select lines A_0, A_1 and A_2 operate in binary mode (000 selects channel 1 and 111 selects Channel 8). The enable line, when LOW, DISABLES the multiplexer and forces its output to the high impedance state. Both the select and enable lines have an operating range of V- to +0.8 volts for a logic 0 input and 4 volts to V+ for a logic 1 input. When driving these inputs with TTL logic, a 1K ohm pullup resistor is recommended to ensure proper switching. All unused inputs (both signal and control) can be hardwired to either V- or ground for a logic 0 and +5 volts (V_{CC}) or V+ for a logic 1.

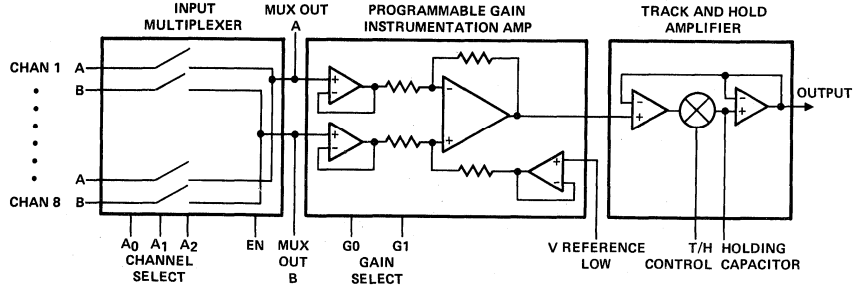

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The programmable gain instrumentation amplifier (PGA) operates in the true differential mode with A input signals being inverted and B input signals being noninverted. Some applications will have true differential input signals with an infinite impedance to ground. These applications should incorporate a 5 megohm resistor to ground from both the MUX OUT A and MUX OUT B outputs to allow amplifier bias currents to flow to ground.

The PGA has digitally selectable gains of 1, 2, 4 and 8 in binary format (00, G = 1; 11, G = 8). The digital control levels are identical to those of the input multiplexer, and as such require 1k ohm pullup resistors when driven from TTL logic.

The V_{REF} LOW line can be tied to ground or used for offset nulling as illustrated in Figure 2. Other configurations such as level shifting or quasi-differential outputs can also be implemented as shown in Figure 5.

TRACK AND HOLD AMPLIFIER

The track and hold amplifier stores and holds the instantaneous signal level applied to its input when the T/H line goes to a logic 1. The T/H mode control is fully TTL compatible and requires no pullup resistor, with the track mode defined as -5 to +0.8V and the hold mode defined as +2 to +7 volts.

An external holding capacitor (typically 1000pF to minimize pedestal errors and droop rate) is used to store the signal level while in the hold mode. This capacitor should be selected for minimum dielectric absorption and leakage as found in Teflon or polystyrene types. As shown in Figure 3, the acquisition time vs. accuracy vs. droop rate is a function of the value of the holding capacitor, and can be chosen to optimize any one parameter for a given application.

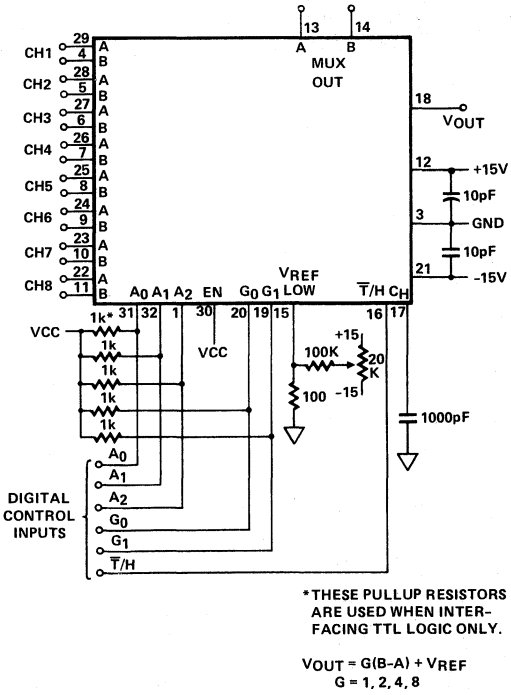

FIGURE 2 – TYPICAL CONFIGURATION

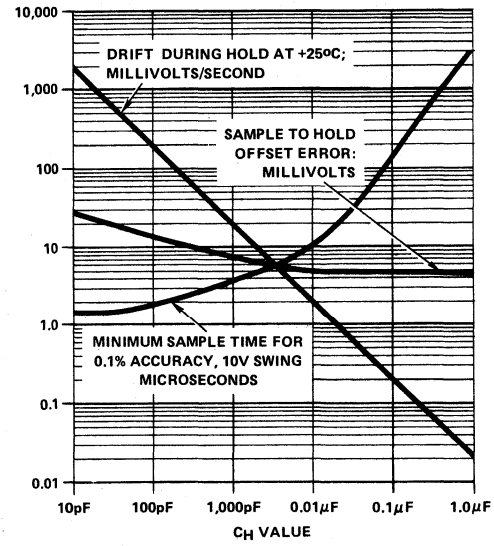

FIGURE 3 – TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE.

APPLICATION HINTS

1. Expanding the Channel Capacity of the HI-5900

Figure 4 illustrates a typical HI-5900 with its channel capacity increased from 8 to 16 channels. Further expansion can easily be implemented by adding more address lines (each additional address line doubles the channel capacity) and the required control logic to enable each multiplexer.

2. The HI-5900 in a Two-Chip DAS

The HI-5900, when teamed with the HI-5712 A/D converter as illustrated in Figure 5, will provide a two-package DAS with 12-bit accuracy and a 50kHz throughput rate. The gain selection of the HI-5900 gives this system a dynamic range of 15 bits.

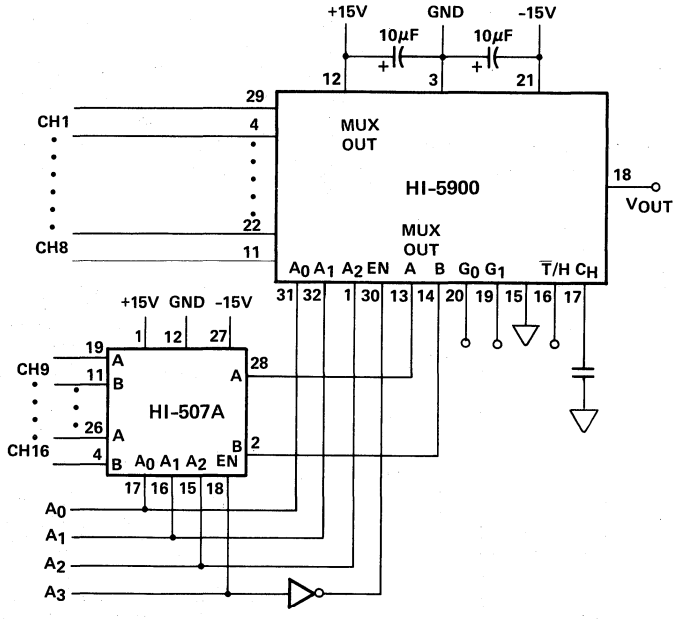

FIGURE 4 – EXPANDING THE HI-5900 TO 16 INPUT CHANNELS.

SELECTED CHANNEL	A_3	A_2	A_1	A_0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

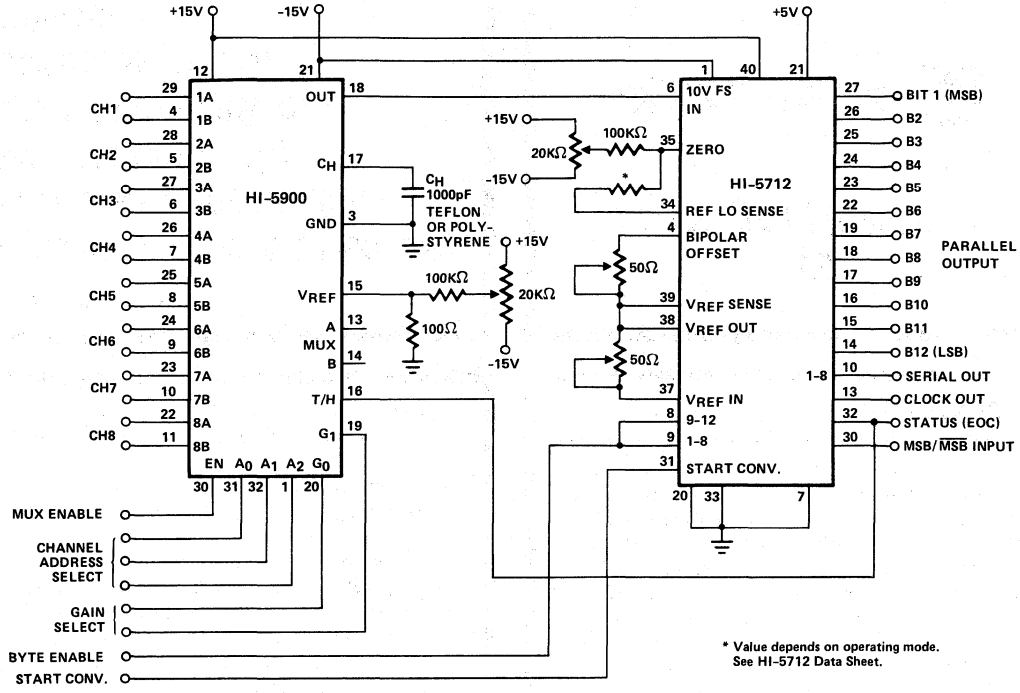

FIGURE 5 – DATA ACQUISITION SYSTEM (USING ONLY TWO PACKAGES).

HARRIS

APPLICATION NOTE 528

INTERFACING MICROPROCESSORS AND MICROCOMPUTERS WITH HI-5712/HI-5722 HIGH PERFORMANCE 12-BIT ANALOG-TO-DIGITAL CONVERTER*

BY JOHN E. SULLIVAN

INTRODUCTION

The microprocessor, with its inherent ease of use, flexibility, and numerical computing capability, has become a powerful tool for control and processing in a host of commercial, industrial and military applications. This tool, however, has had limited success in those applications interfacing the real world of analog signals. Until recently the Analog to Digital Converter (ADC), which is the analog input interface to the microprocessor, has only fulfilled part of this function. Various devices are available to easily interface the input analog signal, but require massive support to interface with the microprocessor. This "extra" interface support not only increases the overall system cost and complexity, but also reduces flexibility. The development of the HI-5712, 12 bit high performance analog to digital converter solves these and other problems by providing both an analog and microprocessor interface in a compact dual-in-line package. An LSI circuit performs all logic and interface functions while the balance of the device performs analog processing. Packaged in the unique Leadless Chip Carrier (LCC) - Hybrid form, the HI-5712 provides all the functions required to interface an analog signal to a microprocessor.

DIGITAL INTERFACE

The successive approximation conversion technique is used in the HI-5712, as illustrated in Figure 1. The Successive Approximation Register (SAR) contains all of the digital interface and control logic for conversion and interface control. Constructed using a modified CMOS process (SAJI), the SAR combines the best features of CMOS and TTL logic. All input or output lines are fully TTL/CMOS/NMOS compatible, with inputs having low loading, and outputs providing 3.2mA of sink current in the active mode and less than 25μA loading in the three state mode. All outputs are of a three state design. Data output lines are enabled with a combination of chip enable and three state enable lines, while all other outputs are enabled using only the chip enable line.

The output is structured in byte format with the most significant eight bits enabled by the enable bit EN 1-8 control line, and the least significant four bits enabled by the enable bit EN 9-12 control line. For 8-bit bus applications, the SAR 8-bit output bus can be hardwired in parallel with the SAR 4-bit output bus, eliminating the need for external drivers (see Figures 2 and 3). The fast enable/disable time (typically 60ns) of the output drivers, and their low loading characteristics minimize system integration problems for applications using unbuffered microprocessor buses (Figure 3).

The input architecture of the SAR, provides for real-time program control of analog signal conversion. Two control lines, SHORT CYCLE A and SHORT CYCLE B, control the conversion process. Conversion of 6, 8, 10 or 12-bit analog signals can be configured as per Table 1. The output format, either binary or twos complement is controlled with the MSB/MSB select line. These control lines are all internally latched into the SAR command register on the falling edge of the START CONVERT signal. These input lines can be hardwired to V_{CC}, ground or directly connected to the microprocessor for dynamic program control as illustrated in Figure 3.

TABLE 1

SHORT CYCLE A	SHORT CYCLE B	CONVERSION RESOLUTION
0	0	6 Bits
1	0	8 Bits
0	1	10 Bits
1	1	12 Bits

*Refer to the HI-5722 "PREVIEW" data sheet.

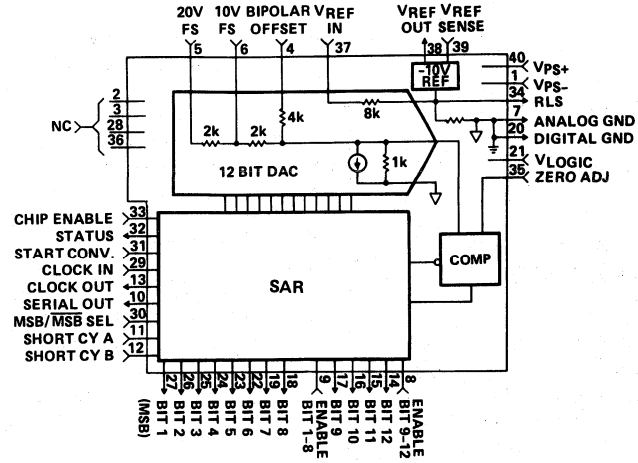

FIGURE 1 – HI-5712 FUNCTIONAL BLOCK DIAGRAM

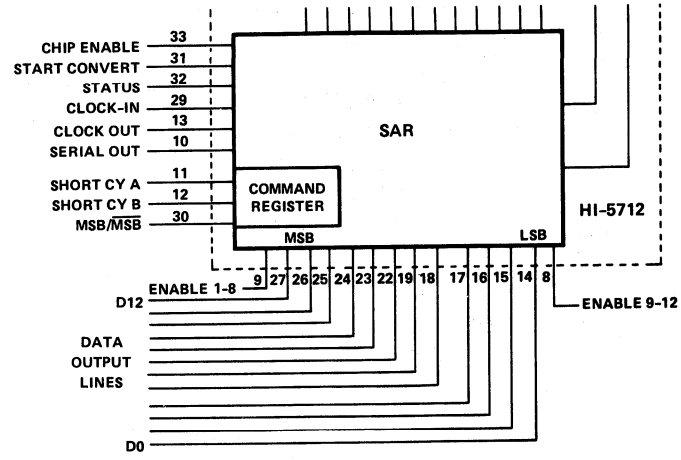

FIGURE 2 – HI-5712 DIGITAL INTERFACE

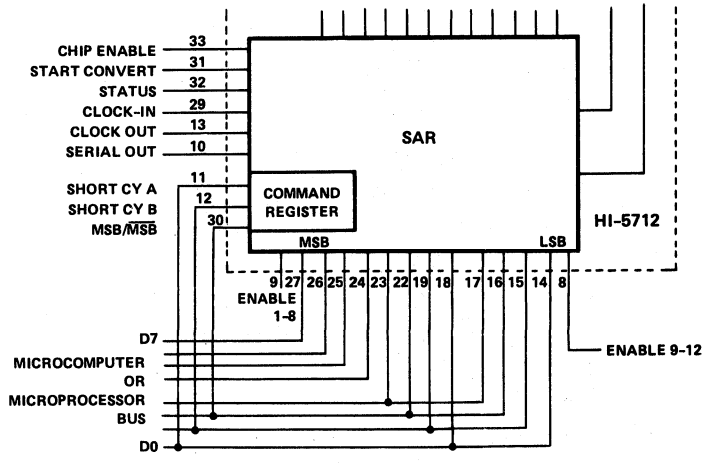

FIGURE 3

Systems requiring serial data transfer can use the serial output data port and clock output to transfer error-free data over twisted pair lines. The SAR also contains an external clock input for those applications requiring external clock synchronization. The balance of the HI-5712 contains analog processing and conditioning circuits for conversion of the input signal.

MICROCOMPUTER INTERFACE

Microcomputer systems using the HI-5712 ADC, unlike other converters, usually require no additional parts for optimum performance. Figures 4 and 5 show interfaces with the Intel 8748 and Motorola 6801 microcomputers. These examples are also applicable to most currently available microcomputers.

Four microcomputer control lines along with the microcomputer bus satisfy all of the interface requirements. Two of the control lines control the flow of data onto the microcomputer bus. The remaining two control lines start ADC conversion and interrupt the microcomputer when data is available. As discussed previously, the command register lines, the four least significant ADC data lines, and the eight most significant ADC data lines are wired in parallel to the microcomputer bus or port. This configuration typically utilizes less than 10% of the bus or port drive capability, allowing connection of additional peripheral support chips, and eliminating the need for buffer or driver devices.

The simplicity of the hardware interface correlates directly with minimal software requirements. The software flowchart in Figure 6 illustrates typical operation. The control word to the HI-5712 need only be applied during the falling edge of the START CONVERT line.

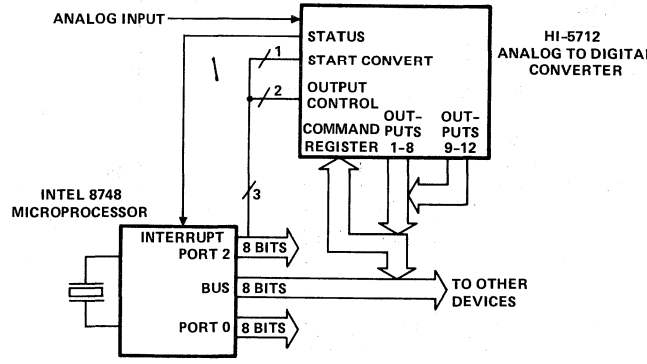

FIGURE 4 – INTEL 8748 MICROCOMPUTER INTERFACE WITH HI-5712 ADC

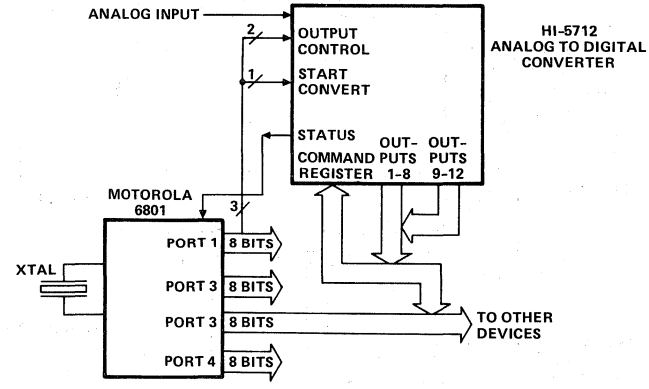

FIGURE 5 – MOTOROLA 6801 MICROCOMPUTER INTERFACE WITH HI-5712 ADC

After meeting the minimum required set-up and hold timing, the data can be removed, freeing the bus for other functions. When the microcomputer receives the interrupt signal, signaling data available, data is then read in two bytes. Since reading of the data is nondestructive, the order of reading can be configured to minimize software requirements.

These microcomputer interfaces, although deceivingly simple, will operate at up to 100kHz throughput rates. At these speeds, high performance complex analog signal processing, for speech, process control and signal analysis applications can be easily implemented.

MICROPROCESSOR INTERFACE

Microprocessor systems are available in two types: the minimum or unbuffered system, and the maximum or fully buffered system. The minimum system is usually found in dedicated or control process applications, while the maximum system is more common in the general purpose application. The HI-5712 ADC is equally well suited for both applications with only a bus driver added to the minimum system configurations discussed here to support the very high drive requirements to the larger maximum system.

As with any peripheral device, the HI-5712 ADC requires address decoding as illustrated in Figure 7 and 8 (Intel 8085 and Motorola 6800 interfaces). The interrupt flip-flop provides stable interrupt generation to notify the microprocessor of data availability when conversion is completed. In a manner similar to the microcomputer, the command register lines and output data lines can be wired in parallel. The minimum system application requires no buffering as the HI-5712 simultaneoulsy exhibits minimum loading with high current drive capability, and can therefore be treated as any other high impedance NMOS peripheral support device.

The software requirement is the same as a microprocessor interface. Command register data can be loaded during a Write cycle with the converter automatically initiating conversion of the rising edge of the Write signal. Data is inputted to the microprocessor in the same two byte format.

The high speed nature of the HI-5712 ADC provides all of the necessary capabilities for use with advanced signal analysis techniques. It should be noted, however, that a 12-bit conversion is completed in 8 microseconds. To fully utilize these high speed throughput rates, microprocessor systems will require operation with a high speed Direct Memory Access (DMA) as most microprocessors cannot keep pace with a 10 microsecond or faster ADC. Systems not incorporating a DMA or other high speed transfer device will be throughput-limited by the microprocessor and not the ADC.

CONCLUSION

High performance analog processing systems using microprocessors can now be easily designed using a minimum of hardware and software support. By careful utilization of the versatile I/O features of the HI-5712, many applications can be implemented with no digital interface hardware and far less software than with other conventional devices. New horizons in signal processing are now realizable. The HI-5712, with its advanced I/O and superior analog characteristics, is an ideal solution for microprocessor/microcomputer systems with analog input interfaces.

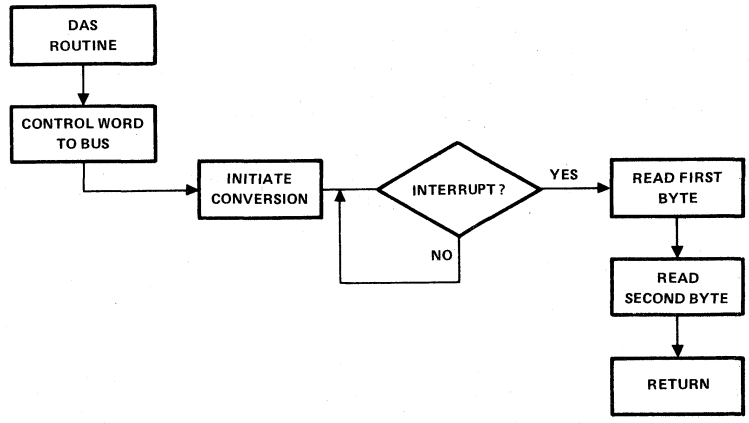

FIGURE 6 – SOFTWARE FLOW CHART FOR MICROCOMPUTER OR MICROPROCESSOR CONTROL OF ADC

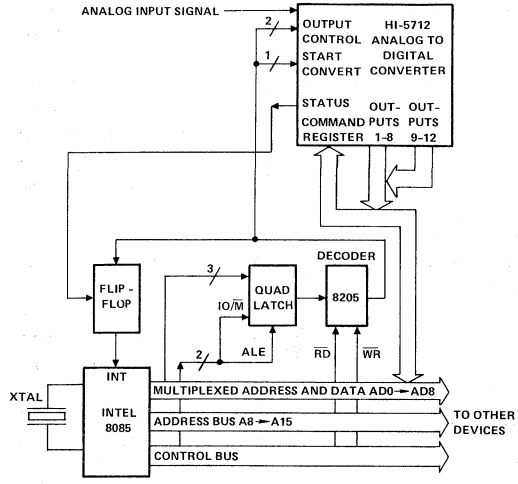

FIGURE 7 – INTEL 8085 MICROPROCESSOR

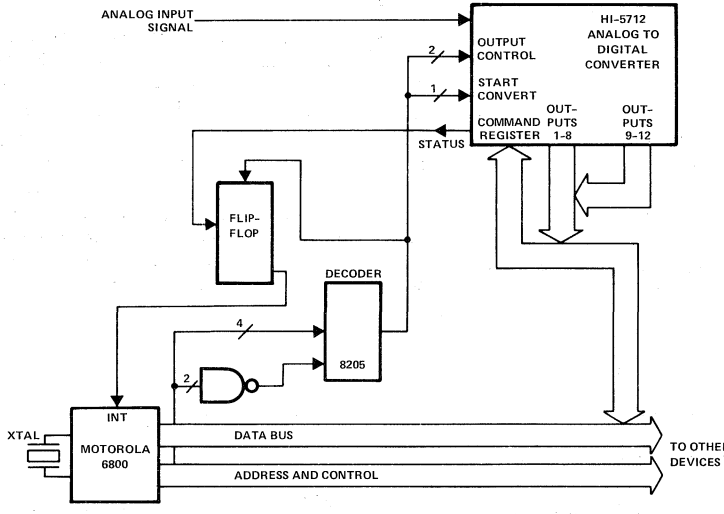

FIGURE 8 – MOTOROLA 6800 MICROPROCESSOR WITH HI-5712 ADC

HARRIS

APPLICATION NOTE 529

MICROPROCESSOR INTERFACE METHODS FOR HIGH-SPEED DATA ACQUISITION SYSTEMS

BY L. E. ENRIQUEZ, J. E. SULLIVAN, D. T. TUNG

Since their introduction in the early 1970's microprocessors have dramatically displaced random logic for system design. This explosive growth of microprocessor applications has greatly influenced the increased use of peripheral interface integrated circuits (IC's). These special IC's were developed to support CRT's, printers, floppy disks and other peripheral devices, but virtually none were offered for analog input signal conditioning and conversion. Typical systems using a single microprocessor board and multiple analog interface boards became commonplace due to the lack of suitable analog interface IC's. Today, new units are available which provide microprocessor compatibility with analog input signal conditioning and processing within compact hybrid devices comparable in size to individual IC's. These new products permit the assembly of a complete analog interface and microprocessor system on a single board no larger than those used in the past for the microprocessor alone. The HI-5900 and the HI-5901 analog signal processors and the HI-5712 Analog to Digital Converter (ADC) are state-of-the-art versions of these new hybrid devices.

A typical analog to microprocessor interface (data acquisition subsystem) consists of five functional blocks. (See Figure 1). Multiple input signals are accepted and selected by the input multiplexer, with the programmable gain instrumentation amplifier providing both common mode signal rejection and signal amplification. Additional signal processing is required between the output of the instrumentation amplifier and the ADC, for the latter cannot convert a continuously changing analog signal into digital form. The additional processing is provided by the track-and-hold stage, which samples the instantaneous value of the analog signal on command and holds this level as a steady input to the ADC until the conversion cycle is completed. The ADC supplies a series of digital output words, which correspond to the individually sampled analog levels. Finally, digital logic circuitry is required to interface the function control signals from the microprocessor to the individual circuit elements.

As shown by the dotted lines in Figure 1, two hybrid devices, the HI-5900 (or the HI-5901), and the HI-5712 contain all of the necessary analog and digital building blocks needed, for a complete two package, multi-channel data acquisition subsystem. The HI-5900 includes an eight-channel differential input multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold stage. Designed for 16-channel pseudo-differential or single-ended applications, the HI-5901 features a 16-channel multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold amplifier. All input control lines are microprocessor compatible and well suited for NMOS, CMOS, and TTL logic.

The HI-5712 is a 12-bit, high speed ADC which features a microprocessor compatible tri-state output bus and software programmable output code and word length controls permitting its application in 8, 12, and 16-bit systems. Accepting either unipolar or bipolar inputs, the device incorporates input latches on all digital control lines, assuring full compatibility with TTL, CMOS, and NMOS logic. The unit also features an on-board, overridable, precision +10 volt reference with sufficient output current capability for external applications.

Unlike conventional hybrid technology, these products are fabricated using leadless chip carrier (LCC) techniques, which employ IC dice packaged in LCC's mounted to both sides of a multilayer ceramic substrate. The final product comprises hermetically-sealed building blocks, each visually inspected and mechanically and electrically tested to the highest standards of commercial, industrial, or military specifications prior to assembly. Subsequently, additional visual and electrical tests are made to the completed hybrid device at nominal and rated temperature extremes to ensure maximum reliability and optimum performance.

When used in combination, the HI-5900 (or 5901) and the HI-5712 form a high performance, extremely accurate two-package data acquisition subsystem with a 50 kHz (600 kbs) throughput rate. The system is compatible with all standard microprocessor systems although the interface peripherals required will vary from one system to another, depending on individual system complexity. An example of a two chip, high performance data acquisition subsystem using a microcomputer is illustrated in Figure 2. This example, using the Intel 8748 series microcomputer, is applicable to any of the

currently available chip microcomputers. Both hardware and software requirements have been minimized to reduce costs and provide maximum flexibility.

Four microcomputer control lines along with the microcomputer bus satisfy all of the interface requirements. Two of the lines are used to initiate data conversion and to interrupt the microcomputer when data is available The remaining two lines enable data onto the bus under microcomputer control. The bus is structured so that channel selection, amplifier gain and ADC modes of operation are controlled by simply outputting data to the bus. Input data is in the form of two bytes: the first byte contains the most significant eight bits with the second byte containing the least significant four bits. Due to the high impedance nature of the Harris parts, other devices can be added to the bus without exceeding bus load limitations.

The complete DAS operates under software control for maximum flexibility. A microcomputer internal software timing loop establishes the necessary hardware timing signals. The software flowchart in Figure 3 illustrates typical system operation.

The system as depicted operates at a 50 kHz throughput rate, while maintaining true 12-bit accuracy throughout the temperature range. Similar high performance DAS's can be implemented for a variety of applications and offering compatibility with most microcomputers.

Interfacing a DAS to a microprocessor system bus is similar to interfacing any other peripheral device. Figure 4 illustrates an interface for a typical microprocessor bus and is applicable to all popular microprocessors.

As with any peripheral, a bus driver and address decoder is required. The octal latch provides stable control information during signal acquisition while the one-shot generates a start convert pulse after the required 10 μsec delay. Two I/O locations are used for the interface: one location is used for both Read and Write and the other is a Read only. A Write to the first location loads multiplexer gain and ADC control information and 10 μsec after the Write initiates a conversion cycle. At the end of conversion an interrupt is generated informing the microprocessor that data is available. Data can then be read in the same two byte format as previously discussed for the microcomputer. Software control for this application is merely a driver routine to support the two I/O locations and the interrupt routine, with all timing functions being generated in the hardware.

Further enhancement of system performance can be achieved with Direct Memory Access (DMA), FIFO's and other circuits to alleviate the high speed data handling requirements that a 50 kHz throughput DAS places on the microprocessor.

In conclusion, a single board microprocessor DAS can now be easily implemented using newly available hybrid analog interface devices. These devices not only support the requirements of microprocessor system buses but provide superior performance compared to discrete designs, while using far less printed circuit (PC) board real estate. The versatile HI-5900, HI-5901 and HI-5712 devices offer ideal solutions for these and other applications requiring high performance, and cost-effective microprocessor interface capability.

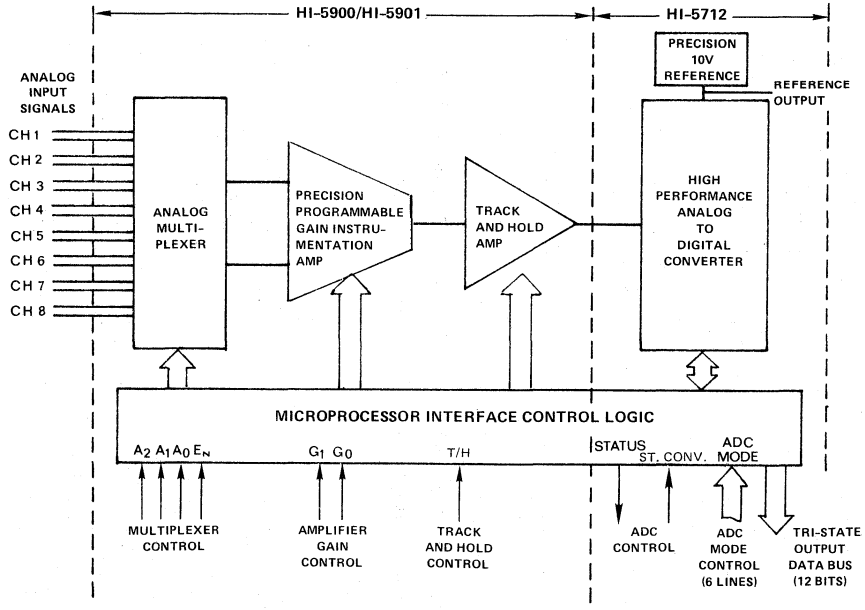

Figure 1 Data Acquisition Subsystem

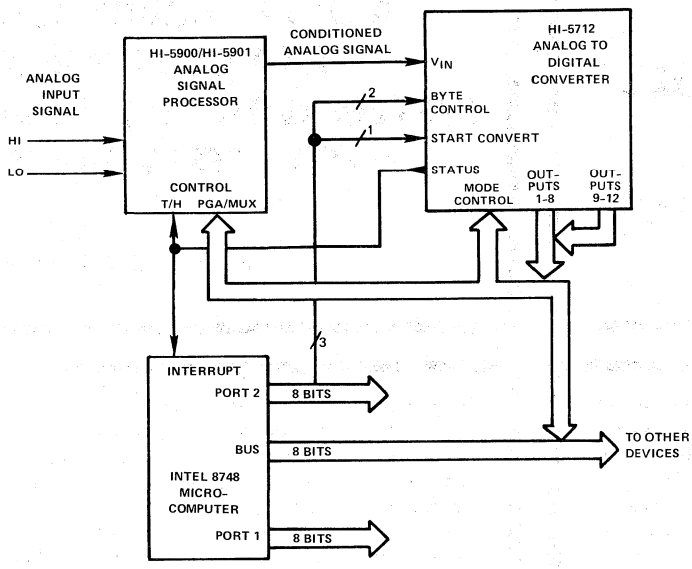

Figure 2. Microcomputer with High Performance Data Acquisition Subsystem

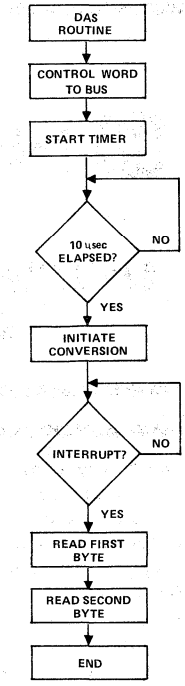

Figure 3 Software Flowchart

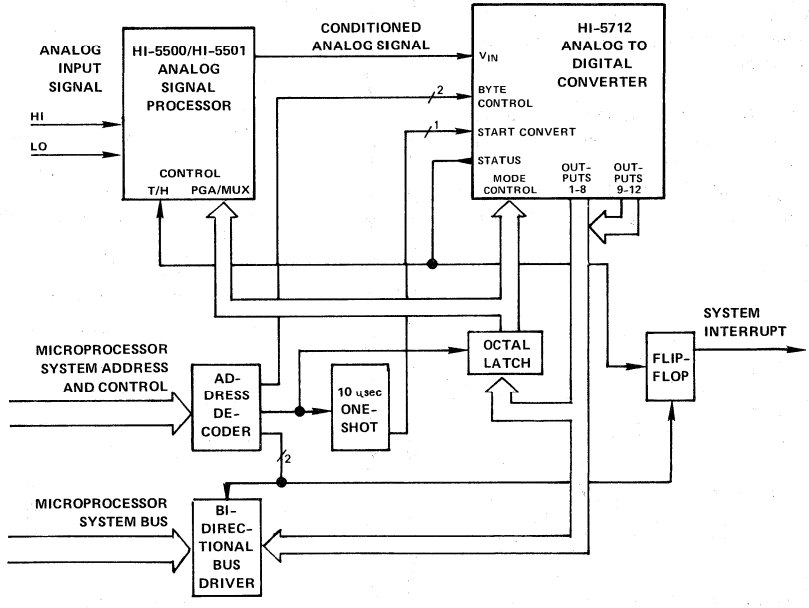

Figure 4. Microprocessor DAS and Interface

HARRIS

APPLICATION NOTE 530

A DATA ACQUISITION AND CONVERSION SYSTEM WITH LESS THAN ±1 LSB OFFSET ERROR

BY JOHN E. SULLIVAN

The continuing pressure for higher resolution and higher accuracy Data Acquisition Systems requires smaller overall system offset errors. Historically, with eight-bit systems, offsets of up to 30 or 40 millivolts were acceptable, and the use of trimpots or fixed resistors for adjustment was more than adequate. State-of-the-art systems with 12 to 16-bit resolution, however, require total system offset over temperature to be less than 5 millivolts. Offset voltages of this magnitude are difficult to achieve using trimpots, and extremely difficult to stabilize in uncontrolled thermal environments.

Ideally, a DAS system should have less than ±1 LSB of offset error regardless of the number of bits incorporated in the system. This goal is extremely difficult to achieve using linear design techniques. Digital design techniques, however, can be used to null offsets, typically to ±1/2 LSB over the complete temperature operating range.

A typical Data Acquisition System is illustrated in Figure 1. System offset correction can be accomplished at any stage even though each stage contributes to the overall offset. The first step to offset correction is to have the analog to digital converter (A/D) calculate the digital code representing total system offset when the input is grounded. This code, when converted back to analog form, inverted and added to the input circuitry at a convenient point, will null all offsets.

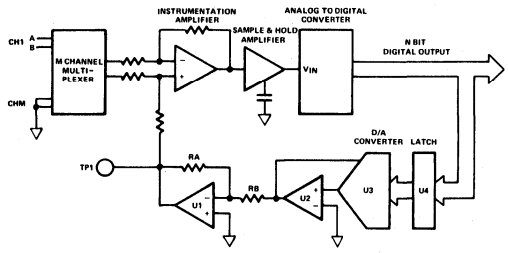

Figure 1 – Typical Data Acquisition Block Diagram

Figure 2 shows a simple digital offset correction scheme. The additional digital to analog converter (D/A) U3 and op amp U2 convert the calculated digital offset code back to analog form. Op amp U1 inverts this signal and adds it to the input differential amplifier. The inverted signal is scaled by resistors RA and RB such that a 1LSB step of the A/D is equal but opposite in sign to a 1LSB step of the D/A at TP1. This scaling can be calculated by Equation 1.

Equation 1

$$\frac{VP_1}{2^{n1}} = \frac{RA}{RB} \quad \frac{VP_2}{2^{n2}}$$

Where: VP_1 = Dynamic range of Linear A/D in volts

n_1 = Number of Bits of A/D

VP_2 = Dynamic Range of Linear D/A in volts

n_2 = Number of Bits of D/A

RA = Feedback Resistor

RB = Input Resistor

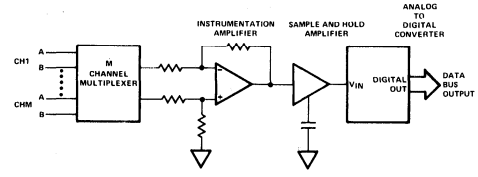

Figure 2 - Digital Error Correction Block Diagram

Measurement of the system offset is made with all digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital zero input results in a positive half full scale output voltage at TP1. This ensures that the A/D need only measure positive offset voltages and not negative voltages, allowing for systems operating both in uinpolar and bipolar modes.

The size of the D/A converter is determined by the maximum amount of offset that must be corrected by the system:

Equation 2

$$\text{D/A Size (Bits)} \geq \frac{\ln(\text{Max offset} \quad 2^{n1})}{\frac{VP_1}{\ln(2)}}$$

In operation, a spare input channel is grounded and the input to the D/A is forced to digital zero. The resulting compound offset, Voffset, is then equal to the voltage at TP1 plus all component offsets. The A/D then calculates a digital code representing V_{offset} which is latched into the D/A. Due to the inversion and scaling of the Op Amp U2, this is equivalent to subtracting Voffset from the half full scale output of the D/A. Obviously the result is the nulling of V_{offset}.

The most critical parameter in this circuit is the ratio of the resistors RA and RB. This ratio will determine the overall accuracy of the correction, and 1% resistors are sufficiently accurate to null all offsets. Normally for 12 and 14-bit systems, a 6-bit DAC will correct all possible offsets.

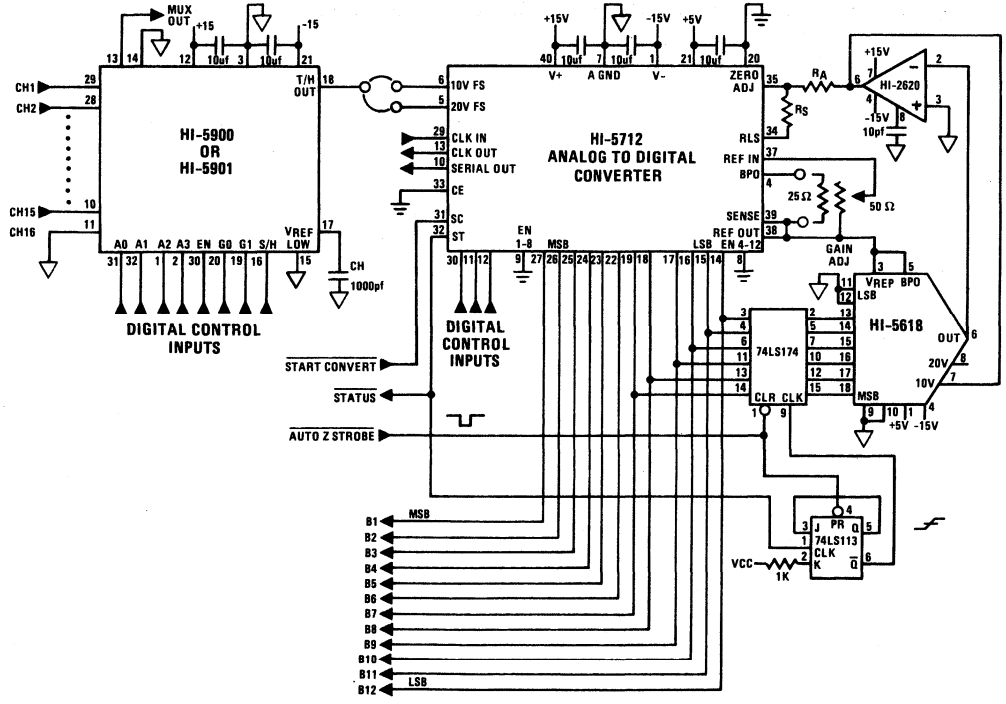

Figure 3 – Auto-Zero Analog to Digital Converter

Various configurations can be employed to minimize parts count. Fully automatic offset correction is added to the HI-5900/HI-5712 DAS component set using only four additional I.C.'s as shown in Figure 3. External digital logic or a microprocessor selects a spare input channel which has been previously grounded. Receipt of the Auto-Z strobe initializes the auto-zero function by clearing the latch to all zeroes, resulting in a D/A output of 32 LSB's of positive offset. The microprocessor then initiates an analog to digital conversion sequence. The Conversion Complete status line of the A/D causes the latch to strobe and store the digital offset correction term to the D/A converter. The analog correction term is then injected into the zero adjust pin of the A/D converter. Care must be taken when injecting the correction term to this point on the A/D since the ratio of RA/RB is affected by the impedance of the summing junction.

Table 1 lists the accuracy of correction for various full scale input ranges. The offset after correction listed in the Table is the maximum observed offset when 10 different 5900's and 5712's were tested at all temperature ranges between -55°C, and +125°C ambient. In no case did the offset after correction ever exceed 1LSB of the analog to digital converter.

HI-5712 INPUT CONFIGURATION	R_S	R_A	OFFSET AFTER CORRECTION
0 TO +10V	681Ω	147kΩ	0.5mV
0 TO +20V	825Ω	147kΩ	1.0mV
-5V TO +5V	580Ω	147kΩ	1.0mV
-10V TO +10V	681Ω	147kΩ	2.0mV

Table 1 — Offset Correction Accuracy

Along with the straight forward benefit of greatly improved offset performance, this correction technique eliminates the requirement for any offset adjustments, either initially or during the operating life of the DAS. In practice, the auto-zero function need only to be used after system power is applied or after a significant change in ambient temperature. Therefore, high performance microprocessor-based DAS systems requiring maximum performance can employ this technique to improve accuracy with minimal impact on throughput rate.

HARRIS

APPLICATION NOTE 531

ANALOG SWITCH APPLICATIONS IN A/D DATA CONVERSION SYSTEMS

BY RICHARD WHITEHEAD

INTRODUCTION

A choice of three approaches is available when implementing a data conversion system: 1). "build-from-scratch", 2) buy sub-systems and configure a system, or 3) purchase a pre-engineered system which meets the requirements. Also, as a matter of economics, the users of sensor-based data acquisition systems make it common practice to ensure a maximum number of elements are shared in the system. An invaluable tool used in this process is the analog switch or multiplexer. The purpose of this article is to focus attention on those parts of the system which require analog switches and to emphasize the importance of relative operating parameters.

BASIC SYSTEM CONFIGURATIONS

A/D data conversion systems can be categorized into two general groups: 1) low level signal conversion (analog signals below 1 volt) and 2) high level signal conversion (analog signals above 1 volt). Within these categories, four basic data conversion configurations are illustrated to point out the advantages of using analog switches.

Conditioning the analog signals prior to multiplexing (Figure 1A) is the most popular system arrangement and is both efficient and capable of high performance This configuration, which shares the level signals. Figure 1B represents a more austere approach resulting in lower cost and decreased performance. This type is useful in less demanding applications such as processing high level signals. To process multichannel, single event information such as wind tunnel or seismographic measurements the arrangement shown in Figure 1C is most likely to be used. This configuration represents a more expensive, less efficient approach due to the decreased number of shared elements. Figure 1D shows the elimination of the analog multiplexer and sample and hold circuits. By moving the multiplexing task to the digital domain, slower and lower cost A/D converters can be used.

TYPES OF ANALOG SWITCHES

The most commonly used types of analog switches found in today's data conversion systems are: reed relay, JFET, and CMOS. Reed relays offer low ON and high OFF resistance and are capable of handling very high voltages, but have slow speeds. JFET switches have lower OFF leakage current and are capable of very high speeds. CMOS switches, which are the most popular and widely used in multiplexer applications, have low OFF leakage currents, good speed, and stable ON resistance under varying input signal conditions.

SELECTING THE PROPER CMOS ANALOG SWITCH

The data conversion system error budget should be used to narrow the field of CMOS analog switches suitable for the application. Primarily, the speed of the switch must be consistent with the systems's sample rate requirements without introducing unacceptable transfer error. Significant dynamic errors inherent to CMOS analog switches are OFF channel leakage current and a settling time value dictated by the device's ON resistance and its inherent capacitance. Figure 2 shows the equivalent of a CMOS analog switch giving all of the inherent and distributed properties which may become the source of unwanted system errors.

Other system restrictions may further narrow the field of candidates suitable to performing the switching task. These restrictions could include, low power budget, hostile environment, cost, alternate sourcing, and package density. It's possible that all of

these restrictions could occur, and this situation may influence the user to seek a compromise solution to his problem.

Fortunately, CMOS analog switches consume very little power and only the most demanding power budget would feel the strain of their power requirements. If the operating environment of the device includes high voltage spikes, excessive noise pickup, and/or power supply interruptions, the selection should be narrowed to the internally protected analog devices such as the HARRIS HI-506A/507A. These multiplexers come with guaranteed overvoltage specifications which enhance the reliability of the data conversion system. Usually, package density, cost restrictions, and alternate source requirements are simultaneously applied, and with present CMOS analog switch availability from several vending sources, these problems should be minimal. It should also be ensured that the CMOS analog switch selected does not exhibit any inherent latch-up tendencies. The Harris dielectrically isolated CMOS analog switches offer latch free operation.

To some users the proper CMOS analog switch selection may become complicated leading to possible alternate solutions. An example of such a situation could be in high speed data conversion system where the settling time constraint placed on the multiplexer results in an unacceptable time penalty (Figure 3A). Figure 3B shows an alternate and practical solution to this problem. The two tiered multiplexing scheme may reduce the errors caused by leakage currents and settling time by an order of magnitude. Another practical solution would be to select an analog signal processor such as the HARRIS HI-5900/5901 shown in Figures 4A and 4B. These devices facilitate user application and reduce engineering time thereby reducing overall cost.

OTHER USES FOR CMOS ANALOG SWITCHES

Attention has been focused on the selection of CMOS analog multiplexers used to increase efficiency of data conversion systems through shared elements. But the versatile CMOS switch is not limited to only that function. Obviously they can be used in sample and hold circuits, with important parameters being switching speed, OFF leakage current, and charge transfer. Analog switches such as the HARRIS HI-200/201 and HI-300 series may be used in sample and hold circuits and also in auto-zeroing circuits for integrating type data converters (Figure 5).

Figure 6 shows the CMOS analog switch used to program the gain of an instrumentation amplifier.

HIGHLIGHTS

In A/D data conversion systems analog switches are mainly used as multi-channel multiplexers to increase system efficiency through shared elements.

CMOS analog switches are the most widely used in data conversion systems.

When selecting the proper CMOS analog switch, look for low OFF leakage current, good settling time, latch free operation, and stable ON resistance under varying analog signal input conditions.

If the environment is hostile, select from the internally protected CMOS analog switches.

Where an alternate solution is required, attempt to ensure your solution is the most practical with respect to your error budget.

References:

Garrett, Patrick H. Analog Systems for Microprocessors and Minicomputers. Virginia: Reston Publishing Company, Inc., 1978.

Kaufman, Milton and Seidman, Arthur H. Handbook of Electronic Calculations. New York: McGraw-Hill Book Company, 1979.

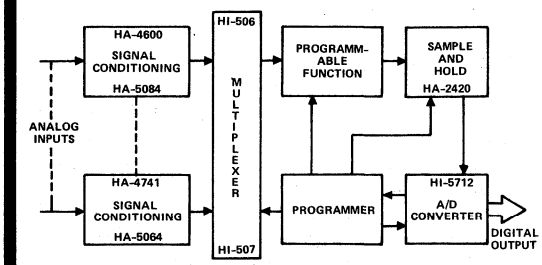

Figure 1A – Multiplexed. Signal Conditioning for Low Level Inputs

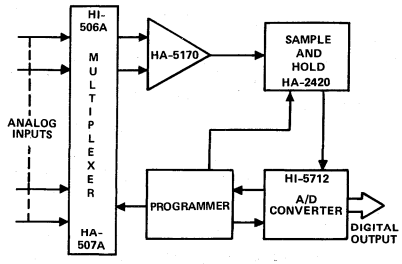

Figure 1B – Multiplexed, High Level Inputs

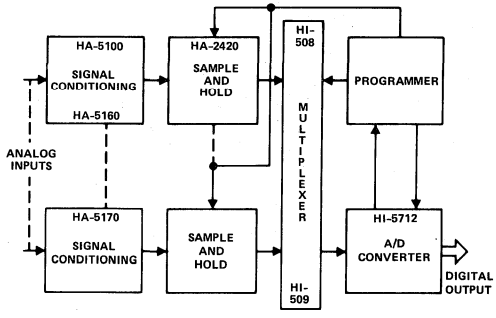

Figure 1C – Multiplexed, Sample / Hold Outputs

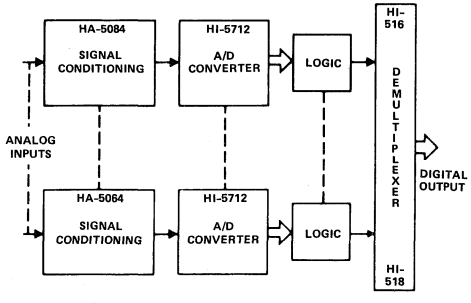

Figure 1D – Multiplexed, Demultiplexer
A/D Outputs

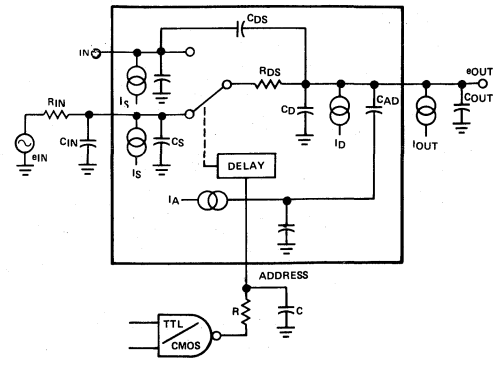

Figure 2 – Equivalent CMOS ANALOG SWITCH
DC Offset Error = $R_{DS} \times I_D$
Setting Time Determined by $R_{DS} \times C_D$

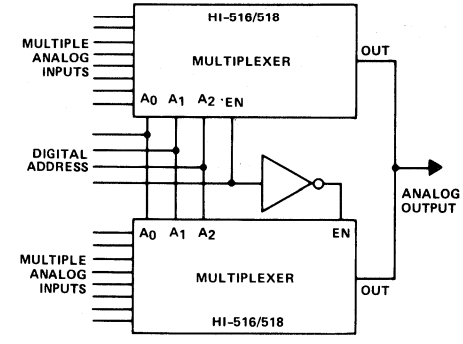

Figure 3A – Cascaded Multiplexers: Output Leakage Currents and Output Capacitance Increase Errors

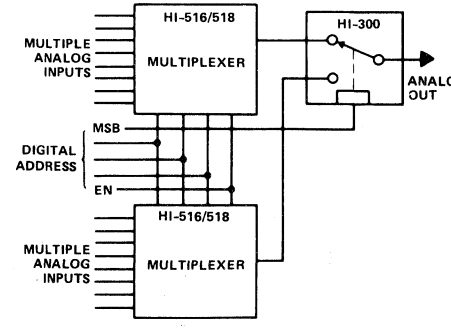

Figure 3B – Cascaded Multiplexers Two - Tiered Method : Errors Reduced Through Shared Switch

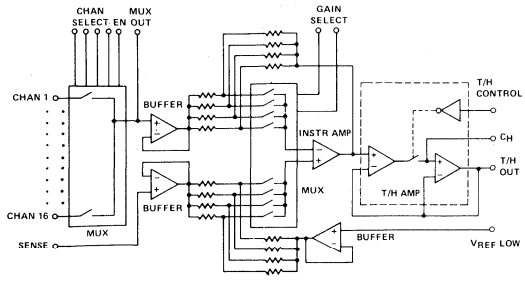

Figure 4A – HI-5900 Analog Signal Processor

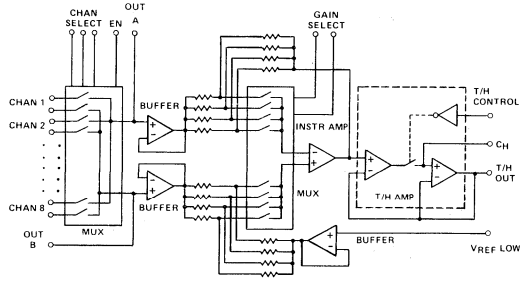

Figure 4B – HI-5901 Analog Signal Processor

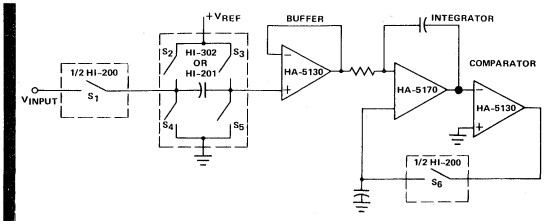

Figure 5. This autozero integrating converter uses six analog switches – S_1 through S_6. Zero correction occurs when S_3, S_4 and S_6 are "on". Integration occurs with S_1 closed. Integrate-reference takes place when S_2 or S_5 is "on".

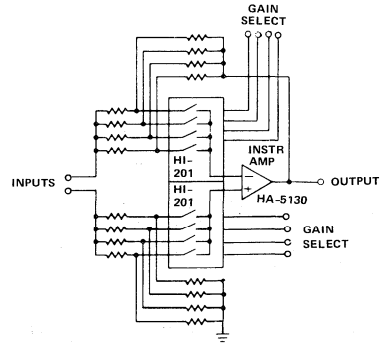

Figure 6 – Programmable Gain Instrumentation Amplifier

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APPLICATION NOTE 532

COMMON QUESTIONS CONCERNING CMOS ANALOG SWITCHES

BY CARL WOLFE

INTRODUCTION

The following information is a direct result of a significant amount of time spent in response to questions from users of HARRIS analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of HARRIS analog switches. Some questions are technical in nature while others are simply questions on interpretation of the HARRIS Analog Data Book.

POWER SUPPLY CONSIDERATIONS

The first two questions are similar questions and the explanation will apply to both:

QUESTION #1: If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)

QUESTION #2: If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transitors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transitor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

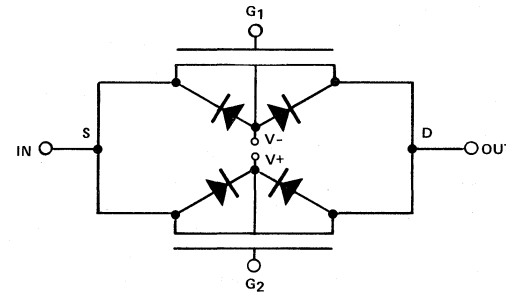


Figure 1. Basic CMOS Transmission Gate

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

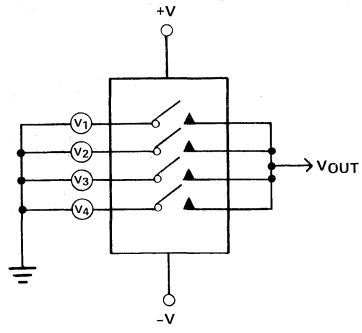


Figure 2. Switching Multiple Inputs

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

INPUT OVERVOLTAGE PROTECTION

There is a possibilty the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

QUESTION #3: Can an input greater than the supplies be applied?

QUESTION #4: In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

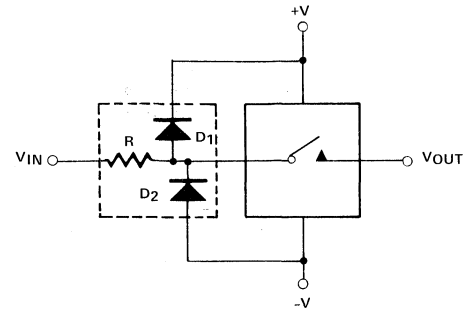


Figure 3. Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottkey diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The HARRIS switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

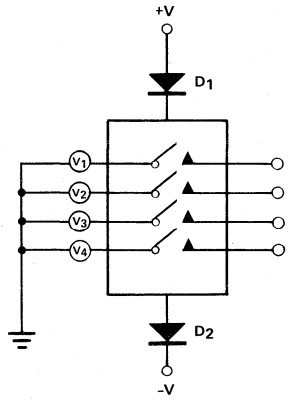


Figure 4. Powering the Switch With the Input Signals

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has ±15V supplies and needs to switch a +18V signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to +20V, -10V. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

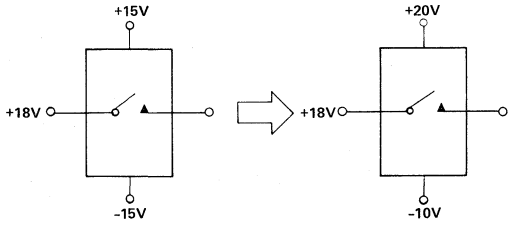


Figure 5. Varying the Supplies to Meet the V_{IN} < V Supply Requirements

SINGLE SUPPLY OPERATION

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

QUESTION #5: Can the switch be operated at a single power supply?

QUESTION #6: What is the minimum power supply possible?

Usually engineers with critical power requirements request single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5 volt supply. The performance of the switch will vary, however, as the supply voltage varies. So, for the HI-300 series, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5 volt supply will have higher on resistance and slower switching speeds than the same device at ±15 volts or even a single +15 volt supply. This represents a change in both DC and AC performance. Even though the switch may now meet the users power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate - source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

QUESTIONS ABOUT HARRIS SWITCHES

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Harris product line and data catalog. The following are examples of some of the more common questions concerning the Harris Analog Data Catalog.

QUESTION #7: What is the difference between the VL and VR pins on the HI-5043 and V_{REF} pins on the HI-201 ?

The device pins mentioned above have their own individual functions even though they are all associated wth the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving from CMOS Logic greater than 5 volts. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal establishes the ground for the internal ref-

erence circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5 volts for TTL logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accomodate the higher CMOS level.

The next question is easily the most frequently asked question about HARRIS HI-50XX series of switches.

QUESTION #8: Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW ?

Actually, the answer to the question is printed at the top of the data sheet page,depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the maximum ratings and performance between channels of the switches. The following questions are typical:

QUESTION #9: Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometime arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around these conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptable to variations in manufacturing.

QUESTION #10: What is the variation in "on" resistance between channels on the switch?

There are two causes for these variation. One cause is process variation which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is ±10% tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a ±5Ω variation.

HARRIS

APPLICATION NOTE 533

A MONOLITHIC SUBSCRIBER LINE INTERFACE CIRCUIT

BY DAVID P. LAUDE
DAVID J. DONOVAN

INTRODUCTION

This application note describes the HC-5502A and HC-5504 Subscriber Line Interface Circuits (SLICs). These are monolithic low current (LC) SLICs for use in analog or digital PABX or Central Office (CO) applications. They are fabricated with 80 volt Dielectric Isolation technology. Both have enhanced surge voltage capability, and require four external resistors as shown in the application circuits (Fig. 1 & 2). The SLIC-LC incorporates many of the BORSHT functions on a single IC chip, including battery feed with power denial control, loop current limiting, overvoltage protection (with some external devices), ringing relay control, line supervision with off-hook, ring trip and ground key detection and 2/4 wire conversion. In addition, an uncommitted op amp is included in the SLIC-LC either for external connection of a balance network or for any other application.

FUNCTIONAL DESCRIPTION

Shown in Fig. 1 is a typical line circuit configuration using the HC-5502A SLIC-LC, and Fig. 2 shows a typical line circuit configuration using the HC-5504 SLIC-LC.

Balanced DC Battery Feed with Loop Current Limiting and Power Denial.

The SLIC-LC provides DC loop current to the two wire side for powering the end instrument in the off-hook state and for loop monitoring purposes. Furthermore, this battery feed is balanced so that the tip to ground impedance is the same as the ring to ground impedance. To minimize power dissipation, the HC-5502A provides a maximum 34.5mA of loop current and the HC-5504 provides a maximum of 48mA of loop current under worst case conditions (R_{Loop} = 200 Ω). This is accomplished by a loop current limiting circuit within the SLIC-LC devices.

The tip feed (TF) and the ring feed (RF) outputs are low impedance and require four external 150 Ω ±1% resistors that limit current to the secondary protection bridge during overvoltage surges and present a 600Ω impedance to the subscriber loop. All four feed resistors must be matched to within 0.1% for the specified longitudinal balance.

If the SLIC is not in a loop current limiting mode, then $R_{Loop} = (V_{T-R}/I_{Loop}) - 600\,\Omega$. Under loop current limit conditions, the voltage at RF will move towards ground, as a function of R_{Loop}, to maintain the maximum loop current (I_{Loop}).

The HC-5502A and the HC-5504 differ mainly in two areas. The first is the maximum off-hook loop current. The HC-5504 is able to drive longer lines with its maximum 48mA current capability as compared to a maximum of 34.5mA for the HC-5502A.

Secondly, notice the difference in ring configurations in the respective applications circuits (Fig. 1 & 2). The HC-5502 ring generator is referenced to GND and is injected on the tip side, while the HC-5504 ring generator is referenced to VBat-and is injected on the ring side. The HC-5504 may also be configured for ground referenced ringing or balanced ringing. (See applications note #549 for detailed explanation.)

Both SLICs offer selective denial of power to subscriber loops. When a logic level 0 is applied to the power denial ($\overline{PD}$) Terminal, the following events occur:

- Metallic loop current is limited to a maximum of 2mA.
- The loop monitoring functions described later are not necessarily valid.
- It is not possible to apply ringing voltage to the loop (across tip and ring).

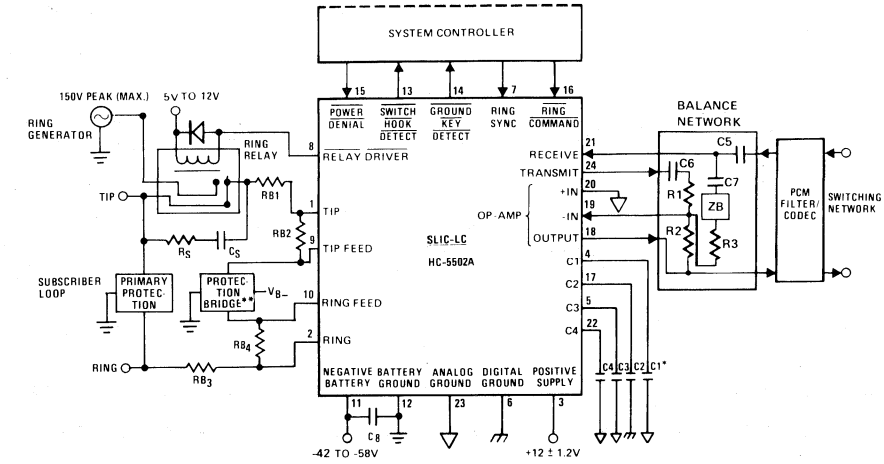


Figure 1. Typical Line Circuit Application with the HC-5502A Monolithic SLIC.

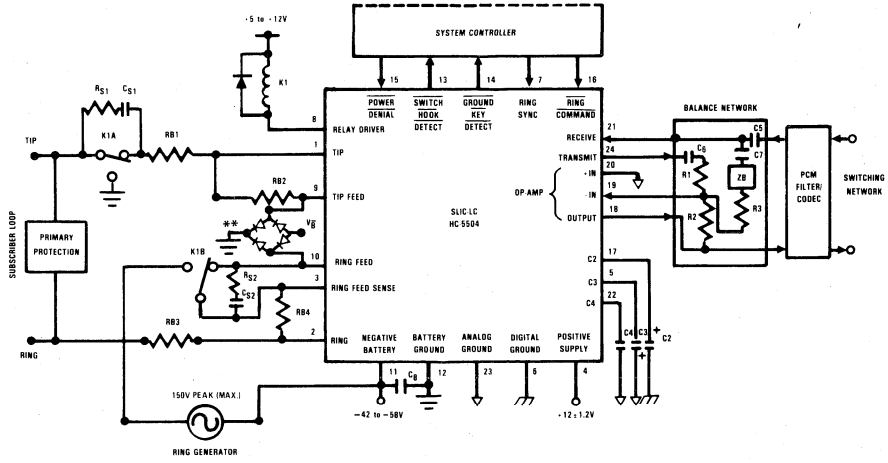


Figure 2. Typical Line Circuit Application with the HC-5504 Monolithic SLIC.

TYPICAL COMPONENT VALUES

*C1=0.5μF
C2=0.5μF, 10V
C3=0.3μF, 30V
C4=0.5μF to 1.0μF, ±10%, 20V (should be nonpolarized)
C5=0.5μF, 20V
C6=C7=0.5μF (10% Match Required) Note 2, 20V
C8=0.01μF, 100V

R1→R3=100KΩ (0.1% Match Required, 1% absolute value), ZB= 0 for 600Ω Terminations (Note 2)
RB1=RB2=RB3=RB4=150Ω (0.1% Match Required, 1% absolute value)
$R_{S1}=R_{S2}=R_S$=1KΩ, $C_{S1}=C_{S2}=C_S$=0.1μF, 200V typically, depending on V_{ring} and line length.

*Note 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

Note 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1 μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10V to -29V step when the loop is closed and the too large a value for C6 may produce an excessively long transient at the op-amp output to the PCM filter/CODEC. A 0.5 μF and 100KΩ gives time constant of 50msec.

**Note 3: Secondary protection diode bridge recommended is MDA 220 or similar.

Overvoltage Protection and Longitudinal Current Rejection

The SLIC-LC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

Table 1

PARAMETER	TEST CONDITION	PERFORMANCE (MIN)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak
T/GND, R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak
50/60Hz Current			
T/GND, R/GND	700V rms Limited to 10A rms	11	Cycles

The SLIC-LC will withstand longitudinal currents up to maximum of 30mA rms, 15mA rms per leg, without any performance degradation.

Ring Injection and Ring Trip Detection with Hardware Interlock

Ring Injection is accomplished by a ring relay external to the SLIC-LC device. The SLIC-LC device has an open collector relay driver output ($\overline{RD}$) capable of sinking 62mA current for control of this ring relay. Furthermore, the device has a low active ring command ($\overline{RC}$) input (TTL compatible) which activates the ring relay unless the subscriber is off hook ($I_{Loop} > 10mA$) or the SLIC-LC is in the power denial state ($\overline{PD}$) < 0.8 volts. This hardware interlock feature, prevents inadvertent ringing of the phone in the off-hook or power denial conditions.

In order to preserve the ring relay contacts and minimize RFI, the ($\overline{RD}$) output is only permitted to change state at or near the zero voltage crossings of the ring voltage signal. A TTL compatible ring sync (RS) input synchronized with ring voltage is applied to implement this feature.

Ring trip detection is also performed by the SLIC-LC device. If the subscriber goes off-hook during ringing, the $\overline{RD}$ output becomes inactive within 3 ring voltage cycles after this event occurs.

Loop Monitoring (Switch Hook and Ground Key Detection)

The SLIC-LC is able to monitor DC conditions associated with the loop (i.e. tip and ring) in order to determine end instrument status, transmit dialing pulses, and detect line fault conditions.

The SLIC-LC device provides the following low active TTL compatible logic outputs which indicate loop status:

- Switch Hook Detection ($\overline{SHD}$) – This output becomes active for loop currents exceeding 5.0mA and becomes inactive for loop currents less than 10mA.
- Ground Key Detection ($\overline{GKD}$) – This output becomes active when the DC current flowing into the ring lead (I_{RING}) exceeds the current flowing out of the tip lead ($-I_{TIP}$) by more than 10mA, and becomes inactive when this current difference is less than 20mA. This function can be used for monitoring calibrated ground key signals or sustained unbalanced output shorts.

Hybrid Function

Conversion of bidirectional signals from 2 wire telephone lines to separate receive and transmit signals is accomplished with the SLIC-LC device. Key features are:

- With external feed resistors as specified, a balanced DC and AC impedance of 600Ω appears across tip and ring terminals.
- Longitudinal balance (2 wire off hook) in excess of 58dB. A measure of degree of matching of tip to ground and ring to ground impedance.
- Longitudinal balance (4 wire off hook) in excess of 50dB. A measure of common mode rejection capability of the device.
- Low frequency longitudinal current suppression – operational capability in presence of large common mode current at power line frequencies.
- Low idle channel noise.
- Level linearity over 58dB dynamic range.
- Overload level to accommodate maximum speech power level.
- Good transhybrid loss (i.e. rejection of receive signals leaking through to transmit side) capability in conjunction with appropriate balancing network. As shown in Figs. 1 & 2, , external passive components and internal uncommitted op amp make up the balance network.

The impedance Z_B can be made to balance any loop impedance. Parameters of the balance impedance can be calculated by knowing the loop termination Z_L and from the following equation: $Z_B = \frac{K}{2} Z_L$

(K is a scale factor and this function allows the user to scale the balance impedance components to practical values. K = 100 is recommended for most applications.)

Values of other components in balance network are shown in the Typical Component Values Table.

- Minimum delay in transmitting signals through the device.
- Capacitors C1 through C4 help provide filtering and time delay functions.

BLOCK DIAGRAM DESCRIPTION

In the SLIC-LC block diagram of Fig. 3, the Receive (RCV) signal and -4V are summed and buffered to TF, they are negatively summed with VB- and buffered to RF, providing an open circuit DC feed of -4V and -44V for a VB- of -48V. Since the RCV signal appears in opposite phase between TF and RF, the 4/2 wire insertion loss is 0dB if Z_L = RBF1 + RBF2.

The transversal loop currents appear in voltage form at the output of summer 3 (VTRAN) which is also the transmit (Tx) output. The VTRAN signal is sensed by the switch hook detection circuit which signals the logic when transversal loop currents exceed 7.5mA typical. In addition, the VTRAN signal is monitored by the ITRAN limit circuit, which can modify the DC component of RF through summer 2 by adjustment of I1 through R. This limits the DC transversal current to a maximum value of 34.5mA for HC-5502A and a maximum of 48mA for HC-5504 SLICs, which also limits maximum power dissipation.

Longitudinal loop currents appear in voltage form at the output of summer 4 (VLONG) which provides input for the ring trip and ground key detection circuit. Undesirable power line induced longitudinal currents of up to 30mA rms are suppressed by an external capacitor (C4) which may delay ring trip detection by up to 3 ring cycles.

Power Denial is accomplished by setting I1 so that the voltage at RF is -4V. Power dissipation during line shorts to ground is limited by the thermal limiting circuit, which supplies I2 to force the voltage at RF positive. This limits die temperature by reduction of the short circuit current.

SLIC-LC PIN DESCRIPTIONS (Refer to Fig. 4)

Pin 1 – T

This is an analog input which is connected to the TIP (more positive) side of the subscriber loop through A 150Ω Feed Resistor and a Ring Relay. It is used in conjuction with the RING lead to receive voice signals from the telephone and for loop monitoring purposes.

Pin 2–R

This is an analog input which is connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. It is used in conjunction with the TIP lead to receive voice signals from the telephone and for loop monitoring purposes.

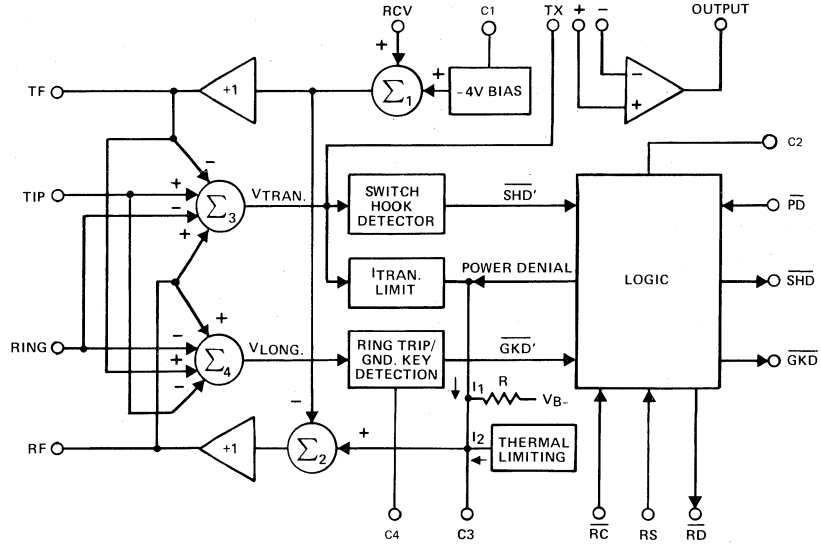
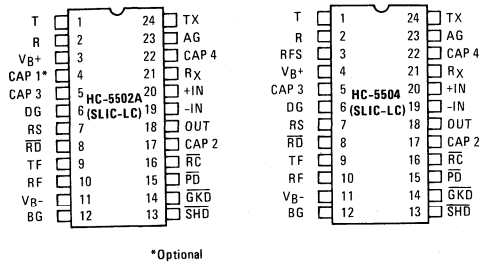


Figure 3. – SLIC LC Block Diagram



*Optional

Figure 4. SLIC-LC Pin Configurations

Pin 3

VB+; most positive supply for the HC-5502A. VB+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.

RFS; Ring Feed Sense for the HC-5504. Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.

Pin 4

C1; an optional external capacitor for the HI-5502A can be connected between this terminal and analog ground to further suppress noise appearing on the +12V supply. Typical value of this capacitor is 0.5μF, 5V. If this pin is unused it should be left open.

VB+; most positive supply for the HC-5504. VB+ is typically 12 volts with an operational range of 10.8 to 13.2V.

Pin 5

C3 (Capacitor #3); an external capacitor is to be connected between this terminal and analog ground. This capacitor is required for proper operation of the loop current limiting function, and for filtering the -48V supply. Typical value of this capacitor is 0.3 μF, 30V.

Pin 6

DG (Digital Ground); this is to be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC device.

Pin 7

RS (Ring Synchronization Input); this is a TTL compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source. This ensures that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If this feature is not required, then this pin should be tied to +5V.

Pin 8

$\overline{RD}$ ($\overline{Relay\ Driver}$); this is a low active open collector logic output. When enabled, the external ring relay is energized. Maximum RD voltage is 15V.

Pin 9

TF (Tip Feed); a low impedance analog output which is connected to the tip lead through a 150Ω $\pm$1% feed resistor. It is used in conjunction with the ring feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.

Pin 10

RF (Ring Feed); a low impedance analog output which is connected to the ring lead through a 150Ω $\pm$1% feed resistor. It is used in conjunction with the tip feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.

Pin 11

V_{B-} (Negative Voltage Source); most negative supply. V_{B-} is typically -48 volts with an operational range of -42 to -58 volts. This supply is frequently referred to as "battery".

Pin 12

BG (Battery Ground); to be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.

Pin 13

$\overline{SHD}$ ($\overline{Switch\ Hook\ Detection}$); a low active TTL compatible logic output. This output is enabled for loop currents exceeding 5.0mA and disabled for loop current less than 10.0mA.

Pin 14

$\overline{GKD}$ ($\overline{Ground\ Key\ Detection}$); a low active TTL compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 10mA, and disabled if this current difference is less than 20mA.

Pin 15

$\overline{PD}$ ($\overline{Power\ Denial}$); a low active TTL compatible logic input. When enabled the metallic loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.

Pin 16

$\overline{RC}$ ($\overline{Ring\ Command}$); a low active TTL compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).

Pin 17

C2 (Capacitor #2); an external capacitor can be con-

nected between this terminal and digital ground. This capacitor prevents false ground key indications from occurring during ring trip detection and may be omitted if $\overline{GKD}$ is not used. Typical value of this capacitor is 0.15 μF, 10V. This capacitor is not needed if the ground key function is not required, and may be left open or connected to digital ground.

Pin 18

Output; the analog output of the spare operational amplifier. The output voltage swing is typically ±5V.

Pin 19

-In; the inverting analog input of the spare operational amplifier.

Pin 20

+In; the noninverting analog input of the spare operational amplifier.

Pin 21

Rx (Receive Input, four wire side); a high impedance (90kohm) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through the 300 ohms of feed resistance on each side of the line.

Pin 22

C4 (Capacitor #4); an external capacitor is to be connected between this terminal and analog ground. This capacitor prevents false ground key indications from occurring when large longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. Typical value of this capacitor is 0.5 μF to 1.0 μF, 20V. This capacitor should be nonpolarized.

Pin 23

AG (Analog Ground); to be connected to zero potential and serves as a reference for the transmit output (Tx) and receive input (Rx) terminals.

Pin 24

Tx (Transmit Output, four wire side); this is a low impedance (10Ω max) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the spare op amp of the SLIC device) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

HARRIS

APPLICATION NOTE

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ADDITIONAL INFORMATION ON THE HI-300 SERIES SWITCH

BY CARL WOLFE

INTRODUCTION

The introduction of the HI-300 series of CMOS analog switches is the latest addition to the HARRIS switch family and gives the designer a viable second source to the Siliconix DG 300 series analog switch.

This family of monolithic, dielectrically isolated, CMOS analog switches consists of twelve products, the HI-300 thru HI-307 and the HI-381 thru HI-390 are designed for TTL level compatibility (logic "0" = .8V, logic "1" = 4.0V). The HI-304 thru HI-307 are CMOS compatible (logic "0" = 3.5V, logic "1" =11V).

The HI-300 series features low and nearly constant on resistance over analog signal range, low leakage and minimal power dissipation.

IMPROVED PERFORMANCE

An understanding of what a designer would consider important in an analog switch is useful in order to illustrate the advantage of the HI-300 series. Although any parameter could be considered important for a particular application, there are certain parameters considered to be most critical for the majority of applications. These parameters are:

"on" Resistance (Ron)
leakage current (I_{SOFF}, I_{DOFF}, I_{DON})
switching speed (ton, toff)
power supply current (I+, I-)

These parameters are important because the majority of designs require either high accuracy, speed, or low power dissipation.

ON RESISTANCE

In high accuracy systems, such as data acquisition systems, the designer would be concerned with minimizing errors caused by "on" resistance and leakage currents. An inverting programmable gain amplifier shown in Figure 1 will help illustrate the need for low on resistance and leakage current in high accuracy systems.

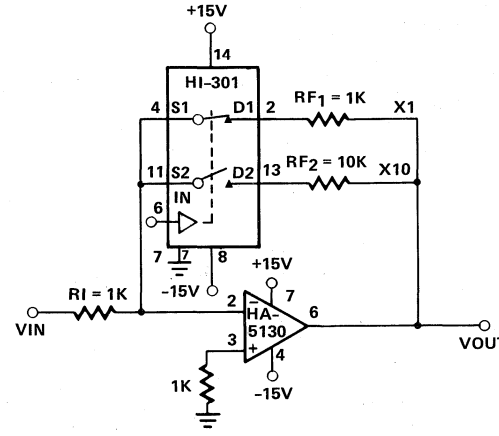


Figure 1 — Inverting Programmable Gain Amplifier

Ideally, the voltage gain of this inverting amplifier would be, $A_V = -(R_F/R_I)$. But when using a switch to program the gain, its characteristics must be taken into account and the amplifier gain equation must be modified to $A_V = -(R_F + R_{ON}/R_I)$. The higher the on resistance of the switch, the greater the gain error. Variations in the on resistance of the switch will also effect the gain error.

LEAKAGE CURRENT

Another source of error occurs in the switch "off" state, where leakage current causes offset voltage errors. In Figure 1, leakage current flowing through the feedback resistor creates an output voltage error equivalent to the expression, $V_O = R_F \times I_{DOFF}$.

SWITCHING SPEED

A designer concerned with switching times would

obviously be sensitive to the ton and toff specifications. A low value of "on" resistance is also important, since this resistance increases the RC time constants and can slow the circuits overall performance.

POWER SUPPLY REQUIREMENTS

The last critical parameter would be power consumption. There are certain applications where power supply currents are the primary concern of the designer. Examples would be portable or battery operated equipment.

The majority of switch applications require critical performance in one or more of the areas just discussed. The HI-300 series offers improved performance in each of these areas. The following tables compare the HI-300 series with existing HARRIS switches. Table 1 contains maximum specifications for T = 125°C and Table 2 consists of typical values at T = 25°C.

+125°C Maximum Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	t_{ON}	t_{OFF}
HI-200	125Ω	500nA	2mA	500ns	500ns
HI-5040	75Ω	500nA	.3mA	1000ns	500ns
HI-300	75Ω	100nA	.1mA	300ns	250ns

Table 1 — Switch Comparisons at T=125°C

+25°C Typical Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	t_{ON}	t_{OFF}
HI-200	55Ω	1nA	.5mA	240ns	330ns
HI-5040	25Ω	.8nA	.3mA	370ns	280ns
HI-300	30Ω	.1nA	.23μA	210ns	160ns

Table 2 — Switch Comparisons at T=25°C

From these tables it should be clear that the HI-300 series offers improved performance to the designer.

INSIDE THE HI-300

Figure 2 shows the schematic of the digital input and driver stages of the HI-300. The purpose of this stage is to take the logic level signals and condition them to drive the gates of the FET switch cells.

The HI-300 series has a digital input protection circuit consisting of a 200Ω series resistor and clamping diodes, D1 and D2, to the supplies.

These diodes will quickly discharge any static charge which might appear at the digital inputs.

The F. E. T. Devices N1 thru N5 and P1 thru P5 form the input buffer and level shifter which establishes the proper voltages to drive the switch cell. N6, N7, P6, and P7 form the output buffers which isolate the level shifter from the capacitive load of the switch cell.

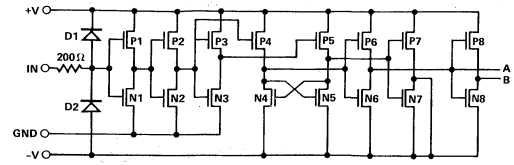


Figure 2 — Partial Schematic

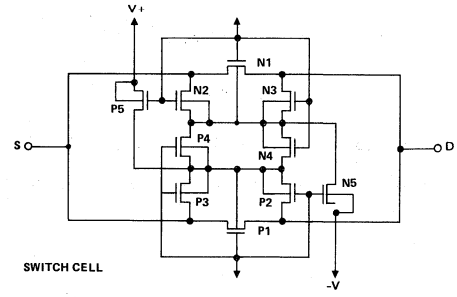


Figure 3 — Schematic

The switch cell shown in Figure 3 is based on the FET devices N1 and P1. The remaining devices, N2 thru P5 serve various functions, such as reducing leakage current, minimizing on resistance variations and minimizing charge injection.

ADDITIONAL PERFORMANCE CHARACTERISTICS

(A) SINGLE SUPPLY OPERATION

The HI-300 series has the capability of single supply operation. These switches can operate to a minimum supply of +5 volts, although designers must be aware of the trade off which exists at these levels. The trade off is the performance of the switch will vary as the supply level varies. Examples of these performance variations are increased on resistance and slower switching times. So, a HI-300 series switch with a single five volt supply will have higher on resistance and slower switching speeds then the same device at ±15 volts or even a single +15 volt supply.

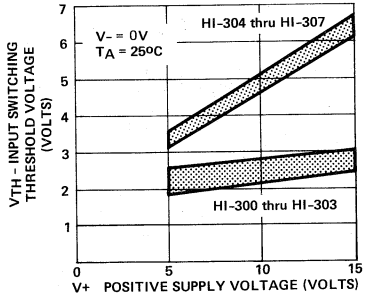
The explanation for these variations can be found in the F.E.T. devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of the FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times. The higher resistance reduces the available current

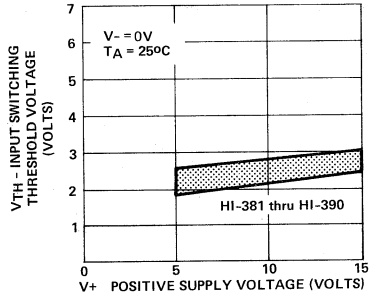
needed to charge the internal capacitances of the switch. Lower charging current directly relates to the slower switching times.

The explanations, just given, along with the following typical curves of the HI-300 single supply operation, should aid the designer in applying the HI-300 series in single supply applications.

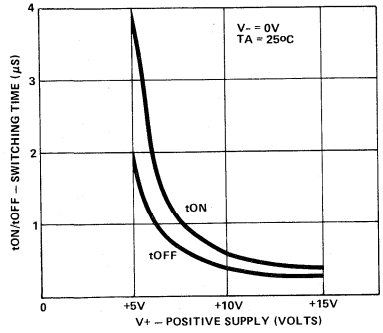
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 THRU HI-307



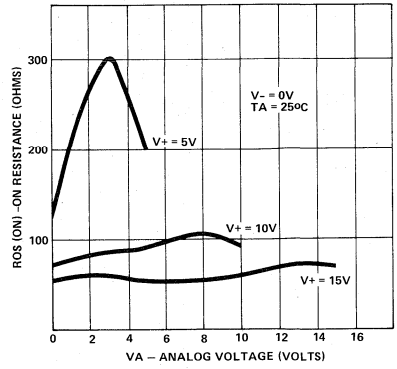
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



SWITCHING TIME VS. V+ - POSITIVE SUPPLY VOLTAGE



RDS(ON) VS. ANALOG AND POSITIVE SUPPLY VOLTAGE WITH V- = 0V



B) CHARGE INJECTION

The charge injection of a switch is a critical parameter for certain applications, such as small signal switching or sample and hold circuits.

For the case of small signal switching, unwanted switching spikes result from this transferred charge causing system errors. These spikes are created when the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances, as shown in Figure 4. The magnitude of these switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch.

For the sample and hold circuit, shown in Figure 5, a common problem is sample to hold offset error. It is caused by the same mechanisms discussed for the small signal application, but in this case the charge is transferred to the hold capacitor and an offset voltage is created. The voltage is determined by the following relationship. V = Q/CH.

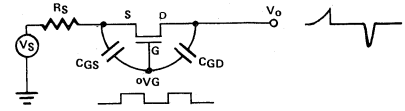


Figure 4 — Charge Transfer

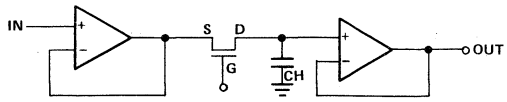


Figure 5 — Sample and Hold

Charge injection can create problems in the type of applications just described. A typical curve of the HI-300 series charge injection performance is shown in Figure 6 as an aid to designing in these type of circuits.

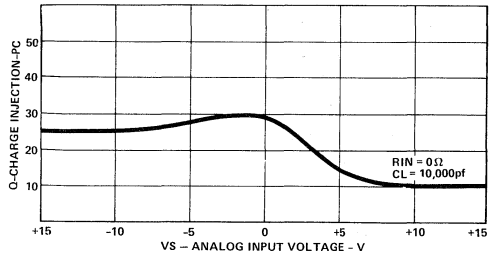


Figure 6 — Charge Injection vs. Input Voltage

APPLICATION HINTS

A\ POWER SUPPLY CONSIDERATIONS

The HI-300 series analog inputs do not feature overvoltage protection. External protection circuitry would be necessary if the switches were subjected to possibly destructive situations.

An example could be an overvoltage condition where the power supplies to the switch go down while an analog input signal is still present. A common misunderstanding is that the switch will be open and block the input signal, when actually the opposite occurs.

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 7, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transistors which are shown in Figure 7 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

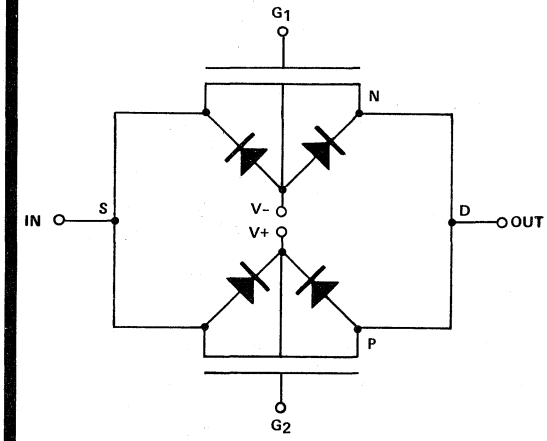


Figure 7 — Basic CMOS Transmission Gate

Another situation occurs if the power supplies are open circuited, the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with input signals less than those used for supply will operate properly.

A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Referring to Figure 7, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will become forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 8. This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and a current path to ground will exist. This protects the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diodes.

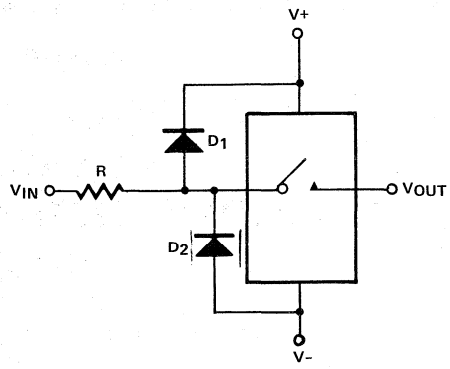


Figure 8 -- Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reversed biased and the signal will not pass through the switch.

The protection network may introduce unwanted error into the circuit in the form of leakage current and increased on resistance. It is recommended that low leakage diodes be used, such as Schottkey diodes. If the switch is looking into a high impedance, such as the input operational amplifier, the error introduces by the increased on resistance will be negligible.

The protection circuit just discussed is not used to prevent the switch from latch up. The HI-300 series switch is constructed using the HARRIS dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FETS.

An alternative to protection circuits takes advantage of CMOS technology. Assume an overvoltage condition exists where the input exceeds supply. Rather than use external components to protect the device, it may be possible to shift the supplies in order to accomodate the input signal. An example would be an application with ±15 volt supplies, but attempting to switch a +18 volt input signal. A possible solution would be to shift the supplies to V+ = +20V and V- = -10V and now the input signal is within the existing supplies. In some applications the supply voltage can be adjusted in order to pass larger input signals.

ACKNOWLEDGEMENT

A. Engineering staff of Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901, particularly Frank Cooper, whose useful comments contributed to this publication.

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(2) Don Jones, "CMOS Analog Multiplexers and Switches' Applications Considerations" Harris Application Note 520.

(3) Ernie Thibodeax, "Getting the most out of C-MOS devices for analog switching jobs", Harris Application Note 521.

(4) Hunter, Bill, CMOS DATA BOOK: Tab Books, 1978.

HARRIS

APPLICATION NOTE 535

DESIGN CONSIDERATIONS FOR A DATA ACQUISITION SYSTEM (DAS)

BY TARLTON FLEMING

INTRODUCTION

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks", rather than a description of the block components and their error contributions. This latter information may be found in the Bibilography under "General".

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application. Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

DATA ACQUISITION SYSTEM ARCHITECTURE

At present the most widely used DAS configuration is that shown in Fig. 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required), track/hold amplifier and A-D converter.

A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Fig. 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Fig. 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters often included to reduce aliasing errors and noise are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Fig. 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Fig. 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

Further discussion will center on Fig. 1, both in the single-ended version shown, and in the differential version.

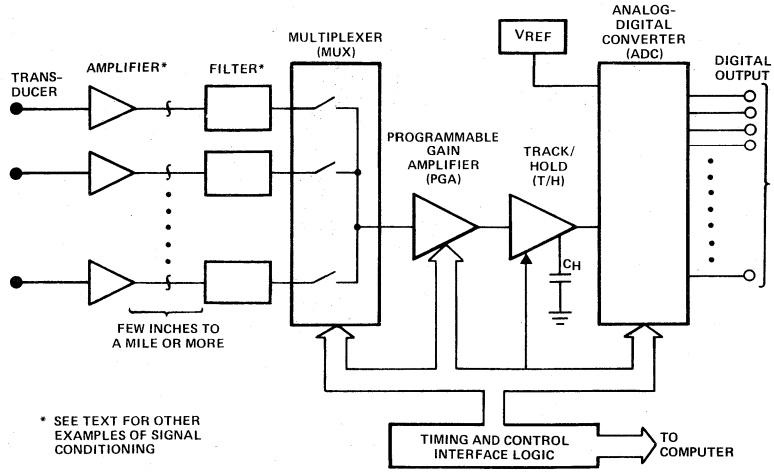


FIGURE 1. Typical Data Acquisition System

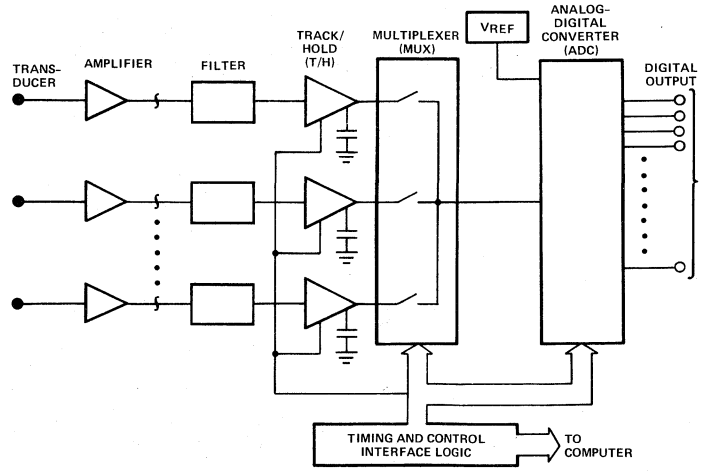


FIGURE 2. DAS System For Simultaneous Sampling Of All Channels

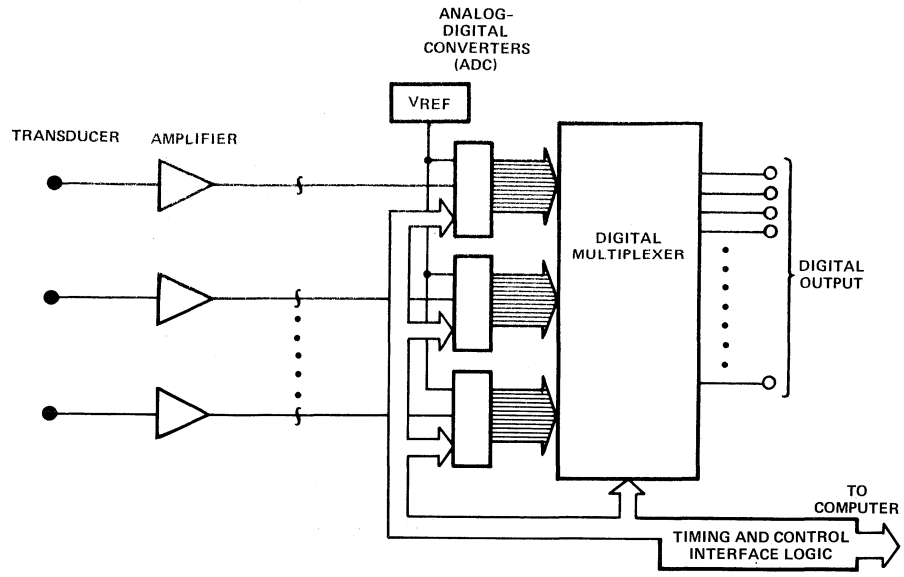


FIGURE 3. High Accuracy, Multi-Converter DAS System

SIGNAL CONDITIONING

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to current conversion (4 to 20 mA; 10 to 50 mA)
- rms to dc conversion
- Logarithmic signal compression
- Common mode rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

TRANSDUCERS

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, dc voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100 mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following Sections.

SINGLE-ENDED VS. DIFFERENTIAL SIGNAL PATHS

Consider the transducer output. A high level signal (100 mV to 10 V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as "pickup" during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return. (see Fig. 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

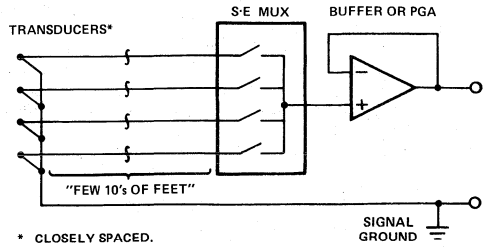


FIGURE 4. Single-ended Data Paths

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100 KHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Fig. 5).

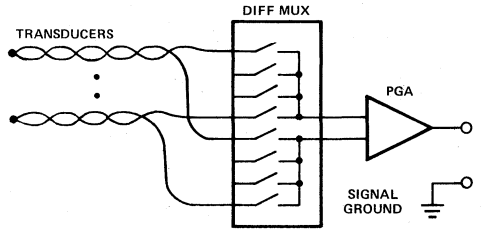


FIGURE 5. Differential Data Paths

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier will provide low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Fig. 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the "flying capacitor" multiplexer of Fig. 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay's 1 ms response time can be a limitation.

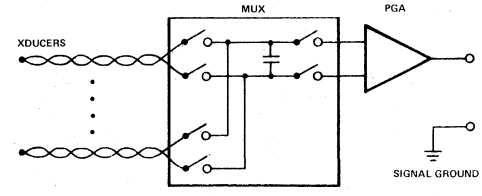


FIGURE 6. "Flying Capacitor" multiplexer using reed relay switches for high CMV signals.

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Fig. 6. For example, magnetically isolated amplifiers are rated at 2KV and up with a small signal bandwidth of approximately 2 KHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include ±15V terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated isolation amplifiers are available with $f_{-3dB} = 15KHz$ and 2KV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

LOW LEVEL SIGNALS

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below 50μV rms.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large dc errors should not be used for low level signals. Passive filters on the other hand, are restricted to two or three poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the Section titled Filters).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in-phase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

The table of Fig. 7 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values for inductance.)

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10KHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

FIGURE 7. Impedance of Electrical Connections, +20° C

As an example, suppose the ADC in Fig. 1 has 12-bit resolution, and the system accuracy is to be ± ½ LSB (± 1.2mV). The interface logic might draw 100 mA from the + 5V supply. Flowing through six inches of #24 wire, this current produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

FILTERS

The presampling or anti-aliasing filters shown in Fig. 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Fig. 8 preserves some degree of impedance balance on the line.

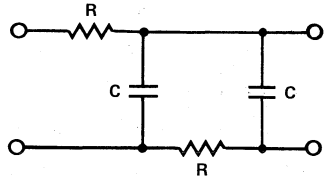
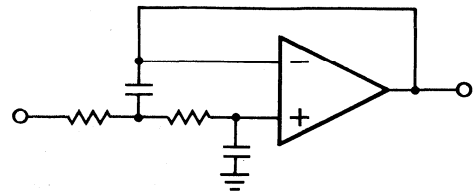


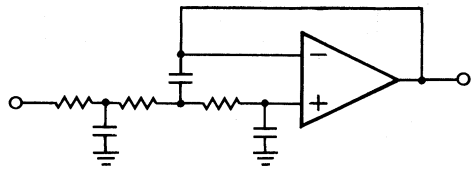
FIGURE 8. A Passive, Two Pole, Low Pass, Differential Input Filter

A low-pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two and three pole sections shown in Fig. 9. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles vs. accuracy requirement.



a. TWO POLE SECTION



b. THREE POLE SECTION

FIGURE 9. Butterworth Low-Pass Filters

PROGRAMMABLE GAIN AMPLIFIER (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2, some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing (FS = Full Scale).

Considering resolution as referred to the input level, a 12-bit converter digitizes an input of .06FS to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.

2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample) /Holds and A-D converters.

3. Common Mode Rejection (CMR). When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Fig. 10 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.

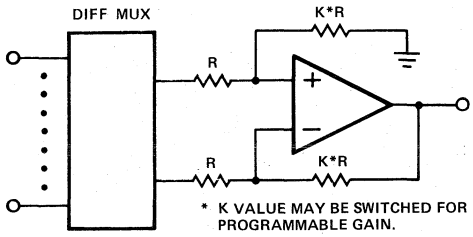


FIGURE 10. Subtractor or Pseudo-Differential PGA

Fig. 11 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.

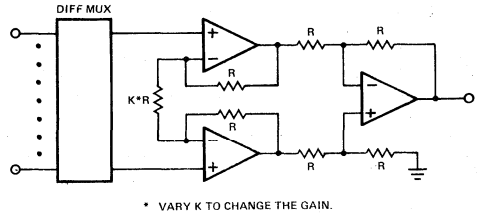


FIGURE 11. Full Differential PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note RESULT
- Iterate until (FS/2 ≤ RESULT ≤ FS)

SAMPLING RATE

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data; but if a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner low bandwidth channels may require a high speed DAS, according to the relationship:

System Sample Rate = (Highest Channel Rate) X (Number of Channels)

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Fig. 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earler, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_S.
2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_S.
3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as ± ½ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided they occur at an acceptable location relative to the cutoff frequency.

Fig. 12 shows aliasing error due to the signal spectrum alone vs sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For ± ½ LSB error in a 12-bit system (± .01%), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Fig. 12 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

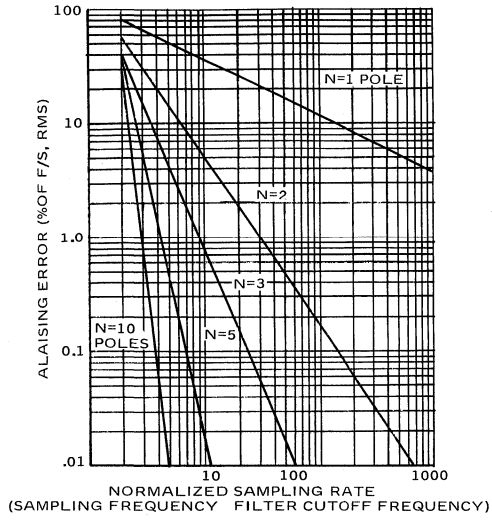


FIGURE 12. Effect of Filter Poles on Aliasing Error

COMPUTER INTERFACE

The typical DAS we have described (Fig. 1) requires several control signals:

- Mulitplexer Channel Address
- PGA Gain Address
- Track/Hold Control
- A-D Converter
  - Start Convert
  - MSB Invert
  - Short cycle
  - Unipolar/Bipolar
  - Output Byte Enable
  - Conversion Interrupt etc.

This control can be provided directly by the computer, but some portion of these signals is usually supplied by an intermediate block of control logic. For monitoring predictable channel data, the DAS can repeatedly scan through its channels, trigger the converter, and notify the computer when each data sample is ready. This independent operation can be accomplished by a clock and counter arrangement to supply channel and gain addresses, plus a dual "one shot" multivibrator (74123) to gate the Start Convert and Track/Hold functions.

To handle a sudden change in data level or other unexpected event, the computer must be able to random access any channel or PGA gain. Provision is made to write this information to the DAS via the computer's data or address bus, using appropriate address decoders and latches.

When processing higher bandwidth signals, one error source to be minimized is the Track/Hold's aperture delay uncertainty, or jitter. The logic which generates the T/H control signal needs close attention, since jitter in this waveform adds to that specified for the device itself.

Finally, the DAS output consists of a serial stream of parallel digital words from the converter, synchronized with the converter's status signal indicating when the data is valid. Techniques for passing this data to the computer include direct memory access (DMA), memory mapping, and mapping via a dedicated I/0 port, all with or without an external interrupt of the processor.

DMA is most efficient for the high speed transfer of large volumes of data. This can proceed by program request, resulting in the movement of a block of data to a designated sequence of memory locations, at a speed limited only by the memory cycle time. As an alternative, hardware can be configured to allow transfer of a data word during every non-memory machine cycle. This allows an almost continuous output of data from the DAS. The transfers are asynchronous and unsolicited by the program with only a slight increase in software execution time.

For less demanding data rates the choice is between an I/0 or memory mapped interface. The former is best for small systems. For example, the 8085 microprocessor can control up to eight I/0 devices without external address decoding. Addition of decoders expands the field from 8 to 256 peripherals.

There is a range of applications for which the choice of I/0 or memory mapping is not clear, but memory mapping becomes attractive with increasing system complexity. The memory reference instructions available with this approach simplify programming and speed execution. A further increase in throughput is obtained by use of the processor's interrupt system, allowing the main program to proceed while an analog-to-digital conversion is in progress.

Memory mapping plus interrupt is very effective; however, the software overhead associated with service of an interrupt-driven I/0 interface results in a diminishing advantage as the required throughput rate increases. Again, DMA offers the advantage for high data rates.

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HARRIS

APPLICATION NOTE 536

TIME WINDOW NAILS DOWN D-A CONVERTER'S SETTLING TIME

BY STEVE MOHR

INTRODUCTION

The speed of digital-to-analog converters has increased so rapidly in recent years that several models now have settling times that cannot be measured directly with standard test equipment. Fortunately, an alternative is available. A newly developed technique—a modified time-window scheme—provides accurate and repeatable measurements of settling time. Measurements are possible from several microseconds down to a few nanoseconds—even for current-output d-a converters with high resolution (more than 8 bits).

The measuring circuit uses a fast and accurate strobed comparator, the HA-4950, instead of a window amplifier (Fig. 1). The comparator senses the point at which the converter's output enters the specified error band around the final value. There is no arbitrary load at the output and little added capacitance.

The HA-4950 can detect a 100-μV differential input within 150ns, making it more than accurate enough to measure the settling time of a 12-bit d-a converter. Because there is a risk of comparator input saturation, the converter's output should be clamped with Schottky diodes.

The converter acts as a current sink. Therefore its full-scale output has a negative value. When the converter is being turned off, its output swings from the negative clamped value (approximately 400mV) to almost zero. When it turned on, however, the output starts at near zero and swings to the negative clamped value, making the measurement invalid, because current now flows through the diode.

Therefore, for turn-on measurements, an opposing current should be injected at the output node to offset the final value to zero and thus turn off the diodes. Many monolithic d-a converters have an on-board resistor intended for bipolar operation of the converter. The on-board resistor is an excellent stable current-injection source if a bias voltage, V_{bias}, is applied to it.

This technique is useful in overcoming many of the problems associated with measuring settling time. A look at some of these problems may be helpful.

SETTLING TIME: THE BASICS

The settling time of a d-a converter is defined as the time required for its output to settle within a given percentage of the final value following a change in the digital input code. The error band around the final output value is often expressed as a fraction of a least significant bit instead of as a percentage of the output.

A 12-bit d-a converter has 4096 possible input codes and the same number of output values. Each input code corresponds to a unique output value. Transitions from one state to another may have vastly different settling times, depending on the magnitude of the current swing from one state to another and on the number of switches involved. For a designer who wishes to use the full dynamic range of a d-a converter the worst-case settling time is the important parameter.

SETTLING TIME IS HARD TO MEASURE

The settling times are higher at the so-called "major carry" transitions, which involve the largest number of switch changes for a single code change at the input. An example of a major carry is the change from an input code of 011 . . . 1 to 100 . . .0. In this case the output changes by only 1 LSB, but all of the switches come into play. Usually, though, the worstcase settling time occurs when the converter is required to slew across its full dynamic range. This is known as the full-scale settling time. A full-scale change occurs when the input code changes from 000. . .0 to 111. . .1, or vice versa.

Consider the full-scale transition of a 12-bit d-a converter. For a full-scale output current of 2mA (a commonly specified value) and a resolution of 1/2 LSB (0.01%), the dynamic range is 80dB. Then, if

the current output is loaded to produce a voltage that can be viewed on an oscilloscope—say, 10V full scale—the scope must be set to a scale that will allow approximately 1mV to be resolved.

With most scopes, the gain must be set very high to resolve a signal of 1mV or less. Therefore the scope amplifier will saturate when presented with a 10-V input signal. As the converter's output begins to slew from 10V to 0V ±1mV, the scope will remain saturated for almost the entire duration of the output swing. Then, when the output finally falls within the range of the scope, the saturated scope amplifier will have to respond very quickly to catch up.

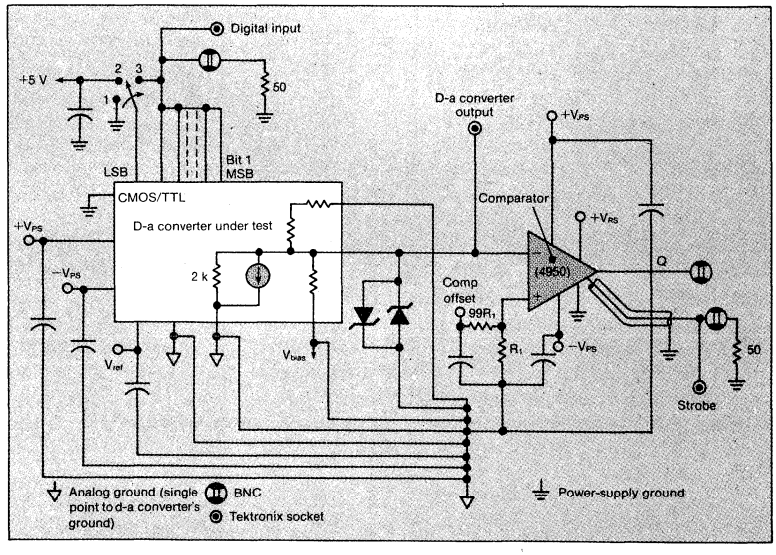
It is probably safe to say that there is no scope capable of such a feat. Usually scope recovery times run to many microseconds and, in some cases to over a millisecond.

A partial solution to the recovery time problem is to limit the d-a converter's output-voltage swing severely by adding shunt-diode clamps. This technique allows the converter's output current to swing through its full range—but without producing a correspondingly high voltage at full scale. However, even the reduced voltages (less than 1V) will still saturate many scopes on their most sensitive ranges.

ACCOUNTING FOR LOADS

Another important consideration in measuring settling time is the allowable load condition at the converter's output. Essentially, the output circuit consists of the equivalent resistance of the divider and the equivalent capacitance of the parasitics on the network. Thus, to a first approximation, the output circuit can be regarded as a single-pole RC network, which has an associated time constant from which the settling time may be estimated. However, this is only an approximation, because both the resistance and capacitance are actually distributed along the divider network.

Usually, a scope probe cannot be used as the d-a converter's load, because it would add excessive capacitance of 10 to 30pF. Some FET-input probes do have an acceptably low capacitance—as little as 1pF—but they tend to have other undesirable characteristics, such as a long tail for large signals, which can obscure a settling-time measurement.



1. The test circuit for measuring the settling time of digital-to-analog converters uses a monolithic comparator, here a type HA-4950, in a modified time-window scheme. As with all sensitive analog measurements, single-point grounding is required to avoid ground loops, a cause of errors.

SOLVING A CAPACITANCE PROBLEM

One solution to the output capacitance problem is to terminate the output with a low resistance. In fact, some manufacturers recommend this approach. But the method has both pros and cons.

A d-a converter like the HI-562A has an output resistance of 2kΩ and an output capacitance of about 10pF. If the output were terminated in, say, 75Ω, the equivalent output resistance would be about 72Ω. The time constant of the open-circuit convert (2kΩ in parallel with 20pF) is 40ns. Its settling characteristic to within 0.02% can be approximated by nine time constants, resulting in a settling time of 360ns. With a 75Ωtermination, however, the time constant becomes 1.44ns, which yields a settling time approximation of 13ns.

Of course, nobody really believes that a 12-bit d-a converter can settle to 0.01% in 13ns. Because the method greatly reduces the RC effects of the ladder network, it tends to present an optimistic picture of the converter's switching performance.

Consider also the full-scale range of a d-a converter terminated in 75Ω. The full-scale range voltage will be 150mV—that is, 2mA X 75Ω. But the error band that must be resolved is only 15 μV, a very small value indeed to measure with off-the-shelf equipment. Therefore the outputs must be amplified—and by an amplifier that settles more quickly than the d-a converter.

But the need to amplify the output signals poses several new problems. The amplifier must be very fast, because the converter is expected to settle in well under 1μs, and few monolithic amplifiers even specify the settling time to 0.01%. Consequently, a less exact measurement must be made, and the actual settling time must then be estimated.

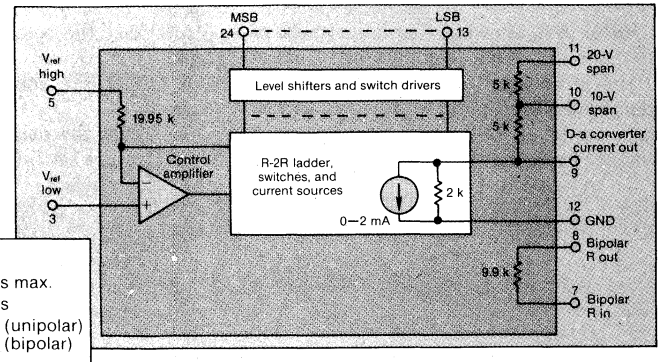
It is doubtful that many applications actually call for a termination resistance as low as 75Ω. One of the more common uses for a d-a converter is as a component for an analog-to-digital converter. The modified time-window measurement technique suggested closely resembles the standard configurations used in successive-approximation a-d converters. And, of course, the measured results closely mirror the performance in actual applications.

MANY DIFFERENT MEASUREMENTS POSSIBLE

Many different settling-time measurements are possible with the new technique, but the most difficult is the one for the transition between zero and full scale. For this measurement, the d-a converter's inputs are pulsed from all on to all off, and vice versa. The comparator is strobed during the on or off portion of the cycle, depending on whether turn-on or turn-off is to be measured. It is important that the digital pulse widths be made long enough to allow 100% settling of the d-a converter. However, they should never exceed 50μs, because the accuracy of the HA-4950 may be upset if its input terminals are held out of balance for too long.

To adjust the offset of the comparator, a precise voltage must be applied to one of the input terminals. This is done by using a resistive divider with a ratio of at least 100:1 thus allowing fine adjustment of the offset voltage. The comparator's offset establishes the error band. Also, the comparator measures the zero-crossing point for turn-on, as well as the actual size of an LSB.

Measurement of settling time to within fractions of an LSB is convenient, because an LSB is the



Specifications	
Settling time to ±½ LSB	400 ns max.
Resolution	12 bits
Output current	2 mA (unipolar) ±1 mA (bipolar)
Output resistance	2 kΩ
Output capacitance	20 pF
Reference input voltage	10 V
Reference input resistance	20 kΩ

2. To illustrate the measurement technique, a 12-bit monolithic d-a is used as the device under test. The HI-562A has a specified settling time of 400ns to within ±1/2LSB. Some of the on-chip resistors are used as part of the test circuit to minimize drift.

smallest discrete output available form a d-a converter. Therefore, before settling time can be measured, the size of an LSB (that is, the absolute voltage value) must be determined first. For a particular d-a converter, this size may differ form the ideal value. Measurement of the LSB also takes into account tolerances in the resistive divider used for comparator offset.

STEP BY STEP PROCEDURE

The procedure for measuring settling time can be summarized in eight steps:

1. Decide on the settling time to be measured—full-scale, MSB, etc.
2. Configure the digital inputs accordingly.
3. Set up the necessary pulse widths and duty cycle.
4. Measure the size of an LSB.
5. Offset the comparator to establish the error band.
6. Offset the converter's output with injected current.
7. Adjust the delay on the comparator strobe.
8. Measure settling time from the digital pulse to the strobe pulse.

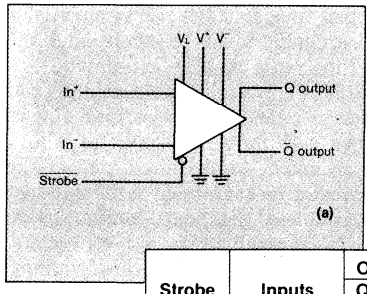
Assume the HI-562A is under test. A simplified functional diagram of the d-a converter is shown in Fig. 2, along with a list of some of its nominal specifications.

The converter has a specified maximum settling time of 400ns to within ±0.01%. This error band is equivalent to approximately 200nA. However, the actual measurement will involve a voltage rather than a current.

Without the Schottky diodes, the output current flows through the parallel combination of the converter's output resistance (2kΩ), the two span resistors in series (10kΩ total), and the bipolar offset resistor (9.9kΩ). Thus the full-scale range is approximately 2.9V. Since the converter has 12-bit resolution, the settling time should be measured to within 350μV, which corresponds to ±1/2LSB.

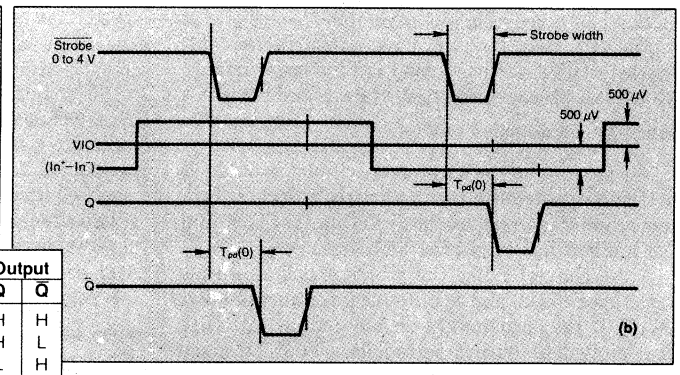
Fortunately, the HA-4950 comparator (Fig. 3) has resolution down to 100μV, with a delay of only 150 ns. That makes it possible to measure the converter's settling time to within the specified error band. With this comparator, settling-time measurements to within ±350μV become straight-forward and repeatable. In fact, the technique can be automated if necessary.

In measuring settling time to turn-off, the Schottky diodes restrict the output voltage to ±380mV. As the converter switches from all bits on to all bits off, the output current swings from a full-scale value of -2mA to almost zero. The clamped output voltage, however, begins at -380mV and settles near zero. Since the final value does not need to be offset, the V_{bias} point should be grounded (OV) for this measurement.



Strobe	Inputs	Output Q	Output $\bar{Q}$
H	Don't care	H	H
↓	$In^+ > In^-$	H	L
↓	$In^+ < In^-$	L	H
L	Don't care	Q_0	$\bar{Q}_0$

Q_0 the latched state



3. The HA-4950 precision comparator was chosen for the test circuit because it has 100-mV resolution in only 150ns. This resolution and speed allow it to sense the output level of a d-a converter much faster than with the usual oscilloscope measurement.

FACTORS THAT LIMIT A D-A CONVERTER'S SPEED

Practical constraints limit the speed of digital-to-analog converters. They can easily be seen with an understanding of how the converters work.

Basically a d-a converter decodes the digital input and uses the information to switch a voltage or current to the output—usually via a resistive ladder network. The total delay—from the time at which an input transition occurs until the output reaches its final value— is the sum of several contributing factors. They are the propagation delays through the decoder section, the actual time required for the switches to change state, and the effects of stray RC time constants associated with the ladder and the output amplifier.

A d-a converter can be regarded as simply a digitally controlled current or voltage source.It produces an output (current or voltage) that is proportional to the coded input multiplied by the reference input (which may be fixed or variable). In the faster d-a converters available, a current is steered to the output via a divider network and a set of transistor switches. A portion of the reference current appears at the output, depending on the value of the digital input.

Voltages, rather than currents, can be switched to produce a voltage-output d-a converter. But the process is slower because of charging effects associated with the junction capacitance of the switching transistors and because of process-dependent parasitic capacitances along the divider network. Therefore for applications requiring a fast voltage-output converter, engineers often use a current-output converter together with an operational amplifier connected as a current-to-voltage converter. In fact, several manufacturers supply the amplifier in the same package as the converter to facilitate and ensure compatibility.

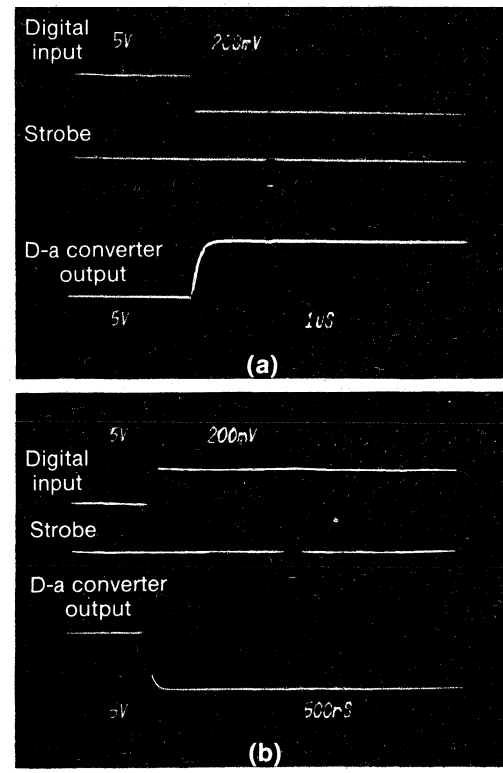
The digital inputs for the converter are produced by a suitable function generator, such as the EH-135A. To allow plenty of time for the d-a converter to settle, the digital pulses are set up for a period of 50μs and a duty cycle of 50%. The strobe pulse for the HA-4950 comparator should have a high state of 2V and a low of 0.8V. It should have a width of about 60ns. An accurate voltage source, such as the Precision Devices 2020, is divided down by about 100:1 to provide the offset voltage for the comparator.

The offset should be set to the final value of the converter's output voltage, with an additional $\pm$1/2 LSB for turn-on tests and $\pm$1/2LSB for turn-off. For both measurements, the output from the converter will settle to near zero. The comparator, used as a zero-crossing detector, establishes the final value with a high degree of certainty.

MEASURING THE WEIGHT OF AN LSB

As stated, before settling time can be measured, the value of an LSB must be determined. To do that, the delay of the comparator strobe should first be adjusted so that it triggers well after the converter is known to have settled—say, 10μs after the falling edge of the digital pulse at the converter's input. To check that the converter is indeed switching and settling, a scope probe should be placed on the output. But be sure to remove the probe before proceeding to the next step, because it will almost certianly disturb the measurement.

The next step is to set the comparator's offset voltage to zero and observe the output of the comparator on the scope. Then turn on the least significant bit. The rest of the bits are now being driven



4. Before the actual settling time can be measured, an offset voltage must be determined so that the d-a converter's output can be held near zero for the time measurement. The oscilloscope waveforms shown are for the turn-off(a) and turn-on (b) for this set-up phase of the procedure. Note that the converter's output, marked with an asterisk, will not be seen at the same time as the other waveforms, because the scope probe must be removed to avoid capacitive loading.

by the pulse generator but the LSB is maintained in a high state. That means that the converter's output will swing from -390mV to 0V minus 1LSB. The comparator output, Q, should then be high.

Next the comparator offset voltage is adjusted until the comparator's output trace has equal brightness for both high and low states (indicating that each pulse is present for about half of the sweeps of the scope trace). The offset voltage should then be measured with a voltmeter and recorded. The scope waveforms for the setup procedure are shown in the photos in Fig. 4.

With basically the same procedure, the final settled value of the converter's output can be determined. It will be close to, but not exactly, 0V. First, the comparator strobe is adjusted so that it occurs several microseconds after the on-off transition of the converter. Then the comparator offset is adjusted until the comparator's output trace has equal brightness for both logic states. This offset voltage is the true final value of the converter's output.

After the exact value of an LSB has been measured, including errors in the comparator offset divider, then the settling-time measurement can be attempted.

FINALLY, THE SETTLING TIME

To measure turn-off time, the comparator's offset voltage is set to the final value minus 1/2 LSB (that is, half a measured LSB). The delay of the comparator strobe pulse is adjusted to a point where the converter has surely settled—several microseconds after the falling edge of the digital input pulse for the converter. Next advance the delay until the scope traces are of equal brightness. Then, the time from the edge of the digital pulse to the leading edge of the comparator strobe (not the comparator output) should be measured. This value is the settling time of the converter to within 1/2 LSB. Figure 5 shows scope waveforms for both turn-on and turn-off settling-time measurements.

To measure turn-on time, the output of the converter must be offset to within the voltage range imposed by the Schottky diodes. This is done by applying a bias voltage to the V_{bias} point.

To begin, all the digital input bits of the converter are turned on. The output will then be clamped to the most negative level the diodes will allow (approximately -380mV). The bias voltage is then adjusted until the converter's output level is very nearly zero. Next, the delay of the comparator strobe is adjusted, as before, to several microseconds beyond the switching point. In this case, of course, the switching point of interest is the rising, rather than the falling, edge of the digital pulse.

As before, the final value of the converter's output is measured. Then the offset is set to the final value + 1/2LSB, and the strobe delay is adjusted from its original value of several microseconds to a lower value—thus moving the strobe pulse toward the rising edge of the digital input pulse. When the trace of the comparator output has faded to half its normal brightness, the settling time is measured from the edge of the digital pulse to the edge of the comparator strobe.

Though the measurement technique is, theoretically, highly accurate, the test results will become inaccurate unless care is taken with the layout and physical assembly of the test fixture.

BREADBOARDING REQUIRES CARE

Accurate resolution of small analog signals (a millivolt or less) requires careful elimination of resistive losses and noise interference. Noise in a test fixture can lead to erroneous or ill-defined test results—or can even make a measurement impossible. A few rules of thumb go a long way toward eliminating noise problems:

- Use separate analog and digital grounds connected at a single point.
- Tie all analog grounds to a single point.
- Use an on-board span resistor for the bias input.
- Ground unused pins.
- Shield the strobe input.
- Minimize lead lengths.
- Solder bypass capacitors close to device pins.

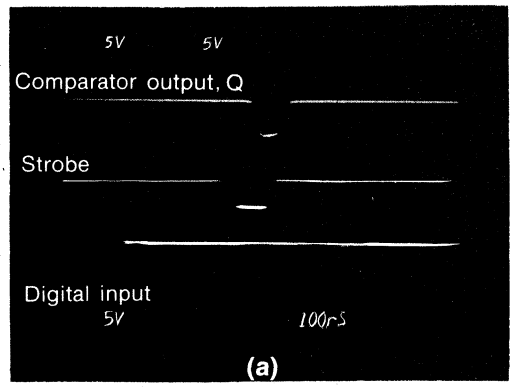
If the test fixture uses a printed-circuit board, it is a good idea to etch separate ground planes for analog and digital grounds. The two planes should be connected at a single point. That helps isolate the effects of digital switching from the low-noise analog ground.

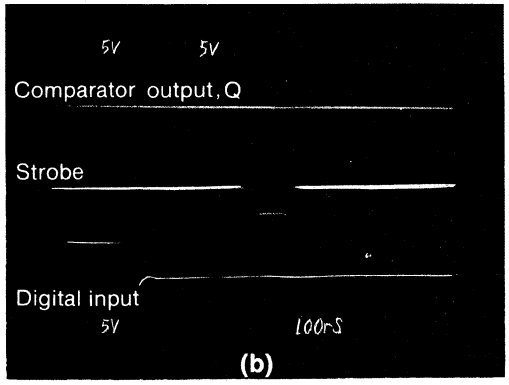
The analog ground can be kept free of ground-loop currents if all ground connections are made to a single point. Care should be taken to minimize the length of leads and circuit-board traces and to shield those that carry time-varying signals.

The d-a converter in Fig. 1, an HI-562A, has built-in span resistors and an offset resistor for bipolar operation. One of these on-board resistors should be used for the bias-voltage source, and any unused span resistors grounded. The converter and the comparator should be separately bypassed with capacitors placed as close as possible to their power supply pins. To ensure adequate bypassing at various frequencies, tantalum or electrolytic capacitors in parallel with ceramic types are best. Typical values might be 1μF and 0.01μF, respectively.

The strobe input to the comparator should be shielded to minimize feedthrough that might upset the measurement. It is advisable to use BNC connectors for the strobe and for the digital inputs to the converter. Both should be properly terminated (50Ω is common) at the connector end, and a grounded sleeve shield should be placed around the lead to the device pin.

Also, to ensure clean switching, the high logic-level voltage for the strobe should be the minimum acceptable. It pays to experiment with the logic level. Do not assume that the data sheet value of 2V is ideal, because some lower value may work better. In general, the smaller the strobe pulse amplitude, the smaller the feedthrough.





5. Settling time is measured from the 50% point on the edge of the digital input pulse to the 50% point of the strobe pulse's falling edge. With the waveforms shown for the d-a converter's turn-on (a) and turn-off (b), the measured settling times are 290ns and 320ns respectively. The converter's specified settling time is 400ns.

HARRIS

APPLICATION NOTE

538

MONOLITHIC SAMPLE/HOLD COMBINES SPEED AND PRECISION

BY TARLTON FLEMING

INTRODUCTION

A new Sample-Hold amplifier from Harris Semiconductor offers the best combination of speed and accuracy available in a monolithic device. It was developed for moderate to high speed applications-and particularly as an input for successive-approximation A/D converters which perform a precise conversion in 30 microseconds or less. This second-generation design includes a 100pF MOS hold capacitor, and offers a 1.0 microsecond acquisition time along with high accuracy over the commercial and military temperature ranges.

This new product, the HA-5320, can track a signal indefinitely (like an op amp) while in the sample mode. At the instant a digital HOLD command is applied the corresponding signal level is held and maintained at the output. The ratio of sample (track) to hold time is set by the user, according to the duty cycle of his digital control signal.

COMPARISON WITH EARLIER DESIGN

The HA-5320 retains the versatility of its predecessor, the popular HA-2420. That is, both have the uncommitted differential inputs of an op amp, allowing their Sample-Hold function to be combined with many conventional op amp circuits. Their circuit designs are different, though, producing significant differences in performance. These are best illustrated by describing the new device in contrast with older HA-2420. Table 1 summarizes the electrical characteristics of each, based on a 100pF hold capacitor.

Both IC's are packaged in a 14 pin DIP and operate on ±15V supplies. The hold capacitor connections differ as shown in Figure 1. Otherwise, the pinouts are compatible to this extent: Either device will operate in an existing HA-2420 socket if pin 6 is grounded, preferably to the system signal ground.

The HA-5320 delivers optimum performance when used as intended — relying on the internal 100pF hold capacitor alone. At +75°C this capacitor allows only 19μV of droop in 15μs. The Droop Rate is proportional to Drift Current, which increases with temperature (Figure 3). Droop may be reduced by adding external cpacitance C_H as shown in Figure 1B. This extra capacitance will reduce the bandwidth (Figure 5) and affect other parameters as shown in Figure 4. Also, a capacitor of value $0.1C_H$ should be added at pin 8 to reduce output noise in the Hold mode. Whether operating with additional hold capacitance or not, an HA-5320 offers a considerable improvement in accuracy over the HA-2420. Particularly welcome is the elimination of variation in "pedestal" error with input voltage. Further, the residual pedestal error may be nulled to zero, yielding great accuracy at a given temperature.

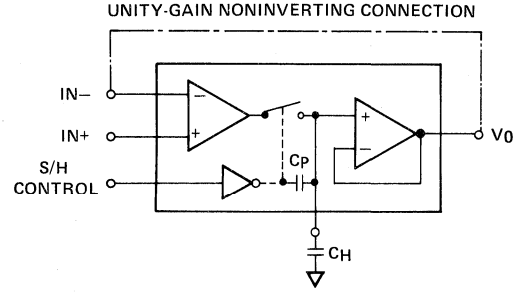


Figure 1A. HA-2420 Diagram

Test Conditions: $V_{PS} = \pm 15V$; $V_{AL} = 0.8V$ (Sample); $V_{AL} = 2.0V$ (Hold); $C_H = 100pF$

(Room Temp R = +25°C; Full Temp. F is -55°C to +125°C)

PARAMETERS	TEMP.	HA-5320 MIN	HA-5320 TYP	HA-5320 MAX	HA-2420 MIN	HA-2420 TYP	HA-2420 MAX	UNITS
Input Characteristics								
Offset Voltage	R		0.2	0.5		2		mV
	F			2.0			6	mV
Bias Current	R		70	200		40		nA
	F			200			400	nA
Offset Current	R		30	100		10		nA
	F			100			100	nA
Common Mode Range	F	±10			±10			V
CMRR	R	-80	-90		-80	-90		dB
Transfer Characteristics								
Large Signal Voltage Gain	R	1×10^6	2×10^6			50K		V/V
Feedthrough Attentuation, 100KHz	F	76	80			76		dB
Gain Bandwidth Product	R		2.0			2.8		MHz
Output Characteristics								
Voltage	F	±10			±10			V
Current	R	±10			±15			mA
Full Power Bandwidth	R		600			100		KHz
Transient Response								
Rise Time	R		100			50	75	nS
Overshoot	R		15			25	40	%
Slew Rate	R		45		5	7		V/S
Digital Input Characteristics								
Voltage High (V_{AH})	F	2.0			2.0			V
Voltage Low (V_{AL})	F			0.8			0.8	V
Current (V_{AL} = 0V)	F			-4			-800	μA
Current (V_{AH} = 5V)	F			100			20K	nA
Sample/Hold Characteristics								
Acquisition Time, to								
±0.1% FS	R		0.8			2.5		μS
±0.01% FS	R		1.0			3		μS
Aperture Time	R		25			30		ns
Effective Aperture Delay Time	R		-25			30		ns
Aperture Uncertainty	R		0.25			5		ns
Drift Current	R		8			5	50	pA
	F		1.7			0.5	4.0	nA
Pedestal Error	R		1.0			9		mV
Power Supply Characteristics								
Positive Voltage	F	14.5	15	16		15		V
Negative Voltage	F	-14.5	-15	-16		-15		V
Positive Current	R		11	13		8.5	12.5	mA
Negative Current	R		-11	-13		-8.5	-12.5	mA
PSRR	F	-65	-75		-80	-90		dB

Table 1. Electrical Characteristics HA-5320 vs. HA-2420.

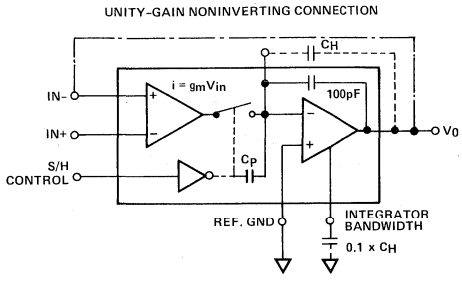


Figure 1B. HA-5320 Diagram

UNDERSTANDING PEDESTAL ERROR

When a S/H amplifier is switched from Sample to Hold, its output voltage rarely matches the ideal value one would expect from a perfect device. Instead, it differs by a small ΔV of a few millivolts, even with a DC input applied. Called "Sample to hold offset" or "pedestal", this error has a predictable polarity and magnitude for given conditions.

In general, this error is affected by magnitude of the input voltage, magnitude of the digital control level V_{AH}, rise time of the logic transition, size of the hold capacitor and temperature. Most troublesome of these is the variation of pedestal with input voltage, and this effect has been completely eliminated in the HA-5320.

Pedestal error is caused by the injection of charge onto the hold capacitor from a digital input, through small values of parasitic capacitance. Injection can come directly from the S/H control input or from the internal switch action. In Figure 1A and 1B, the capacitance of a base-collector junction in the switching circuit is represented as Cp, which varies with base-collector voltage for the transistor. That voltage is constant for the HA-5320, since Cp connects to a virtual ground. Therefore, charge injection and the resulting pedestal error are not affected by changes in V_{IN}. (For the HA-2420 in Figure 1A, Cp varies with V_{IN} and produces a varying pedestal.)

Another source of injected charge is the S/H control signal. This coupling is virtually zero within the HA-5320 chip, but a packaged unit exhibits about one millivolt change in pedestal per volt change in TTL level. However, compensation in the chip has been adjusted for zero pedestal at the nominal TTL level of 3.5V.

NULL THE PEDESTAL

This may be accomplished by introducing an equal and opposite voltage at the output, using the Offset Adjust terminals as shown in Figure 2. Since pedestal error does not change with V_{IN}, it may be treated as a simple offset. Use of the Offset Adjust shifts the pedestal error to the Sample Mode though, which may cause problems in a few applications.

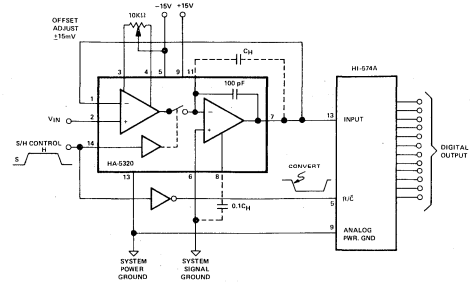
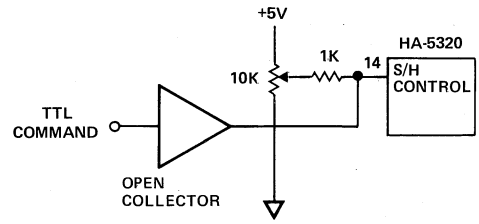


Figure 2. Signal Processing System

For these, one may make use of the relation between pedestal magnitude and the digital input level.

As mentioned earlier, the pedestal changes about one mV per volt of change in the digital "1" level, or V_{AH}. For small systems simply adjust V_{AH} until the pedestal is eliminated. In larger systems, the same adjustment may be made locally:



UNDERSTANDING DROOP ERROR

"Droop" is a change in output voltage vs. time while in the hold mode, caused by a flow of leakage current from the hold capacitor. For the HA-5320, this change is quite linear with time. The leakage current includes "off" leakage from the bipolar switch and bias current into the inverting input of the output integrator. The switch output consists of the joined collectors of two "off" transistors, NPN and PNP. These are tied to a JFET gate at the integrator input, so the hold capacitor looks at three leakage components, each of which doubles every 10°C. Ideally, these sum to zero and maintain a net zero leakage into the hold capacitor with changes in temperature. Effort has been made to achieve this. The JFET also produces less output noise than does the MOSFET used in the HA-2420.

An externally-supplied hold capacitor may provide other avenues for leakage current, but of course the HA-5320 does not require an external capacitor. Its 100pF internal hold capacitor is a guaranteed and factory-tested component. This eliminates the uncertainty associated with a user supplied com-

ponent, and also eliminates the selection, purchase, stocking, test and assembly of high quality hold capacitors.

The typical leakage (called "drift") current varies with temperature as shown in Figure 3. Then, droop error is directly related to drift current by the relation

$$V_{DROOP} = \frac{I_{DRIFT}\,\Delta t_H}{C_H}$$

where t_H is time in the hold mode. Using C_H=100pF and Δt_H = 25 μs, typical droop error may be calculated for a given temperature:

$$V_{DROOP} = \begin{array}{r} 1.25\,\mu V\ @ +\ 25^oC \\ 23.0\ \ \mu V\ @ +\ 75^oC \\ 425.0\ \ \mu V\ @ +125^oC \end{array}$$

This shows a typical droop error of less than 1/5 LSB in 12 bits at +125°C, for one of the major applications targeted for this device (input to a successive-approximation A/D converter with 25μs conversion time.)

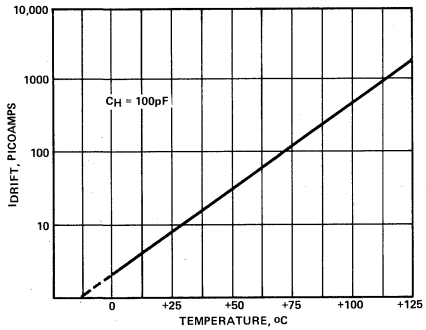


Figure 3. Hold Mode Drift Current v.s. Temperature

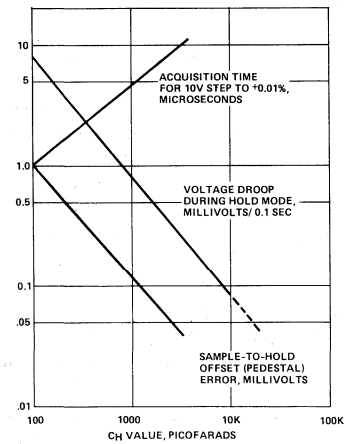


Figure 4. Typical Sample-and-Hold Performance v.s. Hold Capacitance

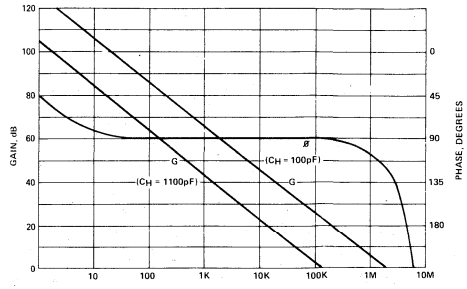


Figure 5. Open Loop Gain and Phase Response

OUTPUT CURRENT

Up to ±20mA may flow without damage, but the guaranteed limit for normal operation is ±10mA. The design does not include short circuit protection; consequently output impedance remains low with increasing frequency. This is an advantage in Figure 2, where the S/H output sees step changes in load current as a conversion proceeds. The HA-5320 is able to absorb these current changes with only a small and brief (5mV, 100nS) perturbation in its output voltage. A higher output impedance would extend this transient toward the moment of decision by the converter's comparator, producing a degradation in digital output accuracy.

With power applied, avoid a momentary short of the HA-5320 output to any fixed potential such as ground or either supply.

SIGNAL PROCESSING CONSIDERATIONS

An analog signal may be digitized by a Sample/Hold-AD converter system such as the one shown in Figure 2. If required, the analog signal may then be reconstructed from that sequence of digital samples, using a D/A converter. One might ask, how does the sample/hold alone constrain this sampling process? That is, how high a frequency can be digitized to a given level of accuracy?

The HA-5320 imposes three types of limit on the highest signal frequency applied at its input. First, the analog channel in the Sample mode has a 2MHz small signal BW, and a 600KHz Full Power BW (20 Vpp input). Next, Aperture Uncertainty Time contributes a trade-off between accuracy and frequency. Finally, Acquisition Time places a ceiling on the maximum sample rate obtainable with a given A/D converter, according to:

$$\text{MAX SR} = \frac{1}{t_{ACQ} + t_{CONV}}$$

where t_{CONV} is the A/D converter's conversion time. (Input frequency must not exceed one half the Sample rate, unless the application is tolerant of "alias" errors).

For example, the typical HA-5320 Acquisition Time for a 10V step is:

Temp	Acquisition Time, t_{ACQ} ±0.1%	±0.01%
+25°C	0.8μs	1.0μs
+125°C	0.9μs	1.1μs

Thus a 25μs converter could generate approximately $(1\mu s + 25\mu s)^{-1} = 38{,}460$ samples per second, allowing input frequencies as high as 19.23 KHz under ideal conditions (a low noise signal source with abrupt bandlimiting).

In most applications though, a low pass "antialiasing" filter is required to bandlimit the HA-5320 input. This filter controls "alias" error by reducing the amplitude of all signals and noise at and above the Nyquist frequency (SR/2). A given accuracy requirement translates to a minimum attenuation at the Nyquist frequency, which is accomplished by increasing the sample rate and/or the filter complexity (# poles). Twelve bit (±1/2 LSB) accuracy for example, calls for a 5 pole filter and sampling at 11X the highest signal frequency of interest. Using 38.46KHz for Sample Rate, this limits the input frequency to 3500Hz (SR/11). If this seems low, bear in mind that 12 bits ±1/2LSB is a tight specification.

The HA-5320's Aperture Uncertainty Time also imposes a limit on input frequency, independent of that due to filter poles and sample rate. The relation is

$$f_{max} = \frac{1}{2^{n+1}\,\pi\,t_{AU}}$$

where t_{AU} is the aperture uncertainty and f_{max} is the highest frequency that can be sampled to ±1/2 LSB accuracy at n-bit resolution. Typical t_{AU} is 270ps for the HA-5320, leading to 143.9 KHz for f_{max} at 12 bits. That makes the HA-5320 compatible with some of the fastest 12 bit converters available today. Also, since f_{max} increases for lower resolution, the frequency limit based on aliasing will be encountered first in nearly all applications.

Another parameter of concern is feedthrough. After sampling a signal and holding it, how much of that signal will couple to the output and appear superimposed on the DC level there? At 100KHz, the answer is 1mVpp at the output, due to 10Vpp at the input. At 10KHz, the feedthrough is still -80dB indicating the coupling path is resistive over this range.

At lower frequencies, the feedthrough is less (better) than this, since the HA-5320 is designed for relatively short hold periods. For example, the 3500Hz limit mentioned above for a 12 bit, 25μs converter requires 285μs to complete one cycle. The HA-5320 will see only a small fraction of this input cycle during each hold period.

OP AMP PROPERTIES

Both the HA-5320 and HA-2420 behave like op amps in the sample mode, and may be treated as such-that is, external feedback may be connected to form filters, integrators, inverting and non-inverting amplifiers with gain, etc. This versatility is in contrast to many other designs in which the inverting input is internally connected, committing the device to the noninverting unity gain configuration.

Referring to Figure 1, it may be noted that the HA-5320 is even more like an op amp that the HA-2420. Where the HA-2420 input stage is a voltage amplifier (actually an op amp by itself), the HA-5320 input stage is a transconductance amplifier, producing an output current $g_m V_{IN}$. Also, the HA-5320 output stage is an integrator, analogous to the 2nd stage of a classical op amp. The hold capacitor corresponds to the op amp's compensation capacitor, through here the analogy falters. Like the op amp though, closed loop gain-bandwidth product for the HA-5320 may be predicted from the expression g_m/C_H.

Fabrication of the HA-5320 features the Harris high frequency dielectric isolation (DI) process, with front-diffused collectors and P-channel JFET's. This approach has yielded DC input characteristics which compare well with those of premium monolithic op amps. Typical Offset Voltage is 200μV at +25°C and only 2mV at +125°. Offset Current is guaranteed less than 100nA at +125°C, or half the value of Bias Current at that temperature. Common Mode Rejection is guaranteed 80dB minimum over the ±10V range, with 90dB typical.

The HA-5320 is very stable in the noninverting unity gain connection. Typical phase margin is 60° at an open loop unity gain frequency of about 2MHz.

As mentioned earlier, the addition of external hold capacitance has a direct affect on bandwidth. For example, adding 1000pF increases C_H from 100pF to 1100pF. As a result, the 2MHz unity gain bandwidth shrinks to (100/1100) 2MHz = 182KHz. This means more time must be allowed for acquisition for a new sample, but not in the same ratio: Acquisition Time to .01% increases from 1.0μs to only 8.7μs.

Figure 6 shows the response to a 10 volt step in the sample mode. The asymmetry from rise to fall time for slew rate and overshoot is common to all units.

Figure 7 shows some Sample/Hold characteristics for a small signal (10mVpp) input. The Sample to Hold settling time is less than 200ns-higher gain and sweep speed resolve this to about 160ns. Notice

the final overshoot is less than .01% (one millivolt). This response is the same for any signal level. Also, slew rate is proportional to the magnitude of an input step, yielding a fairly constant value for slewing time, regardless of the distance slewed. This produces about one microsecond of acquisition time for any step change exceeding small signal conditions. For the small signal input of Figure 7, however, acquisition time is about 400ns (no slewing).

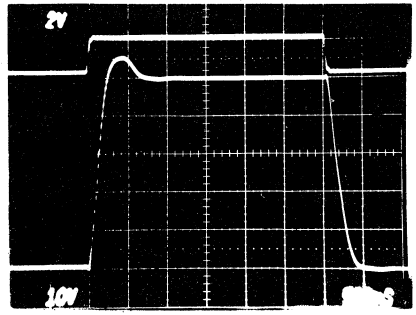


Figure 6. Step Response

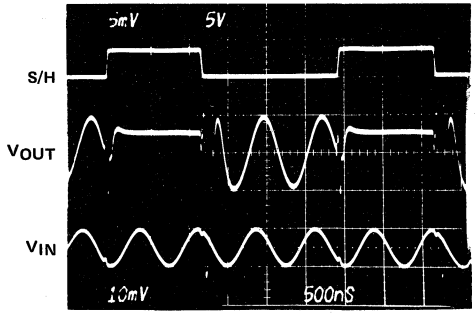


Figure 7. Small Signal Transient Response

APPLICATIONS

A/D CONVERTER INPUT

An important application has been presented in Figure 2, in which the HA-5320 serves to reduce the aperture time of an A/D converter. More directly, the Sample/Hold "freezes" an instantaneous value of V_{IN} and holds it constant during the analog to digital conversion. In Table 2, f_{max} without a Sample/Hold is relatively low, since aperture time equals the HI-5712 conversion time. Adding the HA-5320 substitues a much smaller aperture, which could allow an input frequency over 100KHz, but a lower limit is imposed by alias error effects. This limit depends on various conditions in the application, so the values listed for f_{max} (using the HA-5320) are only representative.

REQUIRED	HI-5712 CONVERSION TIME, MAX.	f_{MAX} (Vin) WITHOUT SAMPLE/HOLD	USING THE HA-5320		
			MAXIMUM SAMPLING RATE	f_{MAX} (Vin)	Min. #POLES, ANTI-ALIASING FILTER
8 BITS ±1/2LSB	7μS	88.8Hz	111KHz	24.8KHz	8
10 BITS ±1/2LSB	8.5μS	18.3Hz	95KHz	6.2KHz	3
12 BITS ±1/2LSB	10μS	3.9Hz	83KHz	1.5KHz	3

Table 2. Accuracy v.s. Maximum Input Frequency f_{max}

AUTO-ZERO CIRCUIT

A Sample/Hold may be used to form a simple but effective auto-zero loop. In Figure 8, an HA-5320 is used to maintain zero calibration for 7 channels of data.

The HI-5900 is a DAS subsystem which includes an 8 channel differential multiplexer, programmable gain amplifier and output sample/hold (the HA-2420). By dedicating channel 8 as the ground reference, a zero correction is accomplished whenever channel 8 is addressed. This must be done often enough to avoid the affects of droop error, and also following each change of PGA gain. The 10K/10Ω divider reduces the percentage effect of droop error by causing the Sample/Hold to store 1000X the actual correction value.

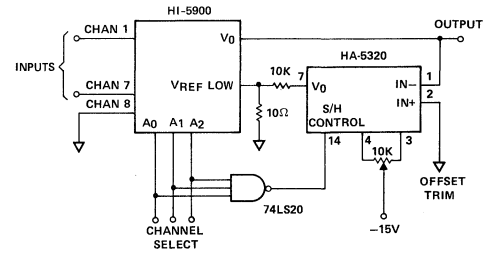


Figure 8. Auto-Zero Circuit

PEAK DETECTOR

An analog signal requires about 100ns to propagate through the HA-5320. For time varying signals, this assures a voltage difference between input and output. Also, the voltage changes polarity when the signal slope changes polarity (passes a peak). This behavior makes possible a Sample-Hold peak detector, by adding a comparator to detect the polarity changes.

In Figure 9 the exclusive NOR gate allows a reset function which forces the HA-5320 to the sample

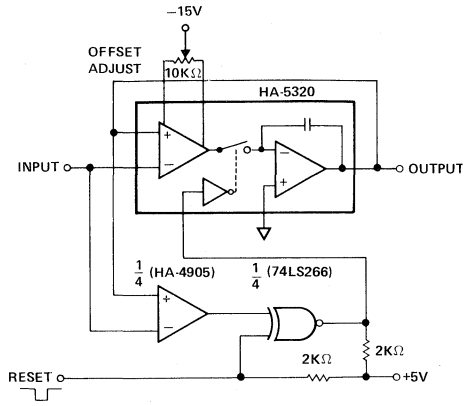


Figure 9. Positive Peak Detector

mode. The connections shown detect positive peaks; the comparator inputs may be reversed to detect negative peaks. Also, offset must be introduced to provide enough step in voltage to trip the comparator after passing a peak.

This circuit works well from below 100Hz up to the frequency at which slew rate limiting occurs. It captures the amplitude of voltage pulses, provided the pulse duration is sufficient for slewing to the top of the pulse.

The author wishes to thank design engineer Paul Hernandez and senior technician Roger O'Brien for their technical support.

HARRIS

APPLICATION NOTE 539

A MONOLITHIC 16 BIT D/A CONVERTER

BY TARLTON FLEMING

INTRODUCTION

Close attention to second order error sources has produced a 16 bit monolithic current-output DAC whose performance over temperature surpasses all similar products available at this time. The HI-DAC 16B is a dielectrically-isolated, bipolar device offering typical differential and integral nonlinearities of +1/2LSB, +3/4LSB respectively at room temperature, increasing to double those limits (maximum) at +75°C. Current mode settling time is 1μs to ±.003% FSR. It carries forward a tradition among monolithic electronic components, in performing a function both at lower cost and with smaller size than most of its predecessors.

The prospect of an emerging market for digital audio equipment is driving the development of high-resolution converters within many semiconductor companies. All are anticipating a need for D/A converters in high volume, whose technical requirements are already well established (14 bit resolution and accuracy, monotonic from 0° to 70°, 1-2μs settling time). Also, the aggressively low selling price of audio playback units dictates a monolithic IC component as the most promising solution.

HARRIS offering in this area was first announced at the 1982 International Solid State Circuits Conference in San Francisco. Called the HI-DAC16, its architecture is an extension of the earlier 12 bit HI-562, but with several significant innovations in circuit design and layout topology. The current result is solid performance at 15 bits. A sixteen bit accurate device is also under development. Since this performance exceeds the present requirements for playback of digital audio, the HI-DAC16 has targeted the markets for high resolution process control and precision instrumentation. It also promises a lower cost alternative for industrial weighing systems, automatic test equipment and high performance vector graphics, as well as digital audio. Performance is specified in Table 1 for the B and C grade units, which were introduced in March.

PARAMETER	MODEL HI-DAC16B	HI-DAC16C
Resolution	16 Bits	*
Unipolar Offset @ 25°C	±.002% FSR	*
0° -75°C	±.5ppm of FSR/°C	*
Integral Nonlinearity @ 25°C	±.0023% FSR	±.0045% FSR
0° -75°C	±.0045% FSR, Max	±.009% FSR, Max
Differential Nonlinearity	±.0015% FSR	±.003% FSR
0° - 75°C	±.003% FSR, Max	±.006% FSR, Max
Reference Input		
Voltage	10V	*
Resistance	10KΩ	*
Output		
Resistance	2.5KΩ	*
Capacitance	10pf	*
Settling Time (Full Scale Transition) Current Settling to ±.003%	1μsec	*
Noise at Output RMS ±1 0.1Hz to 5MHz	1/5 LSB	*
		*
		*
Power Supply Sensitivities		
Gain	85db or .8ppm/%	*
Differential Nonlinearity	95db or .3ppm/%	*
Power Dissipation	465mW	*

Table 1

To appreciate the challenge posed by a 16 bit converter, consider that an LSB is only 153μV, based on a 10V full scale voltage output. Similarly for current outputs, the nominal 2mA full scale sets an LSB at only 30.5 nanoamps. One must be very careful in handling these small increments of signal to avoid losing them among the offsets, noise and bias currents normally present in a system application.

For example, the analog ground connection to a conventional switched current source DAC contains code-dependent currents varying from zero to 2mA or more. Flowing through 6 inches of a typical 40 mil wide printed circuit trace, these currents produce an IR drop of 66 micro volts — nearly 1/2 LSB in a 16 bit system.

The HI-DAC16 eliminates this problem by supplying the ground current from within the chip. This allows its analog ground terminal to sense the system ground at any reasonable distance, without an IR drop.

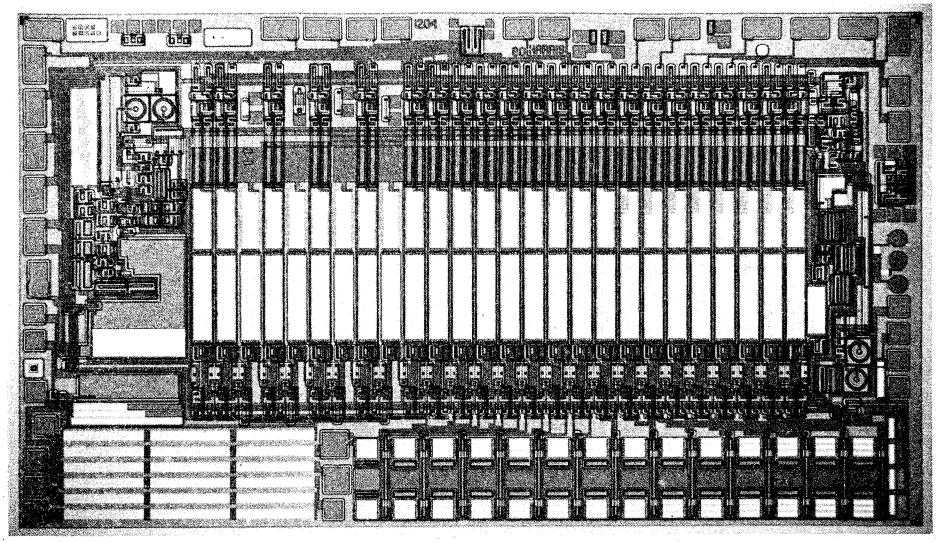


Figure 1.

Photomicrograph of the HI-DAC16. Digital-to-Analog Converter circuit combines dielectrically isolated bipolar technology with nichrome thinfilm resistors.

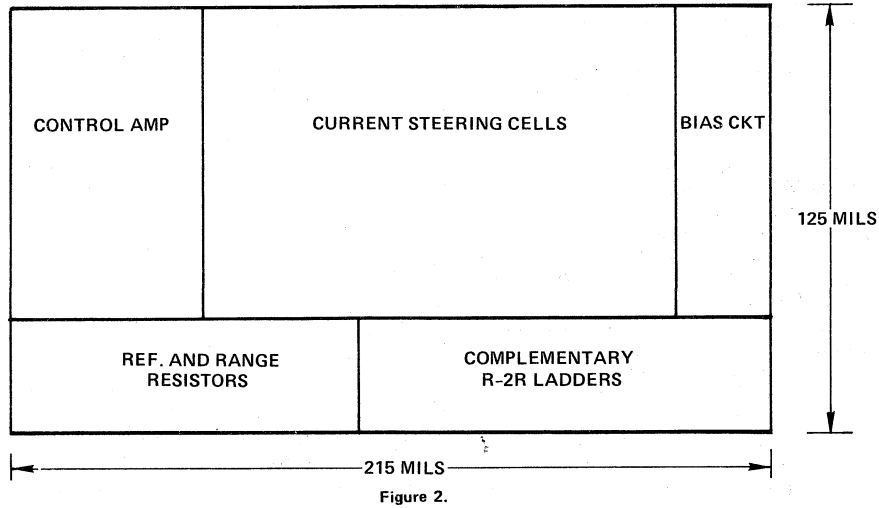


Figure 2.
Chip Diagram

BASIC FACTS

The HI-DAC16 operates on ±15V , with 456mW typical power dissipation. Package is a 40 pin side braze DIP. The 16 digital inputs accept a TTL compatible Straight Binary code word , and the nominal full scale current output is 2mA. An external +10V reference must be supplied. See Figures 1 and 2 for the chip layout and location of functions.

As shown in Figure 3, an onboard thin-film resistor provides a one-half scale offset for the bipolar ranges. Two more span resistors provide feedback around an external op amp to establish any of the standard ranges of output voltage: +5V, +10V, ±2.5V, ±5V and ±10V.

To minimize offset error due to the op amp's input bias currents, each amplifier input should see the same source resistance. An additional onboard resistor network may be connected to the amplifier's noninverting input to provide this matching for three of the five output ranges.

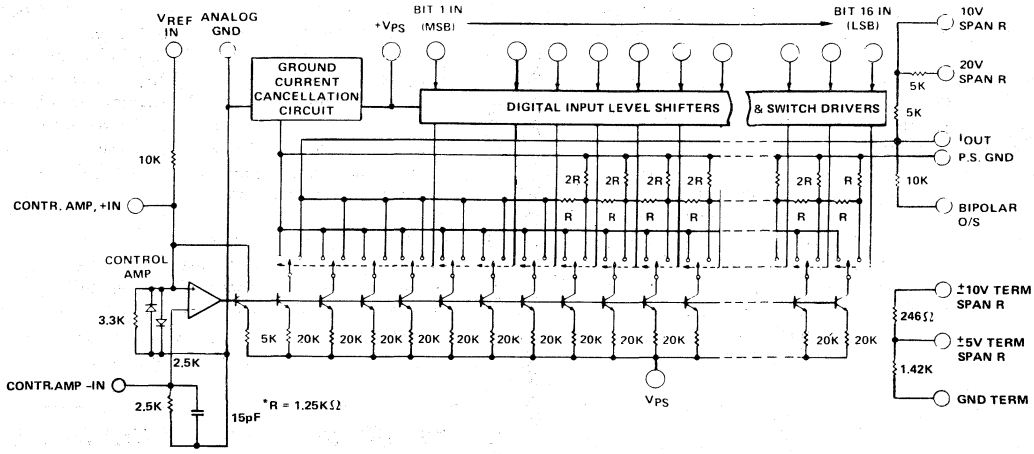


Figure 3.

Simplified Functional Diagram of the HI-DAC16. Details of the ground current cancellation circuit are in Figure 4.

A LOOK AT DESIGN DETAILS

Internal cancellation of ground current is one of the HI-DAC16's most significant improvements. It simplifies application of the device by reducing current in the analog ground terminal nearly to zero. DC offset voltage between the package and system ground is eliminated, and dynamic code-dependent current variations are contained within the chip.

Refer to Figure 4. The chip includes two identical thin film R-2R ladders, deposited with physical symmetry about a common analog ground bus. The main ladder generates output current I_O for the lower 13 bits.

The auxiliary ladder is driven by a complement of the DAC's input code, so the two ladders together draw a constant 3mA from the internal analog ground regardless of input code. (The auxiliary ladder generates a complementary current $\overline{I_O}$ which is dumped into the non-critical power ground.) The nominal three milliamps is supplied internally from the positive power supply, via a current mirror driven by a 0.5mA current source. Net current through the external analog ground is zero. Further, this null condition is maintained with variations in temperature and reference voltage, since the current source is driven by the control amplifier.

To accomplish binary weighting of the sixteen bit currents, identical current cells are employed, each with a 250μA sink and a differential transistor pair used as a two position bipolar switch. For the three MSB's, cell currents are switched either to I_O or power ground. For the remaining 13 bits, binary currents are obtained from an R-2R ladder.

Four cells are switched in tandem for the MSB; two for bit 2 and one for bit 3. In all, 20 cells mirror current from a set of four reference cells, with all 24 driven by an onboard control amplifier and the reference voltage. The resulting transfer function is:

$$I_O = \frac{V_{REF}}{4R_{REF}}\left(4B_1 + 2B_2 + B_3 + \frac{B_4}{2} + \frac{B_5}{4} + \frac{B_6}{8} + \ldots\ldots + \frac{B_{16}}{2^{13}}\right)$$

. . . . where B_1 through B_{16} are logical values for the sixteen digital inputs, ie. either "1" or "0".

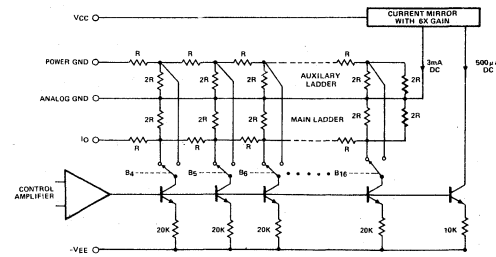


Figure 4.

Ground Current Cancellation. The auxiliary ladder adds complementary current to Analog Ground, to eliminate variations due to input code changes. The resulting DC current is then supplied internally from V_{CC}.

Several measures have been taken to counteract the linearity errors produced by any slight mismatch in cell currents or non-ideal tracking of the composite reference cell. First, the four reference calls are physically positioned among the cells of the first three MSB's in a pattern which minimizes tracking errors. Although close matching is assured by the control of process parameters and the careful matching of resistor and transistor geometries, small errors arise due to thermal gradients and IR drops in the negative supply bus. This bus is configured as a tree rather than a single wide conductor, to minimize the impact of IR drops and their change with temperature. Further, cell matching is enhanced by operation of all cells at the same current, which establishes a uniform power dissipation across the cell array.

"Superposition error" is another aberration in the transfer function of D/A converters, in which the voltage output for a given code does not exactly agree with the sum of those bits if they are turned on one at a time. Small IR drops in the ground line can cause this; as can a slight change in value of the onboard span resistor. Small changes are produced by self heating due to the flow of feedback current from the op amp. This effect is nonlinear with current and may be calibrated to zero at full scale, yielding a maximum error for outputs near 0.6 of full scale.

In the HI-DAC16, however, superposition error is hardly measureable. Ground current has been cancelled, eliminating that error component. To minimize the effect of self heating, the reference resistor is located between the two span resistors to provide a tight thermal coupling among the three. The ratio of reference to span value is only 2:1, using identical geometries, so a temperature change in either span quickly produces a similar effect in the reference resistor. However, a change in the reference produces an opposite effect on the output. The net effect is a first order cancellation of superposition error.

SETTLING TIME - A CHALLENGING MEASUREMENT

This measurement is routine at 8 bit resolution and challenging at 12 bits, but at 14 bits it pushes the limit of currently available techniques. As mentioned earlier, typical full scale settling for the HI-DAC16's current output is one microsecond (to ±0.003% of full scale which is ±1/2 LSB at 14 bits). Although the time interval is only moderately fast, it is difficult to measure the ±1/2LSB window at high resolution.

The method in use at Harris Analog Division simulates the conditions seen by a DAC when used in a successive approximation A/D converter. A strobed comparator (The HA-4950) is used to sense the DAC output with respect to a ±1/2LSB window about the final settled value. At 14 bits, the comparator operates reliably (HI-DAC16 provides 203μV for the LSB in this setup) but at higher resolution the smaller LSB doesn't provide enough overdrive. These measurements will require either a better comparator or a different test method.

For the voltage output case, the LSB is large enough at a given resolution to ease the problem. Also, the settling time is longer. If the amplifier settles in t_a, the DAC in t_d and the measured value for the combination is t_m, then $t_d = \sqrt{t_m^2 - t_a^2}$, provided the amplifier has a single pole response.

VOLTAGE OUTPUT - ANY OLD OP AMP WON'T DO

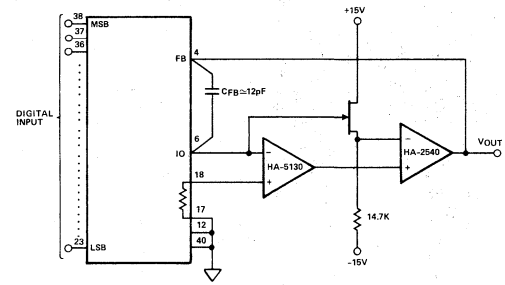


Figure 5.

Composite amplifier provides fast, accurate conversion of output current to voltage.

The HI-DAC16 imposes strenuous demands on its output current-to-voltage amplifier. Amplifier offset voltage adds error to its voltage output; input bias current adds error to the DAC output current; and finite open loop gain introduces gain error. These errors can be compensated by the calibration of offset and gain, but some error will reappear as temperature varies. A precision op amp like the HA-5130 contributes so little DC error that no calibration is required in most cases. It's not fast enough though, for high rates of update at the DAC input. HA-5130 settling time is rated 11μs, just to settle within ±0.1% (for a 10V step, slewing at 0.8V/μs).

Other op amps with different compromises in speed and accuracy may be chosen, but no single monolithic op amp can meet all these requirements:

Input Bias Current	3nA
Input Offset Voltage	15μV
Large Signal Voltage Gain	10^6
Settling Time to $\pm$0.003%	2μs
Unity Gain Stable	

However, a composite based on two monolithic op amps can offer that performance at reasonable cost. The basic connections are shown in Figure 5.

In this arrangement the HA-5130 contributes low input bias current, low offset voltage and high open loop gain, while the HA-2540 contributes high slew rate, wide bandwidth and fast settling. The JFET buffers the HA-2540's input bias current, and C_{FB} may be selected to optimize settling time.

DATA BUS INTERFACE

In general, a D/A converter is more readily connected to a digital data bus than its counterpart, the A/D converter. The interface is especially straightforward if the DAC input and data bus have the same width (in number of bits).

Figure 6 for example, shows the HI-DAC16 providing an analog output from the 16 bit data bus of an 8086 system. The DAC is updated with every coincidence of the M/$\overline{IO}$ and $\overline{WR}$ signals and a proper address. Low Power Schottky TTL latches are recommended for minimal time skew in the arrival of individual bit signals. This in turn, minimizes glitch energy in the DAC output during code changes.

Interfacing the HI-DAC16 to an 8 bit data bus simply requires the microprocessor to write two consecutive bytes to the DAC input. Unless some form of double buffering is employed, however, the DAC output will assume an unwanted intermediate state during the interval between application of the first byte and arrival of the second. This problem is eliminated in Figure 7 with a few additional ICs.

In Figure 7, the HI-DAC16 is connected to a generalized 8 bit system. The Address Decode Logic produces exclusive low states on Q_1, then on Q_2, for two consecutive addresses. These two decoded address signals are gated with "Address Valid" and "Write" from the microprocessor to produce clock inputs for the latches. As a result, the first (and least significant) byte is latched into FF1, then both bytes are fed to the DAC input simultaneously via FF2 and FF3.

The programmable interface devices available in most microprocessor component families are not "double-buffered" and so offer little advantage for interface to the HI-DAC16. The circuits of Figures 6 and 7 are more direct and less expensive. Also, digital feedthrough to the DAC's analog output can be a problem when interface circuitry is included on the DAC chip. For the HI-DAC16, external gates and latches provide a barrier to shut out this digital noise from the microprocessor.

The author wishes to thank design engineer, Tom Guy, for technical advice in support of this article.

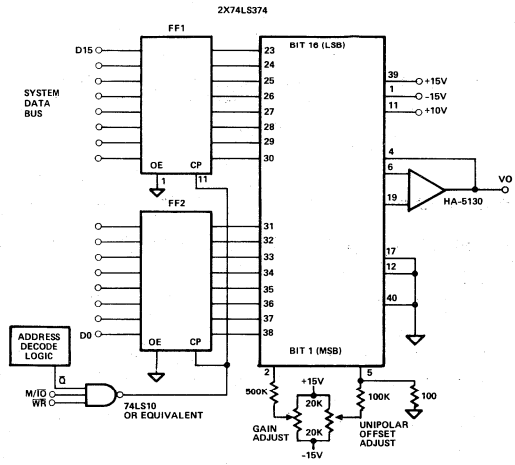


Figure 6.

Interface for a 16 bit DAC and 16 bit data bus (8086 system, minimum mode): New data is latched to the DAC input following a simultaneous low on each input to the NAND gate. The latches are strobed when $\overline{WR}$ returns high.

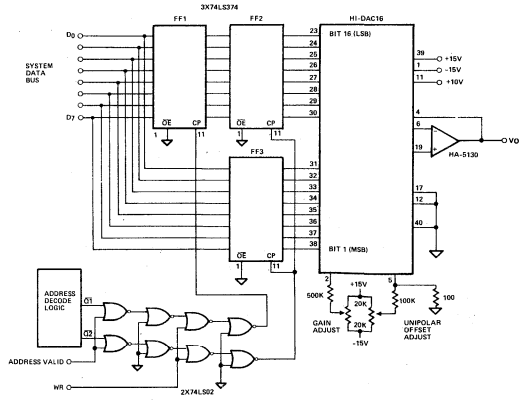


Figure 7.

An 8 bit data bus feeds a 16 bit DAC through this simple interface. The address for the least significant byte produces Q_1. Coincidence of Q_1, ADDRESS VALID and WR Clocks this first byte into FF1. Similarly, the second byte produces Q_2 which results in a strobe to FF2 and FF3, applying both bytes to the DAC input simultaneously.

HARRIS

APPLICATION NOTE 540

HA-5170 PRECISION LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER

BY J. S. PRENTICE
R. W. LEATH

INTRODUCTION

The HA-5170 is a precision, JFET input, operational amplifier which features low noise (12 μ V/$\sqrt{Hz}$ at 1KHz), low offset voltage (100 μ V), low offset voltage drift (3 μ V/^{o}C), and low bias currents (20pA). Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate, 5MHz bandwidth and fast settling times less than 1.5 μs (settling to 0.01%) make the HA-5170 well suited for fast, precision A/D OR D/A converter designs, precision sample and holds, precision integrators, or transducer signal amplifier designs.

INSIDE THE HA-5170

The Harris technology has two important advantages. First, a unique ion implant process produces JFET's with excellent matching and low 1/f noise. Second, the JFET's are in their own dielectrically isolated islands which completely eliminates the largest gate current component – the island to substrate leakage.

The HA-5170 has two voltage gain stages. The first consists of a differential JFET pair with resistor loads which develops a gain of 10. The second is a complete bipolar op amp with a gain of 30K. The absence of active loads in the first stage insures that the offset voltage, offset voltage drift and noise voltage result exclusively from the input JFET pair.

When it comes to JFET noise, bigger is better. The JFET input noise voltage, both the 1/f and white components, is inversely proportional to the square root of the gate area. Likewise, the input noise voltage due to the drain load resistors is inversely proportional to the square root of the resistance value. The JFET's "weigh in" at a whopping 110 mil^2 gate area with the resistors at 14K Ω. This results in typical noise voltages of 12nV/Hz at 1K Hz, 25nV/Hz at 10Hz and 1μV p-p over the 0.1 to 10Hz frequency band.

Trimming the offset voltage of a JFET op amp usually degrades the offset voltage temperature coefficient, so a trim scheme that simultaneously nulls both the offset voltage and offset voltage temperature drift was developed. The dominant JFET mismatches arise from mismatches in the channel height and doping profiles, not photolithography errors. It is not surprising that the V_P mismatches correlate with the I_{DSS} mismatches.

The amplifier offset voltage is given by

$$V_{OS} = \Delta V_P \left(1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right) + \frac{V_P}{2}\sqrt{\frac{I_{DS}}{I_{DSS}}}\left(\frac{\Delta I_{DSS}}{I_{DSS}} - \frac{\Delta I_{DS}}{I_{DS}}\right)$$

In this circuit, the mismatch of the drain load resistor sets the JFET drain current mismatch.

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{\Delta R}{R}$$

Thus, the offset voltage can be zeroed by trimming the load resistors. Since V_P has a large positive temperature coefficient, the offset voltage drift is normally degraded. By making the loads from composite resistors, thin film resistors in series with diffused resistors, the temperature coefficient of the $\Delta R/R$ ratio can be set to cancel both the trimming induced drift and also the JFET mismatch induce drift. This makes the HA-5170 the first JFET op amp in which trimming the offset voltage simultaneously trims the offset temperature drift. Furthermore, the offset voltage drift is reduced to even lower values when the offset voltage is nulled externally with an offset adjustment pot. The 5170 has a typical offset voltage of 100 μ V, offset drift of 3 μ V/^{o}C (without external offset nulling), and warm-up drift of only 20μV.

The excellent dc performance of the HA-5170 is complemented with dynamic ac performance never before available from precision operational amplifiers. The 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in bolth speed and bandwidth. The fast settling time of the HA-5170 (typically less than

1.5μs, settling to 0.01%) also makes it well suited for fast precision A/D and D/A converter designs.

APPLICATIONS

Several applications which utilize the design features and excellent performance of the HA-5170 are described below.

Single Op Amp Instumentation Amplifier

The HA-5170 may be used as a single op amp instrumentation amplifier because of a unique design feature which places the offset adjust terminals at the juncture of two differential gain stages. The instrumentation amplifier, as shown in Fig. 1, is very simple and provides good performance features such as low noise, low offset voltage, low offset voltage drift and high input impedance at low cost.

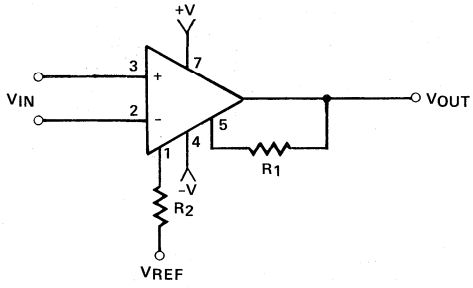


Figure 1. Single Op Amp Instrumentation Amplifier

The gain of the first differential stage is internally fixed at a gain approximately equal to 12. A feedback resistor R_1 connected between the output (Pin 6) and the balance pin (Pin 5) will close the loop around the second differential stage and set its gain. The closed loop gain of the instrumentation amplifier varies directly with the value of R_1 and is approximately

$$A_{VCL} = 12.5\ V/V/K\Omega$$

The minimum gain which can be applied is about 125 ($R_1 = R_2 = 10K\Omega$) because the current into pins 1 or 5 must be limited to 4mA.

The second resistor (R_2, which is connected between Pin 1 and a reference voltage) is used to establish a reference voltage level for the output. This reference voltage may be placed at ground potential or may be variable for use as offset adjustment. The resistor R_2 should also be matched with R_1 in order to maintain high common mode and power supply rejection ratios. Standard 1% tolerance resistors will typically provide 90dB rejection ratios.

The two inputs of the HA-5170, pins 2 and 3, may now be used as high impedance, true differential inputs with a common mode range of $-V_{supply}+3V$ to $+V_{supply}+0.1V$. If resistor values $R_1 = R_2 = 16K\Omega$ are used, for example, this circuit will provide a closed loop gain of 200 with a 3dB bandwidth of 20kHz and a THD $< 0.5\%$ ($V_{out} = 2V_{p-p}$). The gain linearity is typically better than 0.2%. However, the gain also changes about 0.2%/V with both common mode and power supply voltages. The gain T.C. is around 450ppm/°C but this can be reduced to less than 200ppm/°C just by using carbon film resistors which normally have negative T.C.'s (approximately 260ppm/°C for $16K\Omega$ resistors). Of course using resistors which have negative T.C.'s near 450ppm/°C will cancel gain T.C.'s altogether. If a variable gain is desired, a trim pot (in addition to R_1 and R_2) may be placed between the offset adjust pins. Resistors R_1 and R_2 and the maximum value of the trim pot will set the minimum gain. As the resistance of the trim pot is decreased, the gain will increase proportionally to the inverse of the trim pot resistance. This relationship of gain and trim pot resistance is shown in Fig. 2.

This circuit also maintains all to the HA-5170's excellent as and dc characteristics such as low offset voltage, low offset voltage drift, low noise, and high gain.

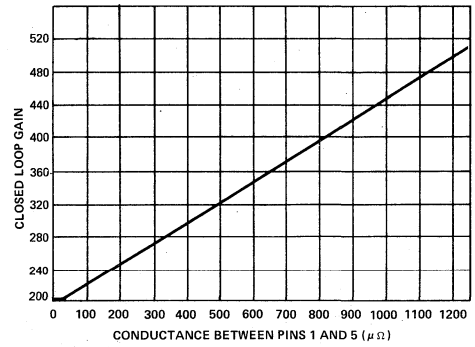


Figure 2. Closed Loop Gain Vs. Conductance Of Trimpot

SINE WAVE OSCILLATOR

The instrumentation amplifier circuit described above can be easily modified to produce a low distortion sine wave oscillator with voltage controlled amplitude as shown in Fig. 3. The small changes in gain of the instrumentation amplifier that occur with changes in common mode voltage has been exploited here to provide oscillator amplitude control with a voltage source. Another unique feature of this circuit is that is does not require any of the nonlinear components that most other sine wave oscillators require.

The phase lead network, which consist of R_3, R_4, and C_1, cancel the phase lag through the amplifier and oscillation occurs at the frequency where the product of amplifier gain and voltage feedback ex-

actly equals one. The amplifier gain is expressed as

$$A_V = \frac{A}{(1 + j\omega/\omega_o)}$$

where A is the dc gain (about 125 for $R_1 = R_2 = 10k\Omega$), ω_o is the bandwidth (about 200K rad/s) and ω is the frequency of oscillation. The voltage feedback is expressed as

$$\frac{j\omega C_1 R_4}{[1 + j\omega C_1 (R_3 + R_4)]}$$

For their product to be equal to one, both of the following must be true:

$$\omega = \frac{\omega_o}{[C_1 (R_3 + R_4)]}$$

$$AC_1R_4 = C_1 (R_3 + R_4) + \frac{1}{\omega_o}$$

The oscillation amplitude is stabilized at the point where the loop gain is equal to one by the small gain nonlinearity of the instrumentation amplifier.

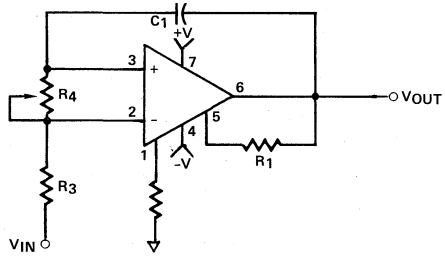


Figure 3. Sine Wave Oscillator With Voltage Controlled Amplititude

This operating point and initial amplitude is set by the resistor divider network of R_3 and trim pot R_4 ($R_4 \ll R_3$). The amplitude can then be varied by applying a common mode voltage (V_{IN}) through R_3. Positive common mode voltages increase amplitude by decreasing gain non-linearity while negative common mode voltages decrease amplitude. A typical curve of amplitude versus common mode voltage is shown in Figure 4. The gain non-linearity of the instrumentation amplifier is small, however, and distortion less than 0.5% can be obtained over a 100Hz to 100kHz range.

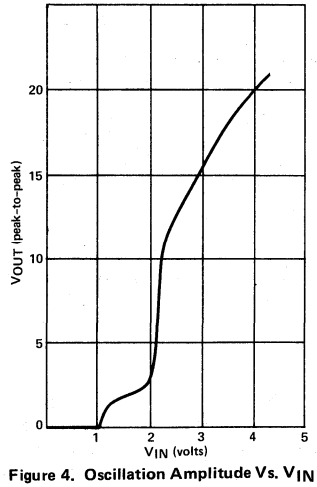


Figure 4. Oscillation Amplitude Vs. V_{IN}

Frequencies down to 10Hz can be achieved by lowering ω_o with a capacitor in parallel with R_1.

HIGH IMPEDANCE TRANSDUCERS

The HA-5170 is well suited as a preamplifier for high impedance transducers, such as photo diodes and hydrophones, because of its high input impedance and low current noise. Fig. 5 shows a photo diode preamplifier circuit whose output voltage is approximately the photo diode current times the value of R_1. When no light is present, the output of the HA-5170 is

$$V_O = I_{ND} R_1 + I_N R_1 + V_{NR} + V_N$$

where I_{ND} = Shot noise of diode
I_N = Noise current of Op Amp
V_{NR} = Noise voltage of resistor
V_N = Noise voltage of Op Amp

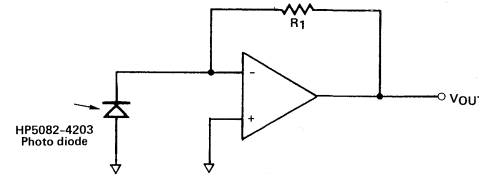


Figure 5. Photodiode Preamplifier

The signal to noise ratio is maximized when the rms sum of op amp and resistor noise current sources is equal to or lower than the noise current of the photo diode. Noise voltage sources are converted to noise current sources by dividing by R_1. The noise current of the photo diode may be approximated by the shot noise formula $2qI_d$, where I_d is the dark current, and is in the range of 10^{-13} to 10^{-14} A/$\sqrt{Hz}$, depending upon the choice of photo diodes. The rms sum of the three sources is approximately 4×10^{-14} A/$\sqrt{Hz}$ at 1kHz, assuming $R_1 = 20M\Omega$. This rms summation is approximately the same magnitude as the noise current of the photo diode with the dominant noise source being the resistor noise (about 2.9×10^{-14} A/$\sqrt{Hz}$). If a bipolar op amp were used instead of the HA-5170, the noise current (typ. 4×10^{-13} A/$\sqrt{Hz}$) would be much higher than the noise current of the photo diode. The response time of the photo diode can be improved by applying 5 to 20 volts of reverse bias but the increased speed is achieved at the expense of higher shot noise.

A resistor equal to the feedback resistor could be inserted between the non-inverting input and ground to reduce offset voltage. This is usually not necessary since the output offset voltage would only be 600μV for a 20MΩ resistor.

Fig. 6 shows a hydrophone preamplifier with a 100Hz to 100kHz bandwith and a gain of 100. Since hydrophone impedance is capacitive, it should be bypassed with a large bleeder resistor to shunt the bias currents to ground.

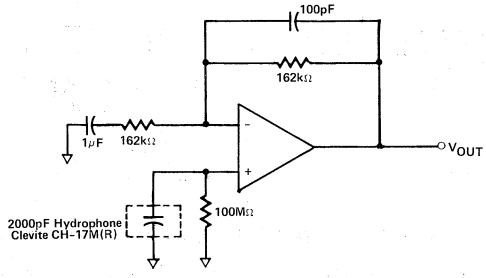


Figure 6. Hydrophone Preamplifier

CURRENT SOURCE/SINK AND CURRENT SENSE CIRCUITS

The HA-5170 can be used as a well regulated, two terminal, constant current source or sink, as shown in Fig. 7, or as a current sense amplifier, as shown in Fig. 8. These circuits take advantage of FET inputs' capability to accept a common mode voltage up to 0.1V above the positive supply.

The current from the constant current source consists of amplifier supply current and load current through R_2, both of which pass through the sense resistor R_1. The amplifier output will sink just enough current to cause the IR drop across R_1 to equal the amplifier offset voltage. This offset voltage may be adjusted by the trim pot R_3 and typically has a minimum adjustment range of 6mV. Smaller offset voltages give better power supply rejection ratios and usually give better results. The amplifier supply current, typ. 1.8mA, sets the minimum constant current while the amplifier short circuit protection limits the maximum to 15mA. Current regulation better than 0.08%/V and temperature variations better than 0.08%/°C can be achieved with this design.

Two operating constraints should be observed for best results. The resistor R_1 should be selected so that the amplifier output voltage remains at least 1.3V from either supply pin and the total voltage across pins 4 and 7 should be at least 12V but not over 40V.

The HA-5170 may also be used as a simple current sense amplifier in power supply applications. In this circuit, the power supply current develops a small voltage drop across the sense resisitor (R_S in Fig. 8) and the ammeter will display a current which is equal to $I_s \times \frac{R_s}{R_1}$. Of course the HA-5170 could also be placed in an open loop (comparator) configuration in which case the output would "trip" when the IR drop across R_s exceeds the offset voltage. This "trip" point can be controlled by an offset adjust trim pot connected as shown. The low noise, low offset voltage, and low bias current characteristics of the HA-5170 provide accurate measurement of supply current with very few components and can operate over a supply range of 7 to 40V.

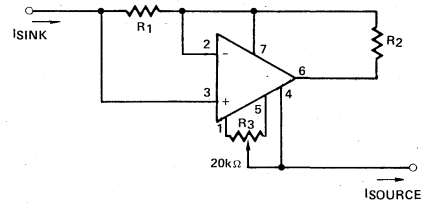


Figure 7. Two Terminal Constant Current Source/Sink

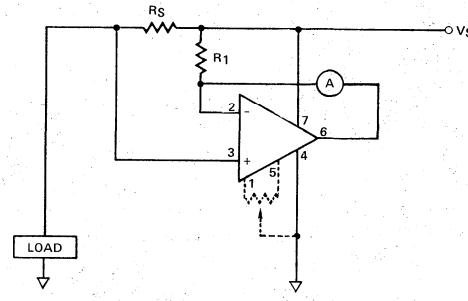


Figure 8. Current Sense Amplifier

HARRIS

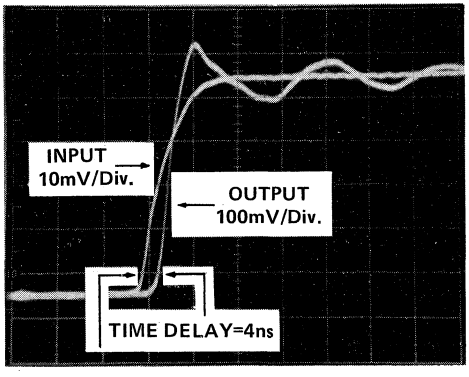
APPLICATION NOTE 541

USING HA-2539 VERY HIGH SLEW RATE WIDEBAND OPERATIONAL AMPLIFIERS

BY RICHARD WHITEHEAD

INTRODUCTION

With the superior dyamic performance available from HA-2539, a wide variety of applications can be "idealized". From high fidelity audio to television broadcast and receiving equipment these operational amplifiers can be used to provide increased system capabilities. Employing the Harris high frequency dielectric isolation process these true differential input devices offer 600V/μs slew rate coupled with 600MHz gain bandwidth product. These parameters in conjunction with an excellent time delay of 4ns (see photo), standardize HA-2539 in critical wideband video and RF applications.



HA-2539 Transient Response Waveforms

PROTOTYPING WITH HA-2539

Being a "true" operational amplifier, HA-2539 may be "designed in" using conventional high frequency amplifier techniques. Quality I.C. sockets may be used, but for maximized dynamic performance it is suggested these devices be mounted through a ground plane. External components should have minimal lead lengths and perferably connected directly to the device pins. Metal film or metal oxide resistors are recommended for feedback components. If direct connection is not possible, Teflon insulated standoffs should be used with locations as close as possible to device pins.

Power supply decoupling with .001μF ceramic capacitors from the device supply pins to ground is essential. Alternatively, filter connectors such as Erie 1201-052 are suggested for optimum decoupling.

HA-2539 may be used without heat sinks up to +75°C ambient. Power derating above this temperature is 8.7mW/°C and heat sinking is recommended. Thermalloy model 6007 or Unitrack CPU 1017 heat sinks are suggested for temperatures up to +125°C ambient.

GENERAL OPERATING CONSIDERATIONS

Dynamic performance of HA-2539 was maximized through the exclusion of output short circuit protection and internal offset voltage adjustment circuitry.

Although these amplifiers can withstand momentary short circuits to ground, it is recommended that some output current limiting network be used, if the operating environment is hostile. Figure 1 shows a suggested method for output terminal protection.

Offset voltage adjustment may be accomplished by the suggested methods shown in Figure 2 (a) and (b).

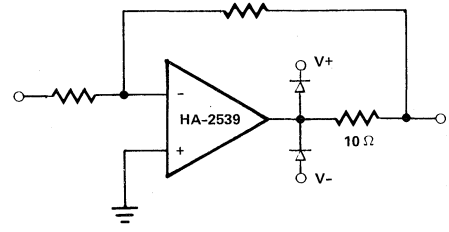
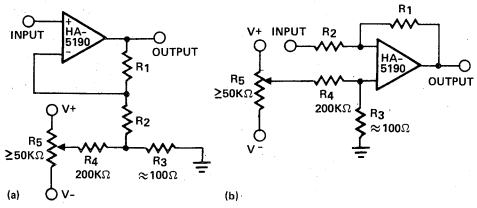


Figure 1. OUTPUT PROTECTION FROM FAULT CONDITIONS



RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

Figure 2. OFFSET NULLING

As with many wideband, high speed devices, recovery from output saturation can be in the order of microseconds. HA-2539's saturation recovery from its positive rail is of the classical variety where voltage charges on the "body" capacitances of output devices must discharge before normal operation can be resumed. Recovery from the negative rail is similar to the positive rail recovery except during saturation small signal oscillation may occur. This oscillation is due mainly to a regenerative signal coupled back to the input during saturation.

GENERAL APPLICATIONS

FREQUENCY COMPENSATION

HA-2539 is stable in standard operational amplifier circuits with closed loop gains exceeding +10 or -9. Keeping the network resistor values as low as practical in these configurations should optimize the dynamic performance.

Circuit configurations shown in Figure 3 may be used to stabilize HA-2539 at closed loop gains less than specified. Figure 3 (a) employs capacitance to over damp HA-2539's response. Stable operation to gains of 5 are practical. Figure 3 (b) utilizes the amplifier's differential input impedance to reduce input and feedback signals thereby raising noise gain to a stable point on the response curve. Gains of -3 are practical.

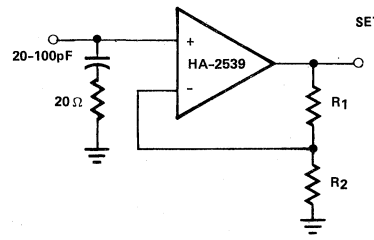


Figure 3. a. COMPENSATION BY OVERDAMPING

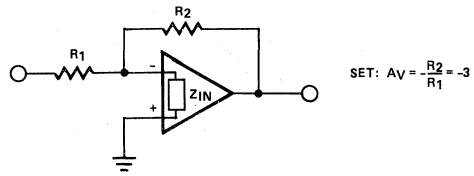


Figure 3. b. STABILIZATION USING Z_{IN}

REDUCING DC ERRORS

A composite amplifier scheme may be used to reduce errors due to offset voltage and bias current. Figure 4 shows HA-2539 and HA-5170 in a composite configuration which greatly reduces DC errors without compromising the high speed, wideband characteristics of HA-2539.

The HA-2539 amplifies signals above 40KHz which are fed forward via C_2 and R_2. Resistors R_4 and R_5 set the voltage gain at -10. The slew rate of this circuit was measured at 350V/μs. Settling time to a 0.1% level for a 10V output step is under 150ns and the gain bandwidth product is 300MHz.

The HA-5170 amplifies signals below 40KHz, as set by C_1 and R_1, and controls the dc input characteristics such as offset voltage, drift, and bias currents of the composite amplifier. Therefore, it has an offset voltage of 100 μV, drift of 2 μV/°C and bias currents in the 20pA range. The offset voltage may be externally nulled by connecting a 20k pot to pins 1 and 5 with the wiper tied to the negative supply. The dc gains of the HA-5170 and HA-2539 are cascaded which means that the dc gain of the composite amplifier is well over 160dB.

The excellent AC and DC performance of this composite amplifier is complemented by its low noise performance, 0.5 μV rms from 0.1Hz 100Hz, and makes it very useful in high speed data acquisition systems.

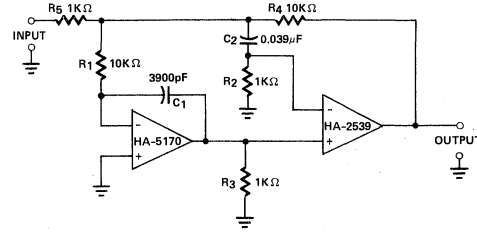
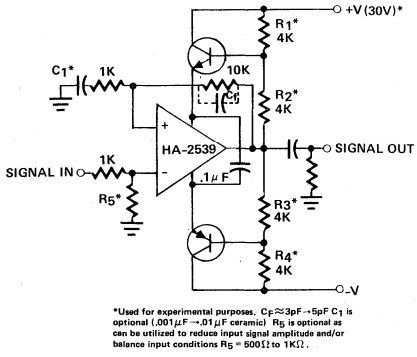


Figure 4. COMPOSITE AMPLIFIER

BOOSTING OUTPUT CURRENT AND INCREASING OUTPUT SIGNAL SWING

Figure 5 shows a cost effective method for increasing output voltage swing or boosting power of HA-2539 while adapting the device to supply rails which exceed the absolute maximum ratings. The supply rail values are limited only by the breakdown voltages of the transistors used, provided R_1 through R_4, are set to limit the voltage at the device supply pins to nominal supply values (±15V). Transistor selection should be limited to high f_T (greater than 60MHz) types such as MPS-A06 and MPS-A56.

Physical layout properties may necessitate the use of phase lead compensation, in which case C_F may be added. It has unmeasurable distortion and very low noise within the audio band.



*Used for experimental purposes. $C_F \approx 3pF \rightarrow 5pF$ C_1 is optional (.001μF →.01μF ceramic) R_5 is optional as can be utilized to reduce input signal amplitude and/or balance input conditions $R_5 = 500\Omega$ to $1K\Omega$.

Figure 5. BOOTSTRAPPING FOR MORE OUTPUT POWER AND VOLTAGE SWING

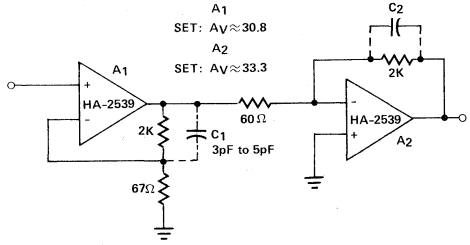
APPLICATIONS

INTRODUCTION

HA-2539 may be utilized in a wide variety of applications ranging from active filters to video pulse amplification. However, the applications to follow were selected to show where this can be used most advantageously.

APPLICATION 1 CASCADED AMPLIFIER

Cascaded amplifier sections are used to extend bandwidth and increase gain. Using two HA-2539 devices, this circuit is capable of 60db gain at 60MHz.



APPLICATION 1 CASCADED AMPLIFIER SECTION

APPLICATION 2 VIDEO GAIN BLOCK

Video drivers and gain blocks used in color video systems are most always required to have outstanding differential phase and differential gain specifications. These requirements historically have eliminated the use of operational amplifiers and favor large discrete amplifiers which can be tailored to minimize system errors.

This configuration utilizes the wide bandwidth and speed of HA-2539 plus the output drive capability of HA-2630. Stabilization circuitry is avoided by operating HA-2539 at a closed loop gain of 10 while maintaining an overall block gain of unity. However, gain of the block may be varied using the equation:

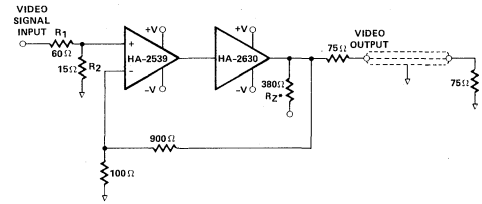
$$\frac{V_{OUT}}{V_{IN}} = 5 \quad \frac{R_2}{(R_1+R_2)}$$

where $R_1 + R_2 = 75$ ohms

A maximum block gain of 3 is recommended to prevent signal distortion.

The output stage of HA-2630 is biased to a higher current level through resistor R_Z. Maintaining this biased "on" condition reduces signal distortion and virtually eliminates errors due to differential phase by decreasing the percent change in the output stage operating point.

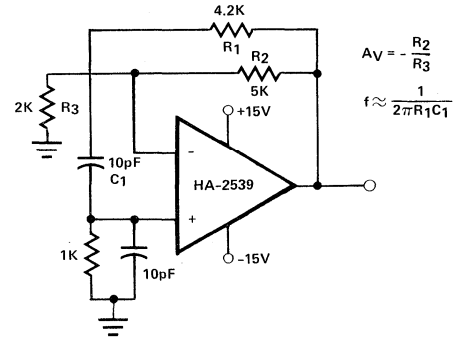
The circuit in Figure 1 was tested for differential phase and differential gain using a Tektronix 520A vector scope and a Tektronix 146 video signal generator. Both differential phase and differential gain were too small to be measured.



APPLICATION 2 VIDEO GAIN BLOCK

APPLICATION 3 HIGH FREQUENCY OSCILLATOR

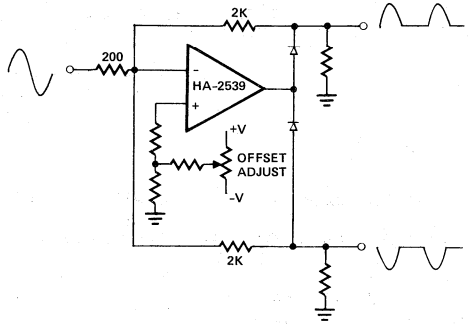
Intended primarily as a building block for a QRP transmitter, this 20MHz oscillator delivered a "clean" 6Vp-p signal into a 100 ohm load.



APPLICATION 3 20MHz OSCILLATOR

APPLICATION 4 WIDEBAND SIGNAL SPLITTER

With one HA-2539 and two low capacitance switching diodes, signals exceeding 10MHz can be seperated This circuit is most useful for full wave rectification, AM detectors or sync generation.



APPLICATION 4 WIDEBAND SIGNAL SPLITTER

ACKNOWLEDGEMENTS

A. Terry D. Hass of Solitron, Inc., Stuart, Fl. developed and tested video gain block.

B. Ron Jasinski of Sound Studio Services, 3208 Cahuenga Blvd. West, Los Angeles, CA. 90068 Developed and tested bootstrapped output scheme.

C. Russ W. Leath of Harris Semiconductor developed and tested composite amplifier circuit.

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Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier May 1979.

Tobey, Braeme, and Huelsman. Operational Amplifiers Design and Applications. New York: McGraw-Hill Book Company, 1971.

HARRIS

APPLICATION NOTE 542

USING THE HV-1000 INDUCTION MOTOR ENERGY SAVER

BY: P.W. SHACKLE
R.S. POSPISIL

WHAT'S IN A NAME?

The HV-1000 is an integrated circuit intended to reduce onto one chip, most of the circuitry of the single phase, induction motor, energy saver circuits first described by Frank Nola of the NASA Marshall Space Flight Center in U.S. Pat. 4052648. The original name given to such motor controller circuits was "power factor controller", or more precisely "power factor sensing controller". The origin of this name lay in the fact that induction motors draw almost a constant current regardless of load, as long as the motor is turning. The motor responds to loading by producing a more resistive power factor, thus drawing more power from the line. The load on the motor can be sensed by measuring the power factor, and so this can be used as the basis of a control algorithm. The original controllers adjusted the firing time of a TRIAC in series with the motor in such a way that the time delay between the voltage zero crossing and the current zero crossing was reduced and held constant. To the extent that this time interval represents the power factor for a non-sinusoidal waveform, the power factor was indeed being improved and kept constant. However, if one adopts the utility company definition of power factor as

$$\frac{\text{Watts}}{\text{Volt Amperes}}$$

then, because both the Amperes and the Watts are reduced roughly proportionately, the power factor, by this definition, is almost unchanged. To avoid confusion, Harris has chosen not to refer to power factor control, using instead the acronym "IMES" (Induction Motor Energy Saver).

APPLICATIONS

Generalities on when to use an IMES:

The induction motor energy saver performs its function by taking advantage of the fact that an AC induction motor runs at almost a constant speed regardless of the voltage applied, its speed being determined by the frequency of the AC supply. When the motor is lightly loaded the voltage applied to the motor can be reduced so that it consumes less current and power, as long as a sufficient voltage remains to drive whatever load is present. All that the IMES does is to sense the load on the motor (through the power factor), and then turn down the voltage by a predetermined amount. To a first approximation, the usefulness of applying an IMES in a given situation can be gauged by driving the motor with a variable transformer and using a power meter to measure the power consumed. If there are circumstances where reducing the voltage reduces the power consumed, then probably the IMES can save some energy. Remember when you do this that the IMES can turn the voltage up and down much faster than you can to follow rapid variations in loading.

Some obvious circumstances where a motor is very lightly loaded part of the time include a radial arm saw (or any saw), a bench grinder or a drill press. In each case it is easy to see that until the machine is actually cutting something, little work is being done and usually the power consumed can be reduced by having the IMES reduce the voltage in between the actual work periods. Less obvious circumstances are the commercial washing machine and the office typewriter. The key to these applications is that in each case, the motors in question must be capable of briefly delivering very high torque, so that for much of the rest of the time, the motor is relatively lightly loaded. The would-be energy saver engineer must keep firmly in mind the fact that for energy savings to be possible, the motor must be relatively lightly loaded compared to its real capability. To make the point more strongly, if you reduce the voltage applied to a one horsepower motor when it is driving a one horsepower load, most likely it will use more power, not less. For example, many of the pump designs used for irrigation sprinklers, pool pumps and well pumps are relatively inefficient hydraulically and load their motors to about the same degree regardless of the volume of water being pumped. Furthermore, the motor supplied is likely to be very well matched to this nearly constant load so that any attempt to reduce the voltage with an IMES will cause more, not less power to be used.

Sometimes the manufacturer of say, a belt sander or a sump pump will have designed the equipment with the idea in mind that the usage will only be very intermittent. In this case, when the motor is actually working, it might be outputting twice its rated power. If this condition were prolonged, the motor might be burned out very rapidly. Clearly no power savings are to be had when the machine is loaded. In the case of the sump pump, no savings are to be had at all since the motor is off when it is not pumping. In the case of belt sanders, the authors have once seen a belt sander in which the motor was running almost at full load when the machine was not doing any work at all. Again, no energy savings are possible in these circumstances by reducing the voltage. This should not be taken as an implication that the IMES cannot be used on any belt sander – merely that some such machines can have much under-powered motors.

One application that is less obvious is the reverse cycle air conditioner or heat pump. It frequently happens that the motor in these machines is much less heavily loaded during the heating cycle than it is during the cooling cycle. In this case, application of the IMES can result in useful energy savings. An industrial clutched compressor, where the motor runs continuously and the compressor is clutched in intermittently, is another useful application.

Three specific tests to identify an IMES application:

From the foregoing discussion and examples, we can now proceed to develop a set of test criteria which allow the identification of good applications for the IMES. The first question is – is the motor in question a single phase induction motor? Vacuum cleaners and portable drills, for instance, frequently have so called universal motors, a totally different kind of motor to which the IMES is not applicable. The IMES principle can be applied to big industrial three phase motors, but such controllers are typically complex and expensive systems. The prime candidates for application are single phase, 120 or 240V induction motors of more than ¼ HP. The HV-1000 can be applied to capacitor-start motors and to capacitor-start, capacitor-run or two value capacitor motors. It would not normally be useful to apply it to a permanent split capacitor motor, since these are usually applied to equipment with steady, non varying loads.

The second question is – does the motor in question experience strongly varying loads, with a large part of the time being lightly loaded? For instance, most ventilation fans have very steady loads and could not be expected to show any power savings. On the other hand, industrial sewing machines have such strongly varying loads that large flywheels are often incorporated to try and smooth the variations. These are an excellent area of application for the IMES.

The third question to be asked is whether the motor operates a sufficient number of hours per year, for the power savings that result, to pay for the cost of the IMES over the lifetime of the equipment, or in the case of an after-market add on, over the desired financial payback period. Sometimes surprising results are obtained – for instance, consider a typewriter which uses 60W when plugged in. If it runs eight hours a day, five days a week for a year, the motor is switched on for 2080 hours per year. With the IMES attached, the power consumed may go down to only 30W, a savings of 30W or 62.4 kilowatt hours per year. In an area such as New York City, where electricity costs about $.10 per KW hour at time of writing, the savings are $6.24 per year or $18.72 over a three year payback period. This number is surprisingly large considering the low power consumption of the typewriter, but the result is inflated by the 50% savings which are possible. In the case of say, a domestic washing machine, energy savings of 60 W-hours are possible over a complete cycle. So that with ten cycles per week, the potential savings are 31.2 KW hours per year. At an average power cost of $.07 per KW hour, the savings are $2.18 per year or $13.10 over a six year lifetime. In a launderette context where 100 cycles per week are possible, the savings would be $21.84 per year. A profile of a typical application of an IMES might be a light industrial carpentry shop where a circular saw operated by a ¾ HP motor was operated for six hours per day. For 50% of the time, the saw is spinning idly as the planks are loaded in to be cut or cleared away. When idling, the motor normally draws 200W -- this is reduced to 100W by the IMES. Thus the savings are .1KW x 6 x 50% x 260 days = 78 KW hours per year. At an average price of $.07 per KW hour, the payback is $5.46 per year of $27.30 over a five year lifetime for the machine. Finally, in computing savings, the hard to quantify fact should not be forgotten that most motors run quieter and cooler with an IMES.

PRECISELY, WHAT DOES THE HV-1000 IMES DO AND WHY DOES IT HAVE TO BE THAT WAY?

In this section we describe the functional capabilities of the HV-1000 and their significance for the user.

The characteristics of a TRIAC controlled motor:

The earliest IMES circuits simply placed a TRIAC in series with the motor and gated the TRIAC on at such a point in each half cycle, that the time delay between the current zero crossing and the voltage zero crossing was kept constant (Figure 1). The trouble with this method of control is that in order for the motor to respond in a stable fashion, the phase sense signal had to be averaged over many cycles otherwise the slightest jerk, vibration, or electrical noise would produce an undesirable large response from the motor. This then gave another problem – that a genuinely fast changing load was not catered to – e.g. when feeding the wood into a circular saw, the motor would stall before the controller turned the voltage up in response to the load. For this reason, it is necessary for an IMES to have a

load anticipator or panic button. When a rapid increase in load is sensed, the HV-1000 IMES instantaneously produces full voltage, preventing a stall.

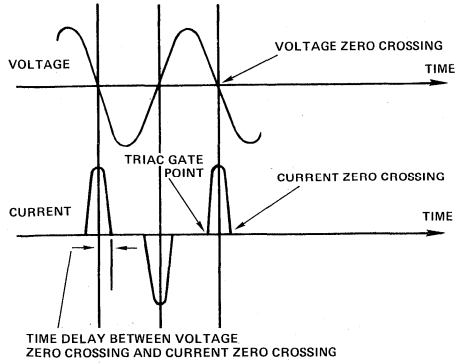

Figure 1.

In determining the best characteristics for an IMES, it is clearly necessary that when the motor is fully loaded, the TRIAC should be fired at the current zero crossing. In other words, the TRIAC should be on continuously, so that full voltage is applied to the motor. This also defines the desired point in the cycle for the current zero crossing. The diagram at the top of Figure 2 illustrates the voltage waveform as a function of time across the terminals of a TRIAC controlled motor. θ_c is the current zero crossing and θ_t is the TRIAC trigger point. At full load these should coincide. If a motor is controlled in such a way that θ_c is kept constant, then as the state of the motor is moved from full load to no load, θ_t will be observed to gradually move to the right, resulting in a throttling back of the voltage applied to the motor. At no load, θ_t will have been delayed by the maximum amount consistent with maintaining θ_c constant. If, by virtue of forced control of the system, θ_t is now moved even further to the right, θ_c will move to the left, but most motors will keep running. In other words, this experiment demonstrates that simply maintaining θ_c constant is not the optimum algorithm for getting the best savings — more power savings can be obtained by an algorithm which moves θ_c to the left by a few hundred microseconds as the load on the motor decreases.

To quantitatively represent this more optimum algorithm, the graphical presentation in the lower half of Figure 2 is helpful. θ_c is plotted against θ_t, and the resulting plots can be used to characterize both the motor and the controller. To characterize the motor, consider first the circumstance where full voltage is applied to the motor. In this case, $\theta_c = \theta_t$ and the full voltage condition may be represented by the line AC along all points of which $\theta_c = \theta_t$. The operating point will move up and down AC as the motor load is varied. Now, suppose that for a given value of θ_t, the load on the motor is increased, decreasing θ_c, until the motor stalls. Recording the value of θ_c at which this happens produces the line DB, the locus of θ_c values at which the motor stalls. It is apparent that for a given point on AC, i.e. a given load, θ_t can be increased (the motor throttled back) at constant load. θ_c will decrease in response, and the operating point of the motor will trace out a line, such as CB, until the motor finally stalls. In this way, the family of curves CB, AD, etc. is traced out. These curves represent the characteristics of a TRIAC controlled motor.

The HV-1000 algorithm:

In the experiment described above, θ_c was kept constant starting from point A, the fully loaded motor with full voltage. It can now be seen that the classic "constant power factor" type of controller has a characteristic which is a horizontal line of constant θ_c across to the no load characteristic from point A. Clearly point B, the condition where the motor is throttled back as much as possible, will never be achieved unless the controller has a characteristic which allows θ_c to vary with θ_t. The HV-1000 IMES is programmed with such a characteristic, shown by the controller line of Figure 2. The HV-1000 IMES does not keep θ_c constant, but instead allows it to vary in such a way that the voltage is throttled back as much as possible for lightly loaded motors. The curves of Figure 2 were plotted for a General Electric ⅓ HP general purpose motor. Different families of curves will be obtained for other motors. The controller line corresponds to the HV-1000 without an external potentiometer (pins 4, 5, 6 shorted together).

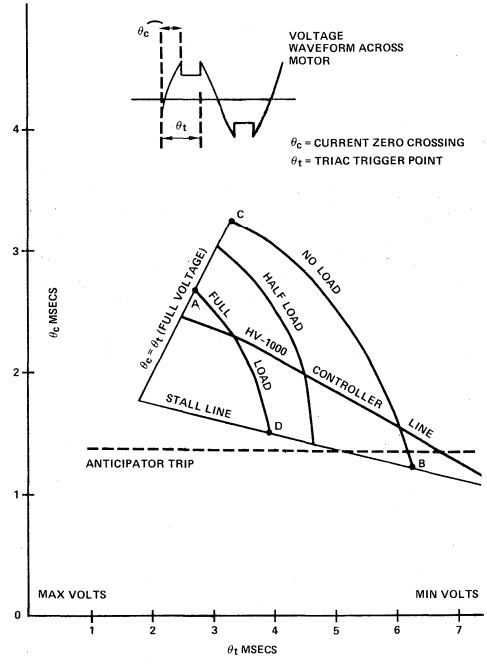

Figure 2.

The load anticipator:

Figure 2 illustrates several interesting properties of the HV-1000/motor combination. Note that the controller line does not hit the full voltage line until

above full load; in other words, the voltage is still throttled back slightly even at full load. For this particular motor this produces close to optimum power savings. For a small number of motors the controller line may have to be moved up or down (see next section) with an external potentiometer to get optimum power savings. When the HV-1000 is fitted with a relatively small (e.g. 0.10 microfarad) time constant capacitor, the operating point of the motor will be observed to stay usually within 100 microseconds of the controller line. However, with a relatively large (5 microfarad) time constant capacitor the response time of the system will be several seconds. In this case when a sudden shock load is applied, θ_t will at first stay constant, and the operating point will drop vertically downwards as θ_c diminishes. Because of angular momentum stored in the rotor and pulleys, the operating point may actually drop a few hundred microseconds below the stall line before the motor stops. As mentioned above, the HV-1000 has built into it a load anticipator designed expressly to prevent such a stall. Its operation can be represented by the "anticipator trip" line shown in Figure 2. Whenever θ_c drops below this line, the HV-1000 connects an "on" SCR and a resistor across the time constant capacitor and discharges it, after at most a hundred milliseconds, depending on the size of the capacitor. The HV-1000 thus is forced to produce full output voltage almost instantaneously. It will be observed, that since the controller characteristic slopes, the anticipator trip line is much closer to the controller line at no load than it is at full load. At no load, only a small disturbance is required to trigger the anticipator, whereas at half load, a much larger shock (and corresponding change in θ_c) is needed to trigger the anticipator. The trip line shown represents the HV-1000 without an external potentiometer. It is interesting to observe that above half load, the trip line actually lies below the stall line. This means that in this region the anticipator can only be tripped by a very large, sudden shock load, which actually pushes θ_c momentarily below the stall line. In theory, there exists a certain size and rate of change of shock, which is fast enough that the controller cannot respond normally, and yet slow enough that the anticipator is not tripped. For this particular motor, there was no problem in practice; however, there are motors with a relatively higher stall line, where it is apparent that adding the HV-1000 clearly does cause premature stalling. In this case, it is necessary to increase the sensitivity by moving up the anticipator trip line. This is controlled by the absolute value of the external potentiometer when added on pin 4, 5 and 6. 5k ohms raises the trip line by 100 microseconds, 10k ohms raises it to 200 microseconds.

Adjusting the set point of the potentiometer allows the controller line to be moved vertically up and down on the θ_c axis. For small absolute values (e.g. 1k) the motion is essentially upwards only, and depending on the motor, may not be sufficient to apply full voltage to an unloaded motor. A 10k potentiometer will allow up to 500 microseconds of downward movement and will permit even an unloaded motor to have full voltage applied. When the controller line is slewed up and down with an external potentiometer, the anticipator trip line is automatically moved by the same amount in the same direction so that the relationship between the two lines is unchanged. This relationship can only be changed by modulating the absolute value (not the ratio) of the potentiometer. As a starting point where a potentiometer has to be added to optimise the control line for a given motor, a 2k potentiometer is recommended. Smaller absolute values give a lesser range of control, while larger values tend to make the anticipator too sensitive and the potentiometer setting too critical.

The HV-1000 self-adapts to different motors:

It is illuminating to reflect that, different motors have their no load, half load, etc. curves differently placed on Figure 2, while the contoller line is fixed. Then, when the HV-1000 is applied to different motors, entirely different values of θ_c and θ_t will result at say, no load or half load. This in sharp contrast with the earlier generation of IMES devices which simply forced every motor to a constant θ_c. It can be seen that because of the sloping characteristic of the controller line, the HV-1000 can apply different values of θ_c and θ_t at no load to each motor according to its need. In other words, the HV-1000 has a degree of self-adaptability. It can accomodate a surprisingly wide range of motors using its internal settings without an external potentiometer. The HV-1000, without a potentiometer, will control a majority of fractional horsepower American induction motors. However, when sufficiently common requirements are identified, HV-1005 and HV-1010 are planned, which will have the controller line set at different points on the θ_c axis.

NON STANDARD BEHAVIORS OF THE HV-1000

As stated previously, the HV-1000, with no potentiometer, will do a fairly good job of driving most U.S., fractional horsepower, induction motors most of the time. In this section, we describe a number of circumstances in which undesirable effects can manifest themselves. Most of these are relatively rare, and most represent oversights in the design of the application circuit.

Instability:

The symptom here is the motor shaft drives the load in short, erratic, violent bursts. An erratic banging noise may be heard. This problem is worse with relatively big (above 1 HP) motors for which the ratio of the torque available to the rotor inertia is more extreme. A special kind of application circuit is needed to control the motor in this circumstance, as described in the next section. Motors from different manufacturers vary greatly in their behavior with respect to this problem.

Anticipator banging:

The symptoms of the problem are that the controller rhythmically applies full voltage with a bang, then slowly throttles back until full voltage is again applied with a bang. The periodicity is fixed by the external time constant capacitor. This problem is easily fixed, but very disconcerting when first observed. Refer to Figure 2. It can be seen that inside the no load – full load range of the motor, the anticipator trip line does not intersect the controller line. This is not always the case – suppose, for instance, that the anticipator trip line had been deliberately shifted up with an external potentiometer, when it might intersect the controller line inside the operating area, or possibly a different motor might have characteristics shifted relatively to the right in Figure 2. Again, the intersection of the controller line and the anticipator trip line could come inside the motors operating area (although in practice this has never yet been observed without an external potentiometer). Suppose the system of motor and IMES had just had a heavy load removed. The operating point will relax along the "no load" line CB with a speed fixed by the time constant capacitor. If the anticipator trip line has been moved upwards sufficiently, the operating point will encounter the anticipator trip point before the controller line. The anticipator will then fire, transferring the operating point abruptly to point C. The operating point will then start off along CB again. The cure is to either place a slight load on the motor or to reduce the absolute value of the potentiometer, shifting down the anticipator trip line. If a resistor is being used in series with pin 5, its value should be reduced.

Latch up:

In this circumstance the HV-1000 simply does not throttle back after reacting to a full load. This is normal, expected behavior associated with too high a value of external potentiometer. It normally starts at about 10K ohms, but is somewhat motor dependent. The cure is to reduce the absolute value of the potentiometer or the resistor in series with pin 5.

Gross rectification:

Here the controller applies half rectified AC to the motor, causing it to vibrate loudly and not turn. Switch off at once. It is caused by too small a time constant capacitor. It cannot happen with a time constant capacitor above 0.1μF.

Glitching:

With this effect, the symptom is that the motor intermittently gets a higher voltage applied to it. The effect is infrequent and non-periodic. The most likely cause is voltage spikes on the AC line breaking over the input protection crowbars. When this happens, the output SCRs are usually turned on delivering full power to the motor. The input protection crowbars fire at ±500V. This symptom can sometimes be helped with a capacitor (high voltage!) between pins 1 and 16. Sometimes also electrical noise, even from the firing of the TRIAC, can cause the anticipator to fire prematurely. Placing 0.01μF (5V) between Pins 1 and 12 usually stops such problems, since such noise normally comes in on the phase sense lead, Pin 12. Since A.C. power lines are often full of spikes, infrequent glitches are regarded as normal HV-1000 behavior. They do not detract from power savings and are the means by which HV-1000 protects itself.

DESIGNING THE APPLICATION CIRCUIT FOR HV-1000

A general purpose application circuit for the HV-1000 is shown in Figure 3. This is the simplest application circuit possible, and will satisfactorily drive a large percentage of U.S., fractional horsepower, induction motors. The TRIAC must be capable of handling the locked rotor condition of the motor for as long as this condition may exist. This is often as much as three times or more the normal running current of the motor – as high as 30A for a typical 115V, ½ HP motor. Normally the TRIAC will require some kind of heat sink – eight or ten watts power dissipation in not, uncommonly encountered. The snubber shown is primarily for illustration. Its purpose is to minimize radio frequency interference, prevent high frequencies being sent down the AC line, and to attenuate the inductive voltage kickback, which appears at the zero crossing of the current through the motor, from accidentally triggering the output stage of HV-1000 or the TRIAC. In some circumstances, the snubber capacitor and resistor can be eliminated completely, and the system will still run normally, although generating a lot of radio frequency noise. Different sizes of capacitors will also work.

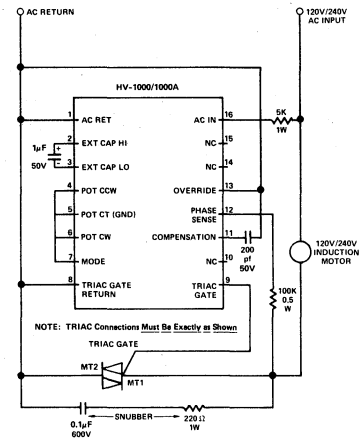

Figure 3. Basic Application Circuit For HV-1000

The 5K ohm resistor shown is for surge protection – in the event of an overvoltage surge, internal protection clamps between pins 1 and 16 breakover and latch down to 1.5V, momentarily dropping all the voltage across this resistor. This voltage can be many kilovolts for a few microseconds, and even though the power dissipation is low, the physically large size

of a 1W resistor is needed to stop arcing from taking place between the terminals and to absorb the energy of the surge. The 1μF capacitor sets the response time constant for the system. Figure 4 shows the relationship between capacitor size and response time of the system. It must be kept in mind that this is basically the time in which the IMES throttles back the voltage after removing a heavy load. The load anticipator will always stop the motor from stalling when the load increases sharply. The sensitivity of the load anticipator can be enhanced by adding an external potentiometer. Even with the potentiometer shorted, the HV-1000 will still produce full power in response to extremely sharp load shocks. The greater the absolute value of the potentiometer, the more sensitive is the load anticipator.

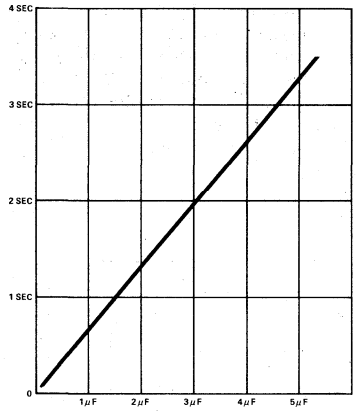

Figure 4.
HV-1000 Response Time as a Function of Capacitor Size

The criteria for satisfactory operation of the HV-1000 IMES circuit are that full line voltage should be applied to the motor when it is close to full load, and that the motor should not stall when exposed to a shock load. Also, the motor should run smoothly at all times without any juddering or vibration. The energy savings should normally be around 50% at no load, diminishing to essentially nothing at full load. A typical plot of Power In against Power Out for the HV-1000 with a ½ HP, Century, electric motor is shown in Figure 5. Remember that in many kinds of equipment, the "no load" losses associated with driving pulley belts and bearings may be sufficient to load the motor by 50 or 100 watts, so the true

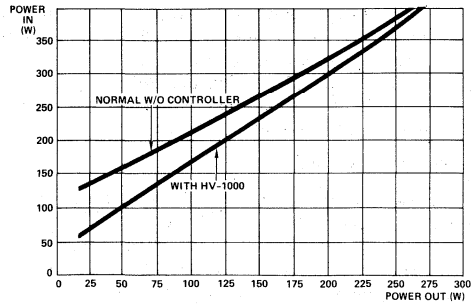

Figure 5.
Power Savings of the HV-1000 on a ½ HP Motor

no load savings of the motor may not be seen.

If the motor stalls more easily with the HV-1000 IMES than it did before, this means that the anticipator trip line is probably too low for the motor and needs raising as described previously. The anticipator sensitivity can be increased with the use of an external potentiometer as shown in Figure 6. A 5 kilohm potentiometer will commonly give a sufficient increase in sensitivity. Ten kilohms gives an extreme increase. If the absolute value of the potentiometer is too high, the motor will observed to give a bump or bang as it gets full power in response to the slightest disturbance. In the extreme case, the rhythmic

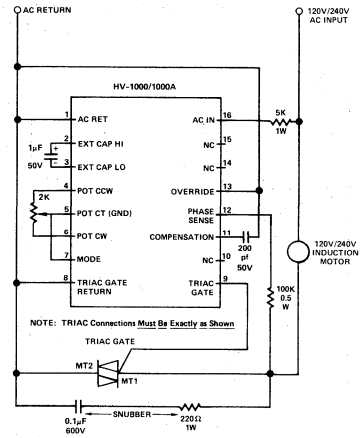

Figure 6.
Application Circuit for the HV-1000 with Potentiometer to get Increased Anticipator Sensitivity and Adjustable Phase Setting.

anticipator banging described in the previous section will be seen. The angular setting of the potentiometer has to be set so that the motor is given full voltage at full load, or produces optimum power savings in the application at hand. (Some motors exist which give optimum power savings when full voltage is only applied at twice full load.) If a piece of equipment is being manufactured containing the HV-1000, then once the potentiometer settings are established, the potentiometer can be replaced by two resistors having the same values. If many hundreds of thousands of such parts are needed, the equivalent resistor settings can be incorporated inside the HV-1000 by arrangement with the factory.

If difficulties with the stability of the motor being controlled are encountered, as descibed previously, special precautions are needed. The nature of the instability is that the controller may over-correct the voltage in response to a small disturbance in the motor's load. Thus the instability comes about as a result of the relationship between the response times of the motor and controller — for disturbances of a certain frequency, the controller's response may be lagging that of the motor by half a cycle, so the controller is actually increasing the voltage at a point in time when it should be decreasing it. Frequently,

the inertia of the motor's normal load slows down the motor's response sufficiently to produce stability. Failing this, capacitor values as large as 10μF or as small as 0.1μF can be tried between pins 2 and 3. If all these simple expedients are not effective, the remedy is to tailor the frequency response of the controller with a circuit like that shown in Figure 7. This circuit is shown for example only, it was found to be optimal for a 1.5 HP Emerson motor. For other motors, slightly different values of the compensation network components connected to pins 2 and 3 may be needed. The purpose of the diode across the 50K resistor is to permit the load anticipator to discharge the 3μF capacitor rapidly, when necessary. At the time of writing no motor has yet been found which could not be stabilized by a compensation network of the general type shown between pins 2 and 3 in Figure 7.

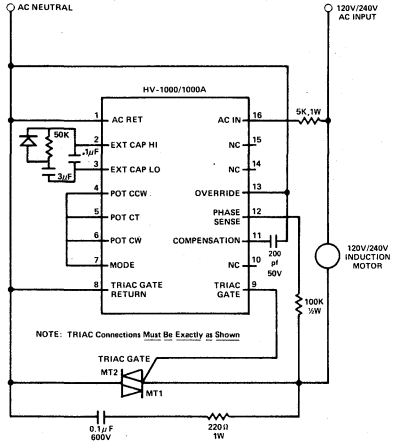

Figure 7.
Application Circuit for a 1½ HP Motor Which Showed Instability with the Basic Application Circuit.

SPECIALIZED APPLICATION FEATURES OF HV-1000

Tailoring the response curve:

Referring to Figure 2, the reader will remember that the HV-1000 controller line is a line sloping down to the right, by contrast with earlier generations of IMES, which had a horizonal (constant θ_C) characteristic. For specialized purposes, typically involving stability, the HV-1000 controller line can be made into a horizontal line if desired. This is done simply by not contacting Pin 7, the Mode pin. A consequence of this is that the load anticipator sensitivity then becomes independent of load. For historical reasons, this is called "single slope" operation. Operation with pins 7 and 5 strapped together is called "dual slope". In single slope operation, the controller loses its self-adaptive property.

Moving back the phase setting without increasing the anticipator sensitivity:

So far the only method of moving down the controller line (reducing θ_C) described has involved the use of a potentiometer which has the side effect of increasing the anticipator sensitivity. To reduce θ_C without affecting the anticipator, try placing a low voltage (5V) capacitor between pins 1 and 12. 0.05μF reduces θ_C about 0.5 msecs and shifts the anticipator trip point by the same amount in the same direction.

Over riding the control function:

There are certain circumstances in which it may be necessary or desirable to disable the control function completely, and simply feed the straight line voltage to the motor. This can be done using pin 13, which is a TTL logic input. It is activated by the application of +2.4V with respect to pin 1 and a current of 0.1mA. Doing this triggers the load anticipator. Figure 8 shows this feature being used with the 0.1mA being derived from the AC Input, Pin 16. This figure also shows pin 7 open to produce single slope operation. The diode shown between pins 13 and 1 is to prevent negative polarity voltages being applied to the TTL input, pin 13. (Not using this diode would result in degraded long term reliability.) In this illustration the positive voltage to trigger the logic input each cycle is being derived from the AC input power.

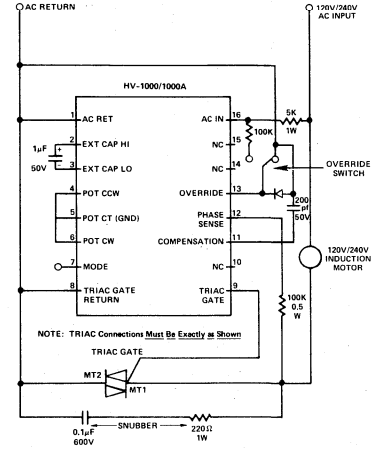

Figure 8.
Application Circuit for the HV-1000 Illustrating Single Slope Operation and Electronic Override.

Circumstances in which the overide might be needed include when equipment other than the motor are connected to the motor and need momentary full voltage. Also it sometimes happens that TRIACs fail by turning into a diode in one direction. In this case, circuitry could detect the imbalance and apply a voltage to pin 13, turning the IMES full on most of the time, and preventing essentially direct current from being applied to an AC motor.

Full power starting:

As a generalization, the HV-1000 will start the motor with full power. When the system has been previously inactive, the time constant capacitor will be discharged corresponding to full power. Also for most motors, the transients associated with starting will usually trigger the load anticiapator, again producing a full power start. However, there are certain special

circumstances where HV-1000 may not produce a full power start.

a) If a motor is driving a light load, so the time constant capacitor is fully charged, and switched off momentarily while a full load is applied; then, when the motor is switched on again, the HV-1000 may "soft start" for a fraction of a second. This tendency can be minimized by using a larger time constant capacitor and by increasing the load anticipator sensitivity with an external potentiometer or resistor. If the behavior is frequent and totally unacceptable, a complete fix is to use the application circuit for electronic override shown in Figure 9. Here the 100kohm resistor which sends the line voltage to pin 13 is replaced by 0.01μF to the start capacitor of the motor. Thus all the time the starter winding is operating, the HV-1000 is commanded to full voltage, guaranteeing a full power start. Since the start capacitor terminals may be inside the motor, this circuit is best suited for motor manufacturers.

b) In some installations the presence of a switch between the HV-1000 and the motor may be unavoidable. When the switch is opened, the HV-1000 will slew to minimum output voltage. In most cases the transient associated with switch closure will trigger the load anticipator, but this can not be guaranteed. Sometimes a "soft start" may then occur. A fix for this circumstance is to place a 0.01μF line-power voltage capacitor across the motor and its switch. This "closes the loop" on the HV-1000 control system even when the switch is open. The result is that the HV-1000 will slew to full voltage, not minimum voltage, when the switch is open, guaranteeing a full power start. For example, in the context of an after-market add on controller, the 0.01μF is placed across the output terminals of the controller.

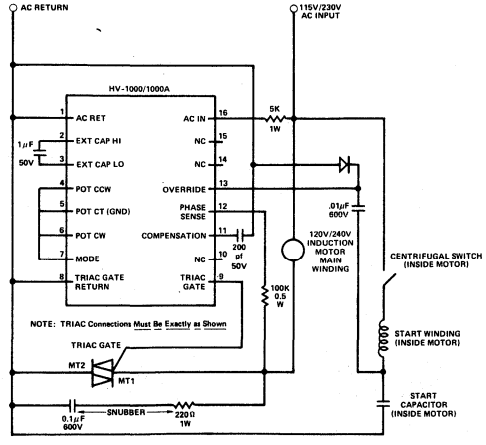

Figure 9.
Application Circuit Which Ensures Full Power Starting Under All Conditions.

MEASURING POWER SAVINGS

A relatively simple and inexpensive power meter can be obtained from the Robinaire Manufacturing Company of Montpelier, Ohio. For many times the price a sophisticated watt-volt-amp meter (Model 259 V.A.W. meter) is sold by Clarke Hess Communications Research Corporation of New York City. Used utility company kilowatt hour meters, rebuilt and recalibrated, can be obtained from the Hialeah Meter Company of Hialeah, Florida.

All of the above will give slightly differing results for power savings, because of the different ways in which they react to the high frequency components in a TRIAC chopped current.

SAFETY

The HV-1000 application circuits shown in the previous figures contain linepower voltages which can be lethal under certain conditions. In assembling and testing such circuits all precautions relevant to the safe handling of 120V and 240V AC should be observed.

In some instances, TRIACs have been known to fail through overheating in such a manner that they resemble a diode in one direction. If no other precautions are taken, an HV-1000 IMES circuit under this circumstance will end up supplying a large component of direct current to the motor, which will not be limited by the inductance of the windings. The motor may overheat, unless it is thermally protected, as are most motors made today. Alternatively, a sense circuit can be devised to detect the rectification and trigger the HV-1000 via the Override, Pin 13.

If the TRIAC fails in the off or open circuit state, the HV-1000 will be destroyed immediately, since it is not designed to carry significant amounts of line current.

HANDLING PRECAUTIONS AND RELIABILITY

Although the HV-1000 can survive multi-kilovolt surges in its application circuit, the chip by itself is sensitive to electrostatic discharge, and precautions should be taked, and handling, to prevent accidental "zapping" of the dual in-line package.

If the HV-1000 is inadvertently inserted backwards into its socket, the chip is not damaged. Usually, the motor will be observed to run without any control. Normal operation will resume when the package is rotated.

Because of the relatively high voltages (including multi kilovolt lightning surges) to be found on the HV-1000 circuit, it is recommended for best reliability, that if a printed circuit board is used, the

conductors having large potential differences should be widely spaced. Coating the whole assembly with resin or varnish will usually improve the reliability achieved.

ACKNOWLEDGEMENTS

The authors wish to acknowledge several helpful conversations with Frank J. Nola of the NASA Marshall Space Flight Center. The development of the HV-1000 was aided by the donation of a motor collection by Reliance Electric, Leeson Electric, Gould Electric, Bodine Motors and Emerson Electric. Illuminating comments from the engineering staff of Doerr Electric and the G.E. General Purpose Motor Division were invaluable.

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HARRIS

APPLICATION NOTE 543

NEW HIGH SPEED SWITCH OFFERS SUB-50ns SWITCHING TIMES

BY CARL WOLFE

INTRODUCTION

An ideal CMOS analog switch would exhibit such characteristics as zero resistance when turned on, infinite resistance when turned off, zero power consumption, and zero switching time. Unfortunately, such a device is usually found as an example in a college textbook. The real world offers tradeoffs and imperfections which prevent the realization of the ideal. The integrated circuit designer works within these limits and attempts to optimize device performance by utilizing new technologies and improving circuit design. The development of a new high speed analog switch required the use of both of these techniques to achieve its performance. (See Appendix I: "Inside the HI-201HS").

The HARRIS HI-201HS is the industry's first sub-50ns monolithic analog switch and along with fast switching speed, offers improved performance and pin compatibility with industry standard 201's (Fig. 1). This article will discuss the technology, performance, and applications for this product.

IMPROVE THOSE EXISTING DESIGNS

The application circuits which follow are examples of typical applications and illustrate how the HI-201HS can improve existing applications where standard 201's are presently being used.

The first example is a high speed multiplexer shown in Fig. 2. The analog multiplexer is a circuit which switches a number of analog inputs to a single output and is used heavily in data conversion and avionic applications. This function can be easily achieved with the HI-201HS by tieing the outputs together and selecting the appropriate analog input. The HI-201HS is an excellent choice for this application since its low on resistance and leakage current will reduce system error, and its high speed is unmatched by any other monolithic analog switch. Since the output capacitance is additive, the RC time constant of the load will increase when the outputs are made common.

The next application is a high speed sample and hold which takes advantage of the improved performance of the HI-201HS and the precision F.E.T. input of the HA-5160 high slew rate amplifier. A sample and hold circuit or track and hold as it is sometimes called, has two operating modes. In one mode the switch is closed and the capacitor charges to the input voltage. The second mode occurs when the switch is opened and the capacitor holds this charge for a specified period of time.

The speed of a sample and hold circuit is directly related to the switching device used and the output amplifier. This characteristic of a sample and hold circuit is called the acquisition time. It is defined as the time required following a "sample" command, for the output to reach its final value. The acquisition time includes the switch delay time, the time constant of the switch on resistance and hold capacitor ($T = R_{ON} C_{HOLD}$), and the slew and settling times of the output amplifier.

The photographs shown in Fig. 3 illustrate the improvement in the acquisition time possible by using the HI-201HS. The first photograph represents the sample/hold circuit using a standard 201 switch and an HA-5100 operational amplifier. The first waveform is the "Sample" voltage (V_A). The second waveform is the voltage on the hold capacitor (V_1). And the third waveform is the output of the amplifier (V_2).

The second photograph is the same circuit with a HI-201HS and on HA-5160 op amp. Comparison of the photographs shows the HI-201HS has significantly reduced the switch delay time and the high slew rate of the 5160 amplifier has also contributed to the reduced acquisition time.

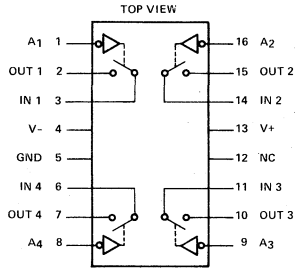
A source of error in this circuit is a d. c. offset which is called sample to hold offset error. This error is

primarily due to the charge injection (Q) of the switch and is related to the hold capacitance by the following expression,

$$\text{offset error } (V_O) = \frac{\text{charge transfer (Q)}.}{C_H}$$

The reduced charge injection of the HI-201HS (typically 10 pc) will result in immediate reduction of this error.

Using analog switches with operational amplifiers is common in circuit design. An example is shown in Figure 4 which is an integrator with start/reset capability.

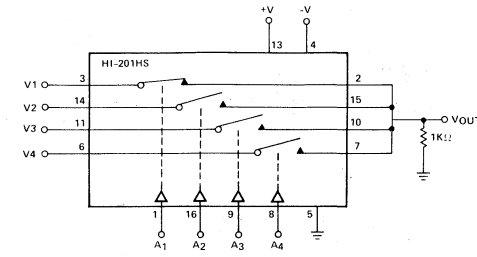


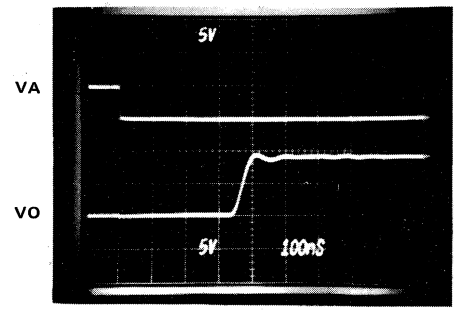
LOGIC	SWITCH
0 - $V_{AL} \leq .8V$	ON
1 - $V_{AH} \geq 2.4V$	OFF

TYPICAL SPECIFICATIONS (±15V Supply)

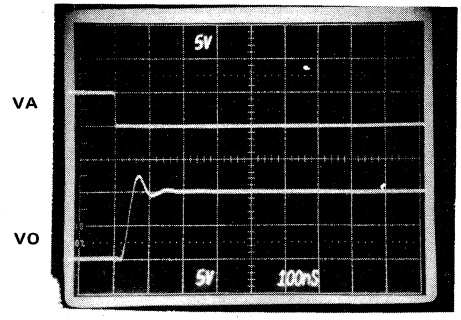
Analog Signal Range	±15V
On Resistance	30Ω
Off Leakage	.3nA
Switch On Time	30ns
Power Dissipation	120mW

Figure 1. Typical Pinout and Specifications — The HI-201HS is pin compatible with standard 201's and offers improved performance. Specifications given are typical values at T_A = 25°C.





(a)



(b)

Figure 2. High Speed Analog Multiplexer: (a) circuit response using the standard 201 (T_{access} = 400ns) (b) circuit response using HI-201HS (t_{access} = 50ns). The access time is defined as total time required to activate an "off" switch to the "on" state. Access time is normally measured from the initiation of the digital input pulse (V_A) to the 90% point of the output transition.

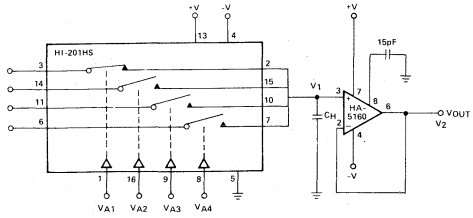


Figure 3A. High Speed Sample and Hold: The basic sample and hold samples the input voltage when the switch is closed and the capacitor holds the voltage when the switch is open. The speed of the switching element affects the speed of the sample and hold.

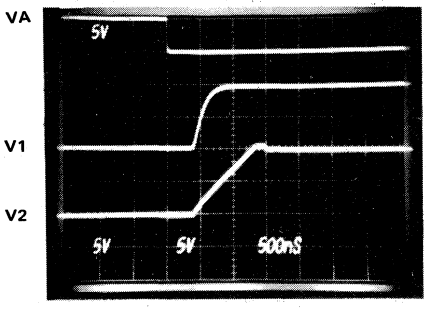


Figure 3B. Circuit response to a "Sample" command using a standard 201 and an HA-5100 operational amplifier (Acquisition time = 1.5μs)

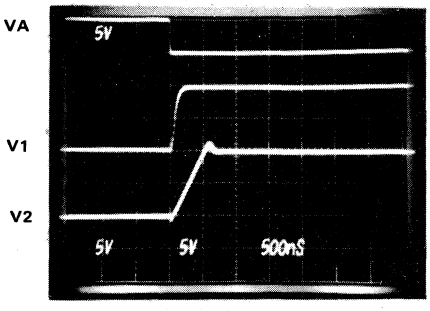


Figure 3C. Circuit response using an HI-201HS and HA-5160: HI-201HS significantly reduces switch delay time. (Acquisition time = 500ns)

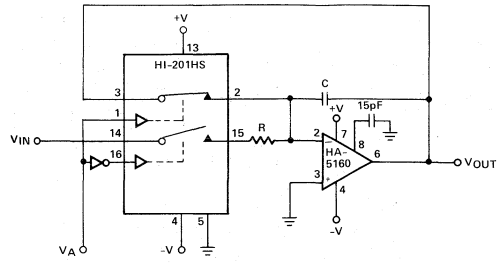


Figure 4A. Integrator with Start/Reset: A low logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input changes to a high state, integrator is activated.

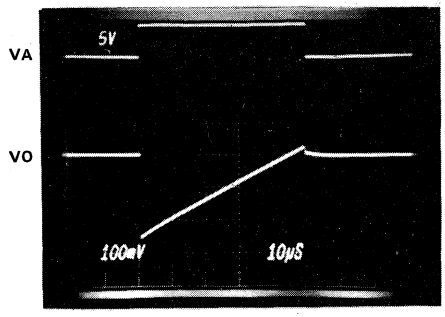


Figure 4B. Low Level Integration— Circuit response using standard 201 switch.

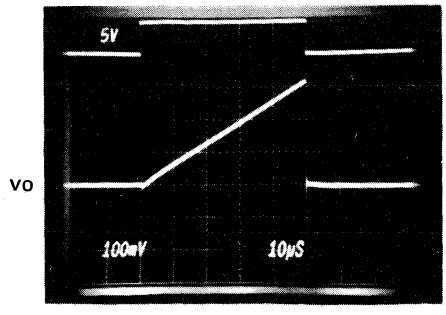


Figure 4C. Low level integration—Circuit response illustrates improved charge injection of the HI-201HS.

The switch is used to apply the input signal and to reset the integrator. Applying a low logic level removes the input signal and the capacitor is discharged. When a logic level high is present, the input signal is integrated with a rate of change equal to

$$dvo/dt = i_f/C_f = -V_i/R_1C_f$$

The reduced on resistance, leakage current, and charge injection of the HI-201HS will improve the performance of this circuit and an example of this improved peformance can be seen in the photographs in Figure 4. These photographs illustrate the reduced charge injection which the 201HS offers. The component values are R_1 = 1MΩ , C = 150pF and V_{IN} = -1V. With these values, the amplifier will integrate the input signal with a slope of 6.6mv/μs. For a 50μs time period, the amplifier will integrate to a magnitude of ≈ 300mV. The photographs of the test results indicate this to be true, but it should be apparent that the two photographs are quite different. The first photograph represents the amplifier output using a standard 201 as the reset switch. The second photograph is the same circuit with a 201HS.

The offset error in the first photograph is due to the charge injection of the switch. Using the expression Q = V x C and knowing the standard 201 has a typical charge transfer of 30pc, this offset can be calculated. V = Q/C = 30pc/150pf=200mV.

Other examples of combining switches and amplifiers are shown in figures 5 and 6. In both these applications the switch is used to tailor the amplifiers performance. Figure 5 is a low pass filter with a selectable break frequency.

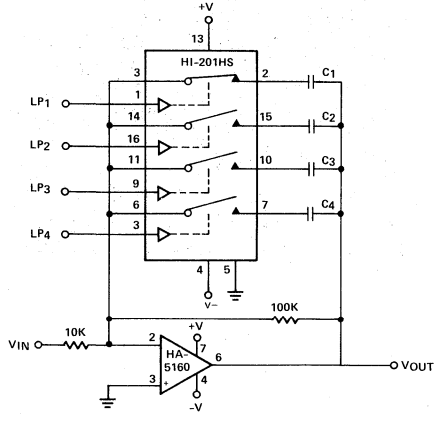


Figure 5. Low Pass Filter with Selectable Break Frequency— Switch selection places various values of capacitance in parallel with the feedback resistor. The value of the capacitor determines the break frequency. The break frequency is that frequency at which the signal begins attenuation.

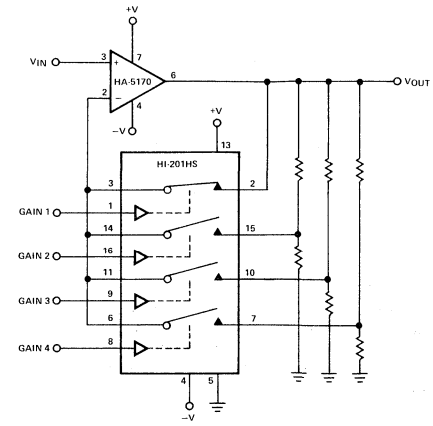


Figure 6. Amplifier with Programmable Gain— Switch selection activates a new voltage gain which is determined by the resistive feedback.

Depending on which switch is selected, a particular cutoff frequency is introduced by the expression,

$$F_C = \frac{1}{2\pi R C_x}$$

A programmable gain amplifier is shown in Figure 6. Similar in function to the filter application, the gain of the amplifier is determined by selection of a switch.

When using switches with other components it is important that a switch be selected which introduces a minimal amount of error to the circuit. Operational amplifier gain error due to high on resistance or offset voltages due to excessive leakage current and charge injection are examples of potential error created by the switch. The previous applications have demonstrated that the 201HS offers improved performance by minimizing circuit error and increasing system speed.

ON THE DRAWING BOARD

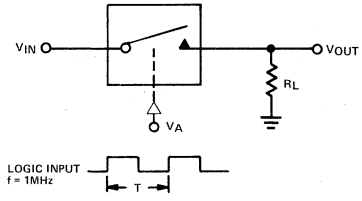
Since the introduction of the HI-201HS switch, many engineers have expressed an interest in using this new product. Although much of their work is in a preliminary stage and they do not want to divulge exact details on their designs, the following information is intended to give you an idea of how other engineers are considering using the HI-201HS.

The majority of the engineers are interested in taking advantage of the products fast switching speed. One particular engineering group is investigating replacement of DMOS (double-diffused MOS) transistors with the HI-201HS.

The DMOS transistor is capable of extremely fast switching speeds (1ns) and until now, switches

fabricated using CMOS technology have not been fast enough to be considered. But the HI-201HS is attractive since it offers unprecedented switching speed along with the established benefits of CMOS technology. Such benefits include a wider analog signal range capability and lower operating power requirements.

A common application for analog switches is time division multiplexing, where many signals are processed on a single channel. High speed switching allows higher information capacity on the channel, since the switching speeds of an analog switch are directly related to the maximum switch activation frequency. The faster a switch can turn on and off, the higher the possible switching frequency. An example of this relationship is shown in Figure 7. If a switch is activated at a frequency of 1MHz, it must turn on and off within a 500ns time period. Since the HI-201HS has a maximum on and off times of 50ns, and can turn on and off within a 100ns time period, it theoretically possible that it can be activated at a 5MHz frequency rate. This improved capability is making the HI-201HS an attractive component to design engineers requiring high frequency data processing. Conversations with engineers indicates that possible applications are computer graphics and visual display circuit designs.



$T = 1/f$
$T = 1/10^6$
$T = 10^{-6}$ sec = 1 μs
$\frac{T}{2}$ = 500ns

Figure 7. High Frequency Switching — HI-201HS fast switching times allow it to transfer data at a higher rate of frequency.

Another area where the HI-201HS is generating interest is in the area of medical electronics. This is a growing field and improvements are continously being made as products become available much of the medical equipment being designed requires both high speed and accuracy.

Medical test equipment is primarily used to transmit or receive information from the patient. An example where both these functions are used is in the area of ultrasound. Ultrasound testing requires that a signal be transmitted to the patient and the return signal is then amplified and displayed or recorded. The 201HS is being considered for the use in such an application and would be used to control the transmission and reception of these signals.

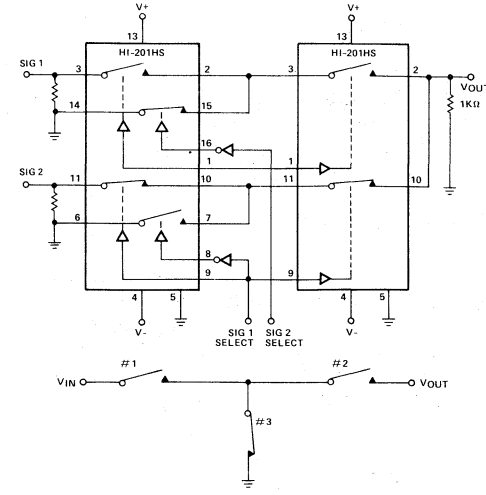


Figure 8. Video Switching with Improved Isolation— Improved high frequency off state performance is obtained by using a T-Switch configuration. When two series switches are off, the third switch is shorted to ground.

The designers are not only interested in fast switching speed, but also in low on resistance. This is an important aspect of the switch since many of the electrical signals in medical electronics are of a small magnitude. An example is patient monitoring equipment which converts physiological parameters into electrical signals. If these low level electrical signals require switching before amplification, a low on resistance switch is essential to minimize the voltage drop across the switch itself. The low on resistance of the HI-201HS enables it to be used in applications using signals of smaller magnitude.

Video circuit design involves the control of high frequency signals. Applications which require the switching of these high frequency signals are usually limited by the off isolation and crosstalk performance of the switch. Off isolation is defined as the amount of feedthrough of an applied signal through an off switch. Crosstalk is the amount of cross coupling of an "off" channel to the output of an "on" channel. Both of these switch characteristics will degrade as the frequency of the input signal increases.

The HI-201HS has some improvement over the standard 201 in these areas but the configuration shown in Figure 8 is being used by designers to improve the isolation capabilities of CMOS analog switches. This configuration is known as "T" switching since the three switches used for passing the signal could be thought of in the shape of the letter T. The simplified figure shows that when switches # 1 and # 2 are off, switch # 3 is tied to ground. When switches # 1 and # 2 are on, # 3 is off. This improves isolation by having two channels in series off and any feedthrough is fed to ground.

CONCLUSION

The HARRIS HI-201HS is the fastest monolithic CMOS analog switch available. It offers improved performance for existing designs and should be considered for use in any application where switching speed is an important criteria.

ACKNOWLEDGEMENTS

The author would like to thank Gary Maulding, Frank Cooper, and Bob Junkins for their technical assistance, Ken Timko and Dick Whitehead for their editorial comments, and the dynamic duo of Lilly Andrews and Kathy Glines for their secretarial skills and patience in the preparation of this paper.

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3. J. A. Connelly, "Analog Integrated Circuits" New York: John Wiley & Sons, 1975.

4. HA-2420/2425 Fast Sample and Hold data sheet, Harris Semiconductor.

APPENDIX I - INSIDE THE HI-201HS

The HI-201 is a TTL compatible quad CMOS analog switch which features switching times under 50ns and a typical "on" resistance of 35Ω. The fast switching times are achieved through a combination of process and circuit design techniques. The HI-201HS is fabricated using a dielectric isolation process with complementary PNP and NPN bipolar transistors and polysilicon-gate CMOS. The use of bi-technology process enabled a unique circuit called a D. C. Static Level Shifter to be designed.

The typical CMOS analog switch consists of a switch cell which is driven by a level shifter. The level shifter converts a single logic input into two complementary outputs which drive the gates of the CMOS switch cell (Fig. A). The switch cell represents a capacitive load to the level shifter, so fast switching times require large drive currents to charge these capacitances quickly. The D. C. Static level shifter circuit (Fig. B) provides large drive currents only when switching and dissipates little power in a quiescent condition.

The D. C. static level shifter achieves high switching speeds through the use of a unique bipolar input stage and a network of switching and holding MOS transistors. Devices MN5, MP5, MN9 MP9 are the switching transistors and MN6, MP6, MN10, MP10 are the holding transistors. The major advantage of the bipolar input transistors is that its transconductance (g_m) is much higher than that possible with F. E. T. transistors.

To understand the level shifter operation, consider a change of logic input from low state to high. Initially V_A is low, $Q = Q_1 = Q' = -15V$ and $\overline{Q} = \overline{Q_1} = \overline{Q'} = 15V$. VB is at ground and QN2, QP2 are off. When V_A goes high, QN2, QP2 turn on, which slew the gates of switching devices MN5, MP5 with a current $I = (V_A - 2V_{BE})/R$. The switching devices overcome the holding devices, MN10, MP10 and switch the internal nodes Q_1, and $\overline{Q_1}$. CMOS buffers I_{11}, I_{13} provide large drive currents to the switch cell, while inverters I_{12}, I_{14} provide delayed feedback signals. The feedback signals turn off holding devices MN10, MP10 while turning on holding devices MN6, MP6. The feedback also turns on QN2, QP2 by means of MN1, MP1. These feedback signals have returned the level shifter to a static condition by turning the bipolar input stage and MOS switching transistors off.

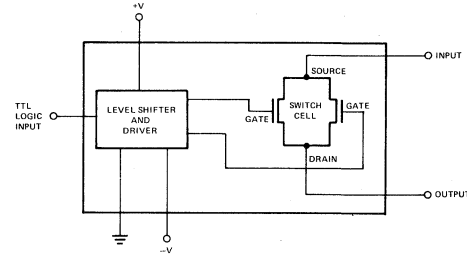


Figure A. Simplified I. C. Analog Switch Operation— Level Shifter converts logic input into drive signal for CMOS switch cell.

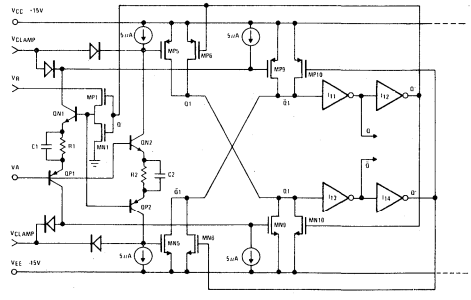


Figure B. Simplified D. C. Static Level Shifter — The level shifter consists of a unique bipolar input stage and a network of switching and holding devices.

Similar operation occurs when V_A goes from high to low, bipolar transistors QN1, QP1 turn on MN9, MP9. The feedback resets the holding devices and turns off the bipolar input stage.

APPENDIX II HI-201HS VS. STANDARD 201

The use of a dual technology process and a creative design improves the performance of this analog switch. The following table illustrates the results of this combination by comparing the specification of the HI-201HS with the standard 201.

It should be apparent from Table 1 the substantial improvement in switching speeds offered by the HI-201HS. But since the switch "off" time of the high speed switch is measured differently from the standard 201, a brief discussion of test methods will avoid any confusion.

Figure A is a typical switching time test circuit for an analog switch. The "on" time is measured from the logic input to the 90% point of the output.

The "off" time can be measured from the logic input to either the 90% or 10% point of the output. This variation in the "off" time test point is due to the dependence of the measurement on the load. The dominant component of the switch "off" time is an exponential RC time constant determined by the values of the load resistance and capacitance. The "off" time of the HI-201HS is measured to the 90% point. The RC time constant due to load is excluded from this measurement. The photograph included in Figure A is a typical HI-201HS switching time response.

The remainder of table one compares other critical specifications of CMOS analog switches. The HI-201HS is not only a high speed switch but also offers improved performance in other areas. The parameters of "on" resistance, leakage current, and charge injection can all contribute unwanted errors to system level applications. With the improvements shown in these areas, the HI-201HS offers potential improvement in system accuracy for a wide variety of applications. and since the HI-201HS is pin compatible with existing 201's, the high speed version can be plugged into existing designs for immediate improvement in performance.

The HI-201HS is an improvement over the standard 201 in many areas, but some trade-offs still exist. One such trade-off was the power dissipation of the product. In order to meet the high speed criteria, larger internal currents are needed which in turn demand increased supply current. But this apparent shortcoming is more than offset by the products performance.

Parameter	Temperature	HARRIS HI-201HS	HARRIS HI-201
Switching Speed			
t_{ON}	25°	50ns	500ns
t_{OFF}	25°	50ns	500ns
ON Resistance	125°	75Ω	125Ω
Leakage Current			
I_{SOFF}	125°	100nA	500nA
I_{DOFF}	125°	100nA	500nA
Charge Injection Q	25°	10pc (typ)	30pc (typ)
Power Dissipation Pd	125°	240mw	60mw

Table 1. Specification Comparison: Improved performance of HI-201HS over standard 201's (all values are maximums unless stated otherwise).

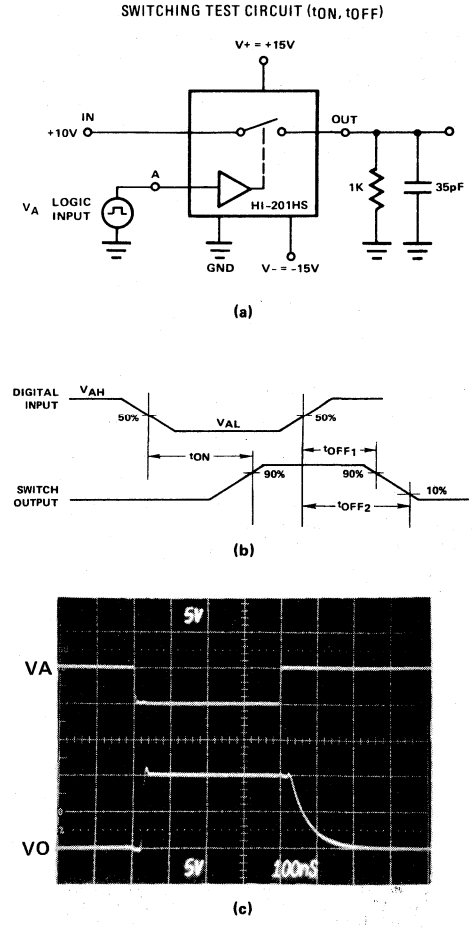


Figure A. Switching Time Test Circuit: (a) Switching test circuit, (b) Switching waveforms, (c) Typical HI-201HS response.

HARRIS

APPLICATION NOTE 545

NEW MULTIPLEXERS SIMPLIFY SYSTEM DESIGN

T. R. FLEMING
T. M. WESTENBURG

INTRODUCTION

Monolithic analog multiplexers have been available since the early seventies. They provide simple switching functions and have undergone relatively few design changes. However, system designers have established three desireable attributes which widen these products. range of application and save board area where they are used.

- Latched channel address inputs
- Overvoltage protection
- High impedance at the channel inputs with power off

These features have been available separately,but only the new HI-50XL family from Harris Semiconductor combines all three in a single product.

Latches for the channel address are required in many cases, so these have been provided on-chip. (If not needed, they may be wired in the "transparent" mode). Overvoltage protection is needed when channel inputs connect directly to a user-accessable interface; having this protection built into the multiplexer often eliminates the need for external resistors and diodes. Finally, high analog input impedance with power off is very welcome in the design of redundant systems, where a powered-down standby MUX may be wired in parallel with an active one.

These products form a conventional multiplexer family: HI-506L/507L, 16 Channel Single Ended/8 Channel Differential versions; and HI-508L/509L, the 8 Channel SE/4 Channel Differential versions. The term "50XL" refers to this product family. In the following sections, the new switch is compared with older designs and the 50XL control signals are described. Next comes a discussion of tradeoffs associated with different methods of interface to a microprocessor system, and a detailed description of a typical application.

NEW SWITCH DESIGN

The switch cell of the 50XL has a different structure than earlier Harris designs (HI-50X, HI-50XA). The new switch (Figure 1) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the trnasmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers much higher Off Isolation with power off and better fault performance. Channel overvoltage protection is inherent since at least one of the three MOSFETs will turn off in the presence of overvoltage.

For the conditions shown in Figure 1 (power on; switch closed), gate voltage for the outer N-channel MOSFETs is +15V. Therefore, channel resistance in the left hand device will increase as the analog input increases from zero, since V_{GS} is approaching the threshold value (approximately 2V). Similarly, the P-channel resistance increases as the input increases in the negative direction, yielding an overall variation of "ON Resistance" as shown in Figure 2. This variation restricts the useable signal range somewhat, but provides a natural "shutoff" for inputs which approach or exceed the supply voltages. Of particular interest is the behavior with power off, in which R_{ON} remains high for all values of input. Table 1 shows the conditions of a 50XL switch for all modes of operation and values of input voltage.

A further advantage for the 50XL switch over earlier designs is its higher OFF Isolation: -72dB with power, and -56dB with power off ($V_{IN} = 3V_{rms}$ @ 500kHz). That is, switch feedthrough with the power off is less than 0.17%.

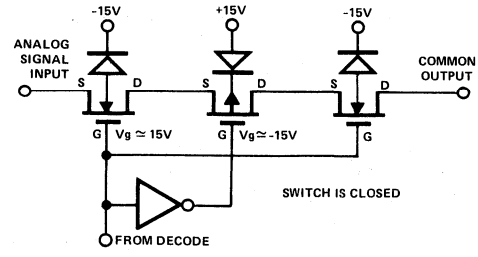


Figure 1. Switch Cell

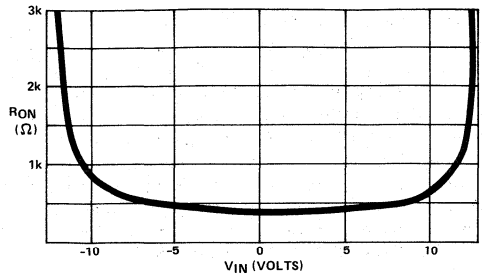


Figure 2. V_{IN} vs. R_{ON}

Table 1. 50XL Switch Behavior

MODE OF OPERATION	ANALOG INPUT, V_{IN}		
	NEGATIVE OVERVOLTAGE ($V_{IN} \leq -14V$)	NORMAL OPERATION ($-10V \leq V_{IN} \leq +10V$)	POSITIVE OVERVOLTAGE ($V_{IN} \geq +14V$)
Power On; Switch Closed	OXO	OOO	XOO
Power On; Switch Open	OXX	XXX	XXX*
Power Off	OXX	–	XXX*

(Switch MOSFETs: N-P-N, where X = OFF; O = ON)
* State of the P-channel MOSFET is indeterminate.

CONTROL SIGNALS

The Address inputs A_0, A_1, A_2, A_3 and Enable are latched into an internal buffer when $\overline{WR}$ goes from low to high. These digital inputs are DTL, TTL and CMOS compatible. Each latch output is level shifted into the decode section, which activates the appropriate channel, (if any). The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system reset line to assure that all channels are OFF following a turn-on of power. The reset ($\overline{RS}$) line may also be tied to the power supply with a resistor and capacitor to provide a delay from initial power-up. Refer to Figure 3.

The reset function overrides all others, just as $\overline{WR}$ (Write) overrides the address inputs (A_0 - A_3 and $\overline{EN}$ are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e., the latches are "transparent".

Members of the 50XL family are easily interfaced to a microprocessor system. The channel select lines may be tied directly to either the address or the data bus. No I/O interface device (PIA, PPI) is required since latches are provided on the HI-50XL chip. However, some additional hardware may be necessary for deriving the HI-50XL $\overline{WR}$ signal, depending on system requirements. Refer to Figure 4.

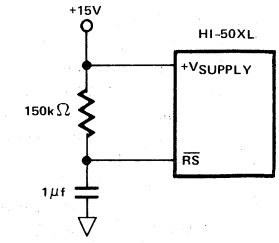


Figure 3. 50XL Switch Behavior

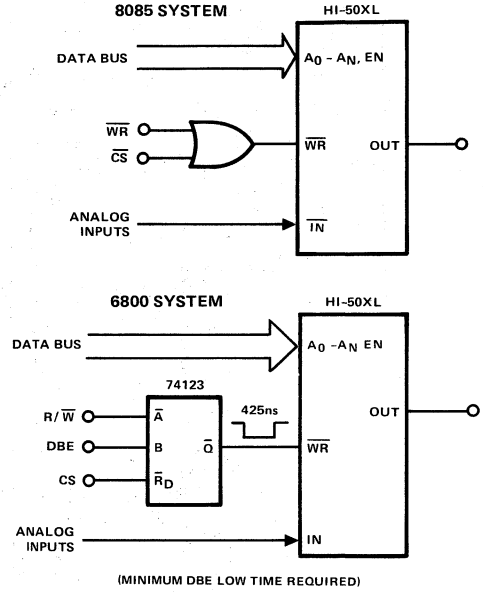


Figure 4. 50XL Control Requirements

THE 50XL-SYSTEM INTERFACE

There are perhaps eight basic ways to connect a 50XL multiplexer in a microprocessor system. Most of these are options common to the interface of any peripheral device, so the most appropriate method is usually indicated by the system hardware and its intended use.

To operate the 50XL, three functions must be provided - chip (device) selection, channel selection (A_0, A_1 . . . A_N, EN) and control ($\overline{WR}$, $\overline{RS}$). Channel selection is accomplished by a direct connection either to the data bus (simpler software) or to the address bus (higher clock speed allowable). For either case, a chip select is obtained in the usual way, using either an address bus decoder or the "bit flag" method, in which one address line is dedicated to the 50XL. Further, many systems will offer access to the 50XL through an option of either "memory mapping" or "I/O mapping", yielding eight different interface connections.

Four of these cases are illustrated in Figure 5, in which each HI-506L multiplexer is installed in the I/O space of an 8085 microprocessor. Channel selection is by the data bus (#1, #2) and the address bus (#3, #4). Device selection is provided by an address decoder (#1, #3) and by the dedicated address line "bit flags" (#2, #4).

For each multiplexer, external gates and control lines are arranged to write a 5 bit word (A_0, A_1, A_2, A_3, EN) to the address inputs, and latch it by a low-to-high transition at MUX's $\overline{WR}$ input. The 50XL requires a minimum 300ns for this WR pulse, and if necessary, a monostable multivibrator (one-shot) may be added to extend the pulse's duration. To clarify these system timing relationships, the parameters relevant to an 8085 I/O Write operation are shown in Figure 6, along with two selected waveforms from Figure 5 and the 50XL Write Pulse. As an alternative, however, the timing requirements may easily be met using a programmable peripheral interface device (PPI, PIA, or equivalent).

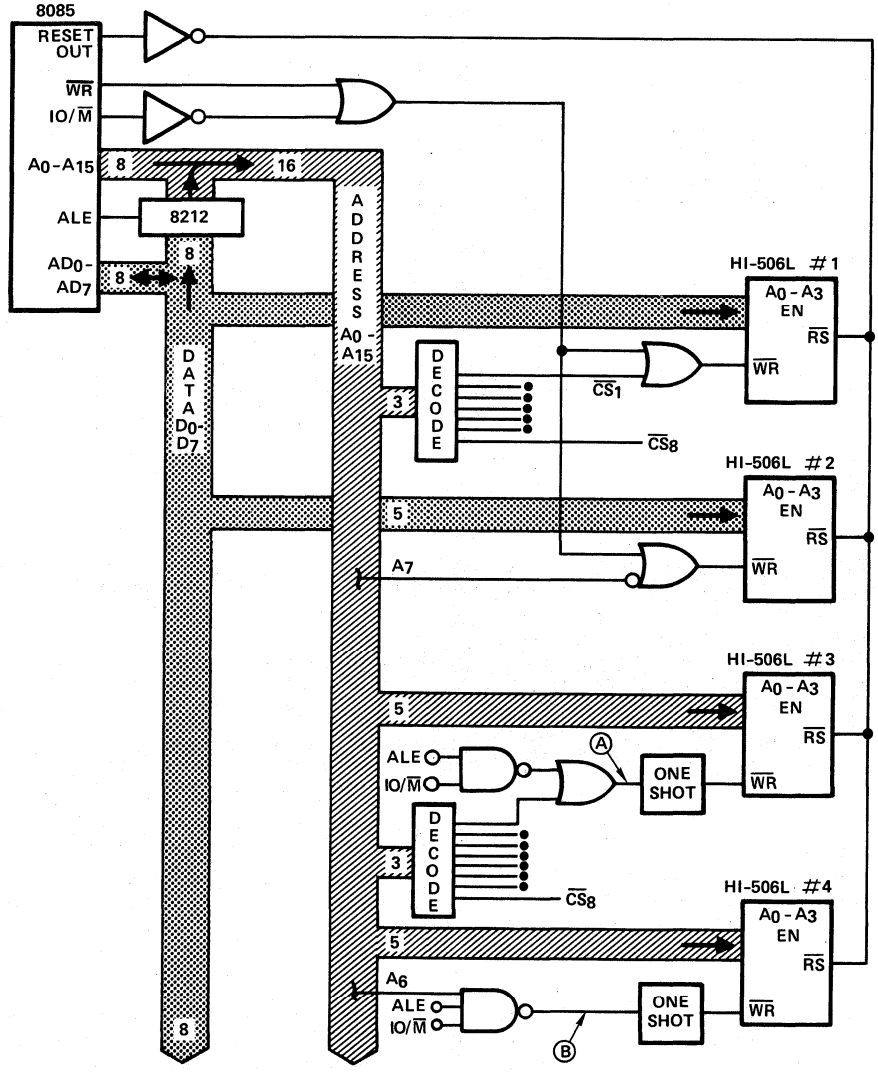


Figure 5. 50XL Interface Examples

SYSTEM APPLICATION EXAMPLE

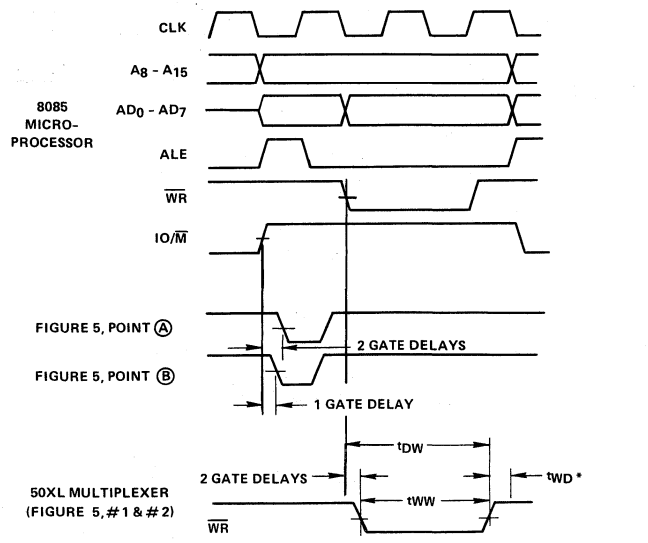
Figure 7 includes two separate data acquisition systems controlled by an 8085 microprocessor. In the upper system, 16 analog channels are multiplexed into a Sample/Hold - A/D Converter combination which provides sample rates as high as 2.7kHz per channel. In the lower system, two HI-506Ls are operated as a single 32 channel multiplexer, delivering the analog signal through a buffer amplifier directly to an A/D converter. Bandwidth of these 32 analog signals is limited since no Sample/Hold is used (for 12 bit accuracy, BW must not exceed 2 hertz). However, each channel may be digitized every 736 μs, for a 1.36kHz sample rate.

In each system of Figure 7, control of the HI-506L multiplexer is as shown in Figure 5, #2. That is, the latched address inputs are connected directly to the data bus for channel selection, and a single bit of the I/O address is used as a chip select. (Up to eight peripherals may be controlled in this manner). The multiplexer's $\overline{WR}$ input is derived by appropriate gating of this chip select with the 8085 $\overline{WR}$ and IO/$\overline{M}$ signals.

In the upper system a D-type flip-flop simultaneously initiates a conversion and switches the Sample/Hold to Hold. This is acceptable since the Hold mode settling is only 185ns, and at least 1μs will elapse before the converter's first bit decision. Similarly, the lower system uses a flip-flop to initiate conversions and another flip-flop to control the HI-200 switch, forming a 32 channel multiplexer.

The two multiplexers in the lower system are operated in parallel so two analog signals are always presented to the analog switch. Crosstalk in the switch is not a concern since only low BW signals are involved. As an alternative, one may eliminate the HI-200 switch and its flip-flop by connecting the MUX outputs together and using the ENable controls to enable one multiplexer at a time. However, output capacitances add together to increase the output time constant. Additional settling time must be allowed for the multiplexer, so the result is a lower channel rate than with the HI-200 switch arrangement.

PARAMETER	TYPICAL +25°C	MIN LIMITS FULL TEMP. RANGE	UNITS
t_{WW}, Write Pulse Width	155	300	ns
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	85	225	ns
t_{WD}, A, EN Data Valid After WRITE (Hold Time)	20	100	ns
t_{RS}, RESET Pulse Width (not shown)	250	400	ns



*TO MEET THE MINIMUM t_{WD} REQUIREMENT, 8085 CLK MUST NOT EXCEED 2MHz.

Figure 6. Timing Requirements.

Initiation of a Read operation by the processor toggles a flip-flop in each system, setting the converters to Read and (for the upper system) switching the Sample/Hold to Sample. Finally, each converter's STATUS output is inverted and tied directly to one of the processor's interrupt request terminals, with higher priority to the upper converter. The processor may execute instructions until a conversion is completed in either system - then it vectors to a Read routine, stores the data, and triggers another conversion. Each result will occupy two bytes of memory since a 12 bit word must be transmitted on an 8 bit data bus. The HI-574A accomplishes this by monitoring the A_0 address line with its A_0 control input, allowing the converter to route the two bytes into consecutive memory locations.

Machine language routines suitable for exercising the system of Figure 7 are listed in the following section. Also, detailed parametric limits for the HI-506L and HI-507L multiplexers are listed in Figure 8.

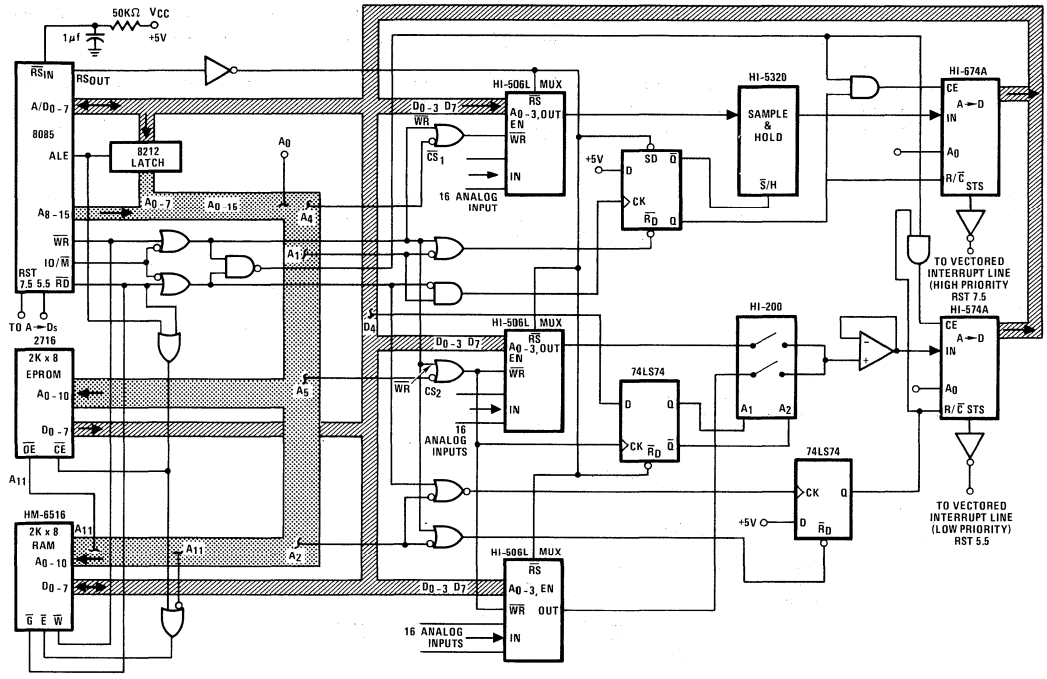
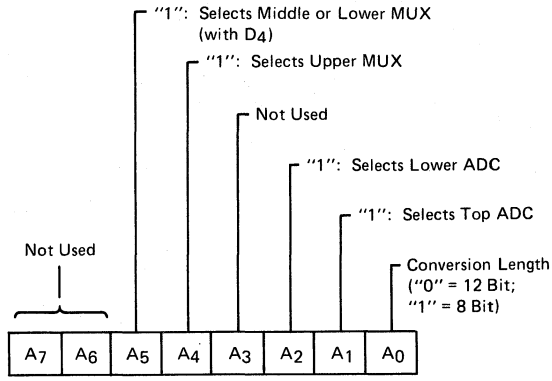
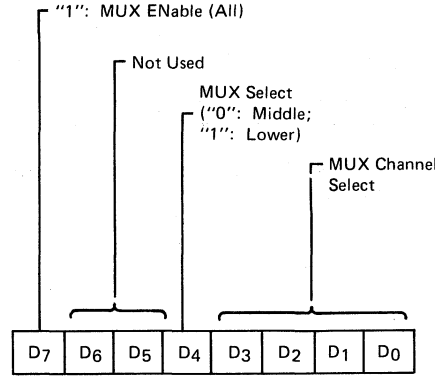


Figure 7. HI-50XL System Application.

SOFTWARE CONTROL

These brief assembly routines implement the basic operations required in Figure 7. Since hardware connections commit various lines of the address and data buses to specific jobs, control information may be conveyed to the system components by individual bit signals on these buses. The programmer simply writes an appropriate control word to the location of a given component. Control words are composed according to the bit information shown below:





OPERATIONS

1. Select Channel 5 of upper MUX:

X	X	0	1	0	0	0	0	= 10 HEX	
1	X	X	X	0	1	0	1		= 85 HEX

MVI	A, 85H	
OUT	10H	
		Move control word to Accumulator
		Write word to MUX

2. S/H to HOLD and start a conversion, upper converter:

X	X	X	X	X	X	1	0	= 02H	
X	X	X	X	X	X	X	X		= 00H

OUT	02H	
		Write word to Flip-flop

3. Read output of top converter, following an interrupt via 8085 RST7.5 input. (Converter output is 1101 0110 1001.):

Read 1st byte -

X	X	X	X	X	X	1	0	= 02H	
1	1	0	1	0	1	1	0		= D6H
							(8MSBs)		

Read 2nd byte -

X	X	X	X	X	X	1	1	= 03H	
1	0	0	1	0	0	0	0		= 90H
							(4LSBs)		

Interrupt RST7.5 causes a JUMP to the following service routine:

IN	02H	Read first byte
MOV	D, A	Move data to D register pair
IN	03H	Read second byte
MOV	E, A	Move data to E register pair
MVI	A, 1AH	Move control word to Accumulator
SIM		Reset Interrupt
(Store data instructions)		
RET		Return

4. Select Channel 14 of lower MUX:

X	X	1	0	X	X	X	X

= 20H

1	X	X	1	1	1	1	0

= 9EH

Note: MUX channels are numbered 0 to 15.

```
MV1     A, 9EH      Move control word to Accumulator
OUT     20H         Write word to MUX
```

5. Initiate a conversion in lower converter:

X	X	X	X	X	1	0	0

= 04H

X	X	X	X	X	X	X	X

= 00H

6. Read output of lower converter following an interrupt via 8085 RST5.5 input:

This is accomplished with a routine identical to that in Operation // 3, except location 04H is used instead of 02H, and 05H instead of 03H.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note1)

Supply Voltage Between Pins 1 and 27	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$:			
V supply (+)	+4V	HI-506L/507L-2	−55°C to 125°C
V supply (−)	−4V	HI-506L/507L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

PARAMETER	HI-506L/507L-2 −55°C to +125°C TEMP	MIN	TYP	MAX	HI-506L/507L-5 0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note 2)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
$\triangle R_{ON}$, Change In R_{ON} (Note 3) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		5	50		5	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-506L	Full		8	200		8	200	nA
HI-507L	Full		4	100		4	100	nA
$I_{D(On)}$, ON Channel leakage current	+25°C		5	10		5	10	nA
HI-506L	Full		10	200		10	200	nA
HI-507L	Full		5	100		5	100	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 4)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-	+25°C		5			5		nA
voltage applied (Note 4)	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current (Note 5)	Full		10	40		10	40	μA
I_{AL}, Input Low Current (Note 5)	Full		40	200		40	200	μA
DYNAMIC SWITCHING CHARACTERISTICS (Note 6)								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	μS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		.025	0.1		μS
t_{ON}, (EN), Enable Delay (ON)	+25°C		0.5	1.0		0.5	1.0	μS
t_{OFF}, (EN), Enable	+25°C		0.5	1.0		0.5	1.0	μS
Delay (OFF)								
Settling Time (±0.1%)	+25°C		1.0			1.0		μS
(±0.01%)	+25°C		1.75			1.75		μS
OFF Isolation (Note 7)	+25°C	50	68		50	68		dB
OFF Isolation POWER OFF (Note 8)	+25°C		56			56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-506L	+25°C		50			50		pF
HI-507L	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 9)	Full		60	100		60	100	mW
I +, Current Pin 1 (Note 9)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 27 (Note 9)	Full		0.3	0.6		0.3	0.6	mA

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, 1 out = -100μa
3. $\Delta R_{ON} = \frac{R_{ON}(Max) - R_{ON}(Min)}{R_{ON}(Avg.)}$, V_{IN} = ± 10V
4. Analog Overvoltage = ± 25V
5. I_{AH} and I_{AL} tested at 2.4V and 0.4 V respectively
6. For measurements in this section, input logic levels are 3.0V (High) and 0V (Low).
7. V_{EN} = 0.8V, R_L = 1KΩ, C_L = 15pF, V_S = 7Vrms, f = 500kHz
Off isolation = 20 log $\frac{|V_D|}{|V_S|}$
8. V+ , V- = 0V, R_L = 1KΩ .
C_L = 50pF, V_S = 3Vrms, f = 500 kHz.
9. See complete data sheet for high toggle frequency applications.

Figure 8.

HARRIS

APPLICATION NOTE 607

DELTA MODULATION FOR VOICE TRANSMISSION

BY DON JONES

INTRODUCTION TO DELTAMOD

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

One can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, therefore an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the height of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

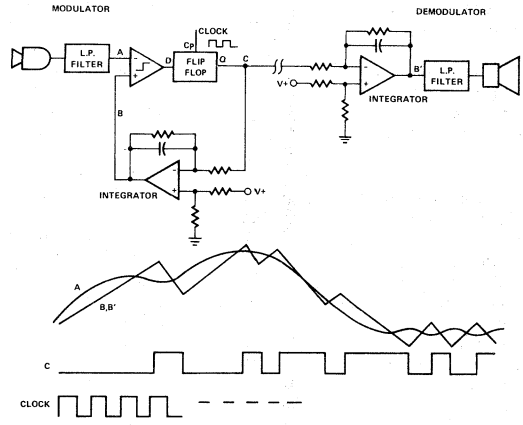
Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

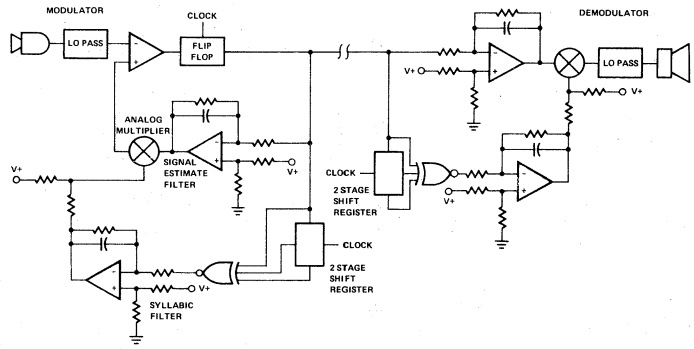
A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound

is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.





THE DIGITAL CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55564 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

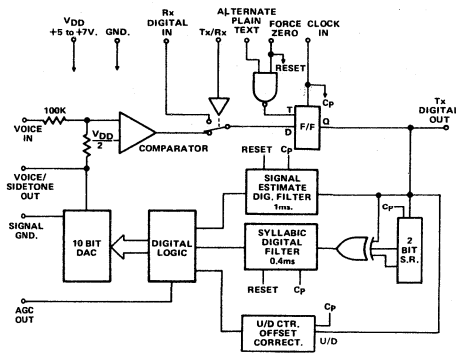


Figure 3 – HC-55564 CVSD Functional Diagram

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

APPLICATIONS OF DELTA MODULATION

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

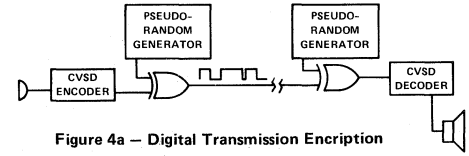


Figure 4a – Digital Transmission Encription

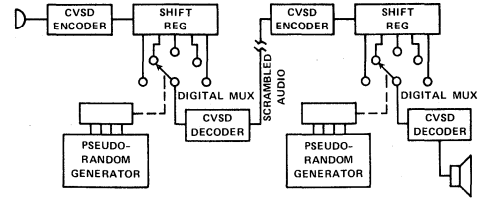


Figure 4b – Voice Transmission Scrambling

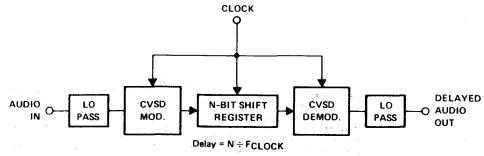


Figure 5 – Audio Delay Line

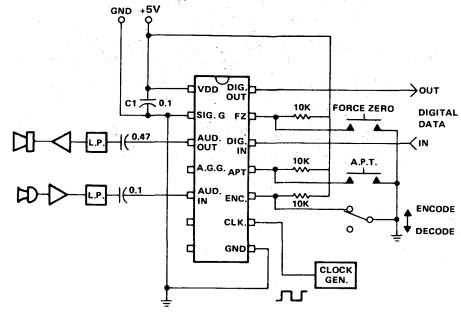


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55564. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The PCM Filter shown in the data sheet lends itself well as a cost-effective input/output filter to the CVSD.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.2V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 10 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.

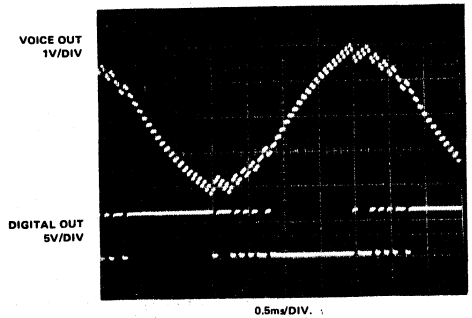


Figure 7 – CVSD Large Signal Sine Wave Reconstruction

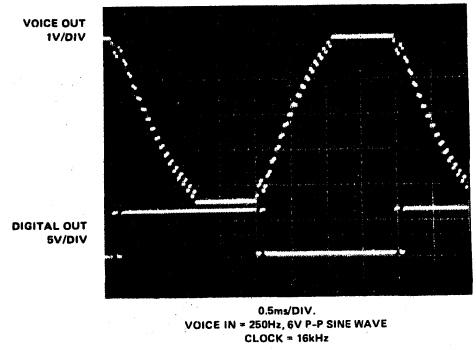


Figure 8 – CVSD Large Signal, Low Frequency Clipped Waveform

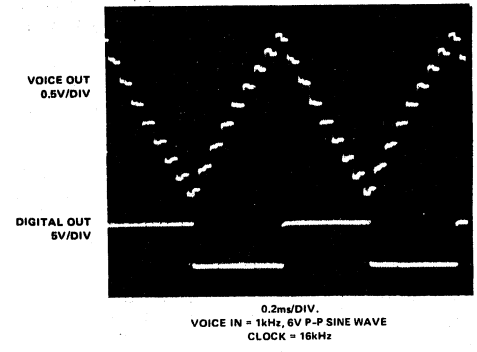


Figure 9 – CVSD Large Signal, High Frequency Slew Limiting

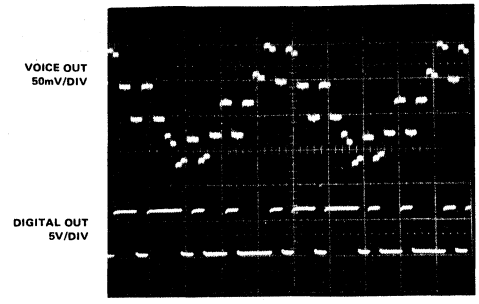


Figure 10 – CVSD Small Signal Sine Wave Reconstruction

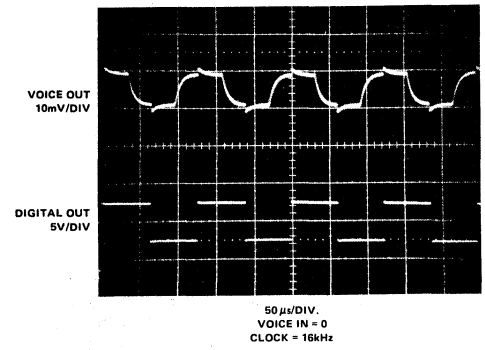


Figure 11 – CVSD Zero Signal Idle Pattern

Custom Integrated Circuits Division

11

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Custom Linear	11-4
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Custom Integrated Circuits Division

Harris. A reputation in hi-rel custom circuits no one else can match. An emerging force in gate arrays and standard cells. A leader with all the options.

Fifteen years of pace-setting experience from programs like Trident and Peacekeeper to commercial satellites and heart pacemakers make Harris your logical choice for quality, speed and performance in custom/semicustom ICs. From commercial screening all the way to Class S equivalents. And beyond.

If fast turnaround to market introduction or system prove-out in low volumes is your need, look to Harris gate arrays. Minimum initial investment and development time make them the logical choice. And upgrading to standard cell or full custom is easy.

Quick turnaround combined with ease of design and medium-to-large volume cost efficiencies make Harris standard cells your best buy.

However, for highest performance, lowest unit price, maximum reliability and smallest silicon area in high-volume requirements, Harris full custom ICs are the preferred option.

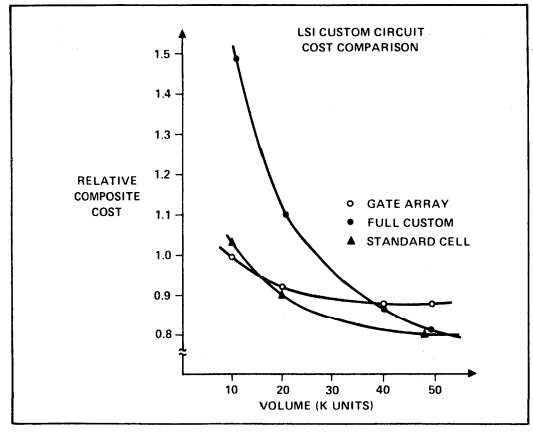
Your choices don't stop there.

Choose the technology. Analog or Digital. Bipolar or CMOS. Separately, or combined onto a single chip. Let us apply our vast experience to provide you with the right product, in the right package, at the right price.

You can even choose your level of design and layout participation to make best use of your in-house capabilities. Use our engineers or use your own. Full capability or silicon foundry, we offer all the support you need.

And if you have radiation hardness requirements look no further. Harris is the leading supplier of radiation hardened circuits in the military marketplace.

No matter which option you take, opt for the experts at Harris. The logical choice.



For more information or data sheets, mail your request to: Harris Custom Integrated Circuits Division, P. O. Box 883, Mail Stop 53/107, Melbourne, Florida 32902.

Or Call: (305) 729-5681

Test Product Flow

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
METHOD 5004, CLASS B
100% SCREENING PROCEDURE

	SCREEN	METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Product Assurance

Harris has served the special HI-Reliability interests of aerospace and electronics manufacturers since 1982 as a supplier of custom, high-performance IC's. Successful deliveries for major strategic weapons electronics, military aircraft flight controls, classified around and air communication systems, tactical weapons guidance and arming, communication satellites, nuclear plant instrumentations, and heart pacemakers has given CICD a unique capability to satisfy the most demanding requirements.

CICD's Product Assurance Department reports directly to the General Manager—assuring continuous management awareness and concern for customer satisfaction. Internal operating procedures have been designed to conform with published Military Standards as a minimum. . .with control systems in place to permit customized manufacturing to individual customer requirements. Outstanding on-site analytical facilities are utilized to support design and problem-solving for timely deliveries. CICD's Product Assurance personnel are dedicated; having many years at working with some of the most demanding quality and reliability professionals in the world. . . . our customers and Department of Defense specialists.

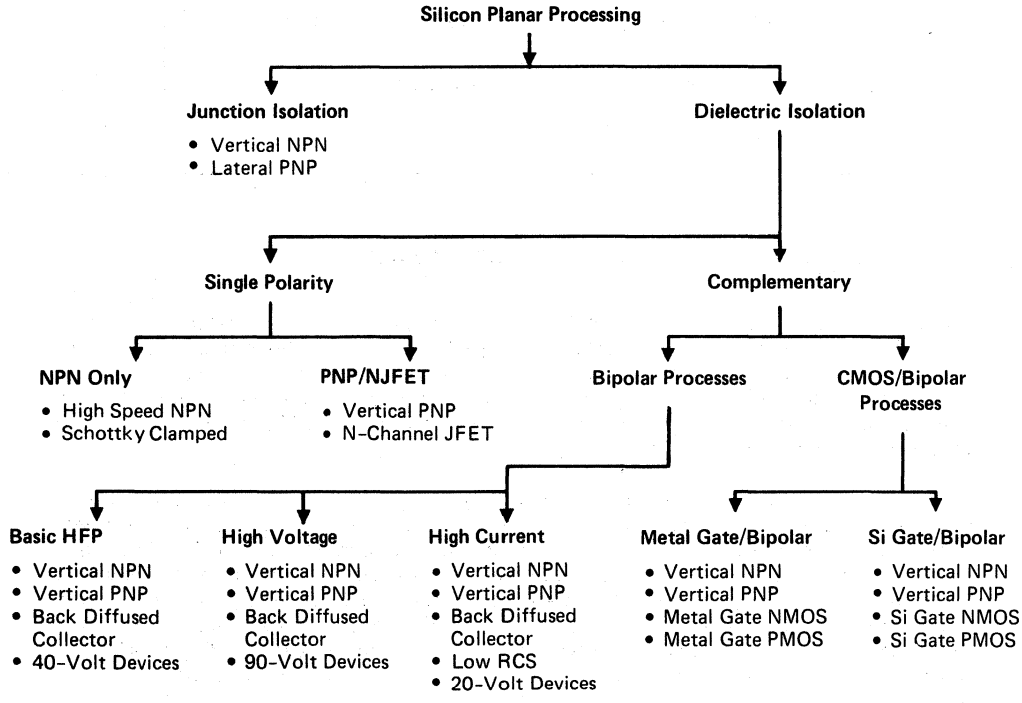
This is the background for assurance of quality and reliability for CICD's Data Sheet Products; circuit types of specialized design and processing which can satisfy many high-performance requirements. CICD is a recognized leader in custom radiation-hard designs. The Data Sheet Product line now makes this hardness available in some widely useable circuit types.

Custom Linear

Linear Engineering Technology Options

- Dielectrically isolated Bipolar
- High performance
  - High voltage capability
  - Radiation tolerant
- Combination CMOS/Bipolar
  - Multiplexer applications
  - High voltage CMOS capability
  - Metal gate or SI gate
- Junction Isolation
  - Low cost technology
- Precision Resistor Technology
  - High sheet resistance implanted Boron
  - Thin Film NiCr—Laser trimmed
- JFET technology
  - Compatible N- and P-Channel devices

Linear Technology Matrix



Linear Technology Comparison

	Process	h_{fe} NPN	h_{fe} PNP	F_t MHz NPN	F_t MHz PNP	BV_{eeo} (V) NPN	BV_{eeo} (V) PNP
Dielectric Isolation	J. I.	150	100	300	2	40	40
	Switching NPN	50	–	500		7.5	–
	PNP-NJFET	–	100		400	(1)	35
	High Frequency	200	100	600	300	40	40
	High Current	200	100	850	500	20	20
	High Voltage	225	50	200	25	100	90
	CMOS/Bipolar	200	100	600	300	35	35

(1) V_P = 2-5V, BV_{DSS} = 30V

Why Choose DI?

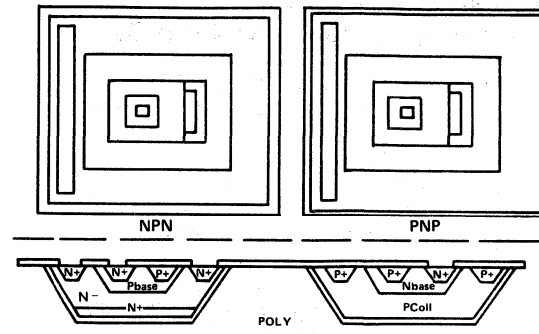
- Performance Advantages
  - High frequency performance
  - High voltage
  - Functional flexibility
  - Radiation resistant
- Technical Basis
  - High performance complementary NPN/PNP's
  - Reduced capacitances
  - Compatible CMOS devices
  - No parasitic substrate effects:
    - SCR's, leakage currents,
    - Device coupling effects

Typical Applications

- High frequency amplifiers
- Radiation hardened amplifiers
- Comparators
- Sample and Holds
- Data conversion
- Analog switches

DI Process Technology

- <1-0-0>Silicon process
- All active devices fully isolated using
- 2 -micron oxide layer
- 11 mask levels
- Vertical NPN
- Vertical PNP
- MOS capacitors
- Diffused resistors
- Process options include full metal gate CMOS, precision thin-film resistors, both polarities of high implanted JFET devices and sheet implanted resistors



BASIC DI CROSS SECTION

DI Process Technology
Typical Device Parameters

NPN transistor	β = 200 BVceo = 35V FT = 600MHz
PNP transistor	β = 100 BVceo = 35V FT = 300MHz
N-channel MOS	VT = 1.0-2.5V BV_{dss} = 40V
P-Channel MOS	VT = 1.0-2.5 BV_{dss} = 40V
N-channel JFET	VP = 1-2V BV_{dss} = 20V
P-channel JFET	VP = 1-2V BV_{dss} = 40V

Advanced Hardened Data Acquisition

Radiation Hardened (Strategic Levels)	Comm. Equiv.
• 12-Bit A/D chip set	
– 12 Bit D/A	HI-562
– 10V precision reference	HI-1610
– Precision voltage comparator	CMP-05
– SAR logic chip	Gate Array
• Voltage/current regulator	–
• 6-bit flash converter	TDC 1014J

All parts use radiation hardened DI processing

Radiation Hardened Data Acquisition A/D Chip Set

- 12-Bit D/A converter (HS-3504)
  - 12-bit, guaranteed monotonic by segmentation
  - 1/2 LSB Accuracy
  - TTL inputs
  - Voltage or current mode
  - 500ns settling time to ± 1/2LSB
  - Laser trimmed
- Precision voltage reference (HS-3506)
  - 10-Volt output
  - 10mA output current
  - 0.002%/V line regulation
  - 0.5mV/mA load regulation
  - ± 10ppm/°C temperature coefficient
  - Laser trimmed
- High-speed comparator (HS-3510)
  - On-Chip input clamp
  - 50 μV offset voltage
  - 30,000 V/V gain
  - 70ns response time
  - Laser trimmed

JI Process Technology Typical Device Parameters

NPN transistor	β = 150 BV_{ceo} = 40V FT = 300MHz
PNP, Lateral	β = 70 (10 μA) β = 10 (500 μA) BV_{ceo} = 40V FT = 2MHz
PNP, substrate	β = 50 BV_{ceo} = 40V FT = 20MHz

Projected Linear Developments

Radiation Hardened	Comm. Equiv.
• Dual Op Amp	HA-2730
• Sample and Hold	HA-2420
• 8-Channel JFET MUX	LM-11508
• 4-Channel sense amp	—
• Switching regulator	SG 1524
• Laser Gyro photo preamp	—

Special Functions

- Switched capacitor arrays
- Low noise amplifiers

CICD Product Index

		PAGE
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HS-4602RH	Radiation Resistant High Performance Quad Op Amp	11-14
HS-3516RH	High Slew Rate, Wideband, Radiation Resistant, Op Amp	11-21
HS-3530RH	Low Power Radiation Resistant Programmable Op Amp	11-24
HS-1840RH	Radiation Resistant 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection	11-28
HS-508ARH	Radiation Resistant 8 Channel CMOS Analog Multiplexer with Overvoltage Protection	11-32

HS-3546RH

Radiation Resistant High Performance Operational Amplifier

Features

- LOW OFFSET VOLTAGE — 0.3mV
- HIGH SLEW RATE — ±4V/μs
- WIDE BANDWIDTH — 8MHz
- LOW DRIFT — 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) — 4.2μs
- LOW POWER CONSUMPTION — 35mW
- SUPPLY RANGE — ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADS (Si)

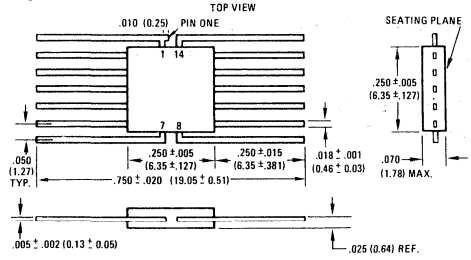
Description

The HS-3546RH is a radiation resistant, high performance dielectrically isolated monolithic operational amplifier with superior specifications. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

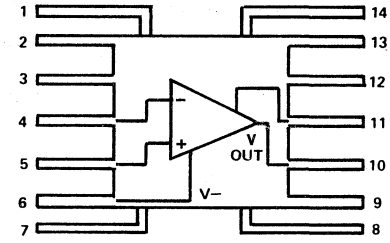
A wide range of applications can be achieved by using the features made available by the HS-3546RH. With wide bandwidth (8MHz), low power (35mW) and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/√Hz) and excellent full power bandwidth (60 KHz). The HS-3546RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-3546RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 Pin Ceramic Flatpack package and is guaranteed operational from -55°C to +125°C.

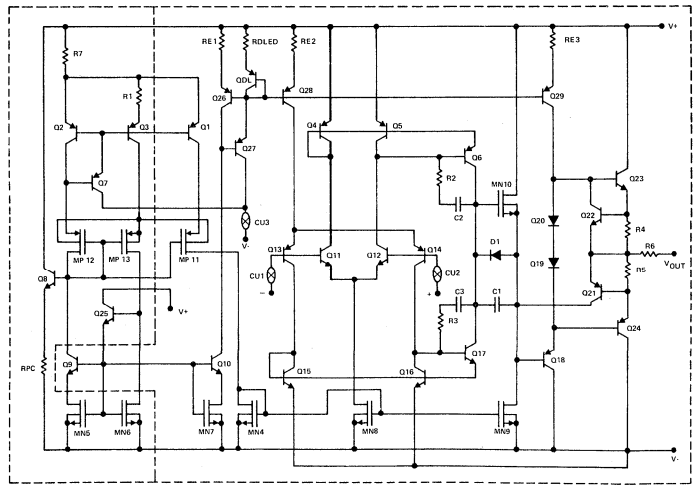
Package



Pinout



Schematic



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±7V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration (Note 3)	Indefinite
Power Dissipation (Note 4)	880mW
Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		µV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	50K	150K		V/V
* Common Mode Rejection Ratio (Note 8)	Full	86			dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 6)	Full	±18	±25		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/µs
Settling Time (Note 9)			4.2		µs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 8)	Full	86			dB

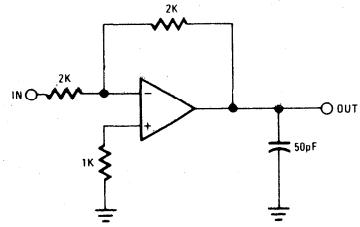
*100% tested

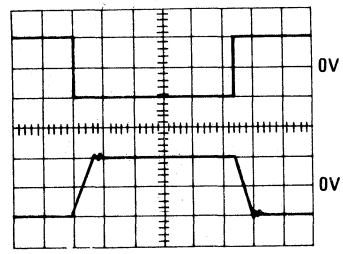
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Output current is measured with V_{OUT} = ±5 volts.
7. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
8. ΔV = ±5.0 volts.
9. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

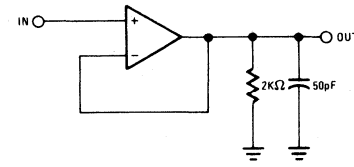
Test Circuits

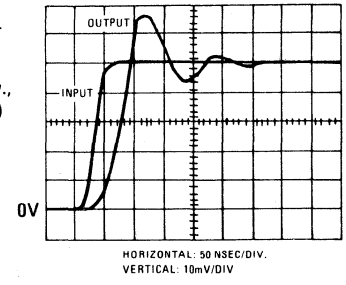
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



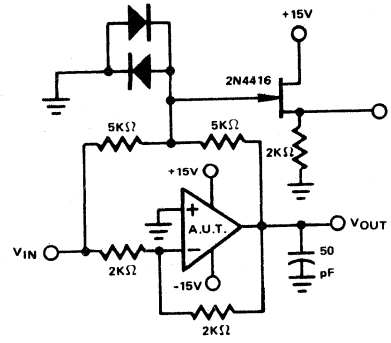


SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)





SETTLING TIME CIRCUIT

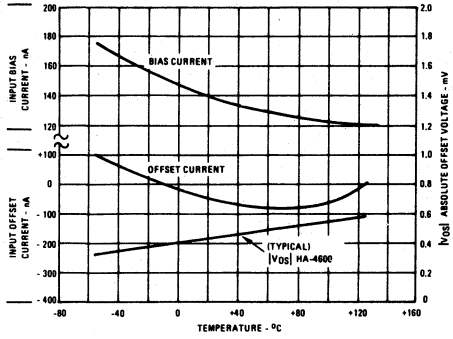


- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

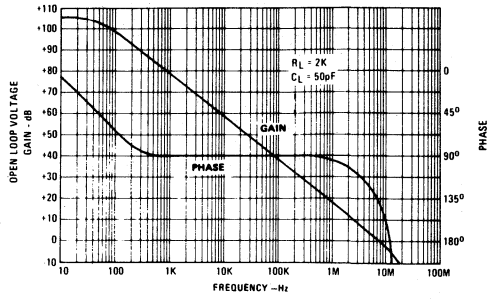
Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

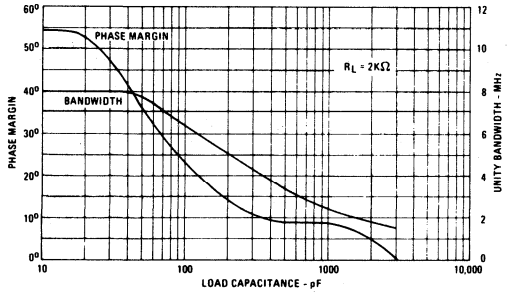
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



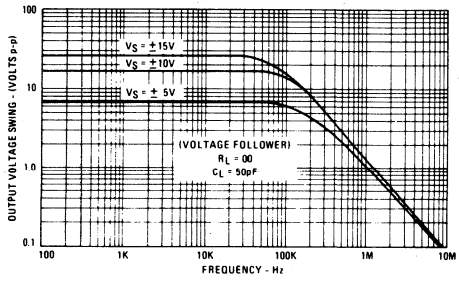
OPEN LOOP FREQUENCY RESPONSE



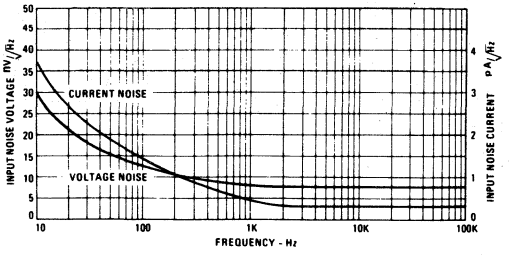
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE

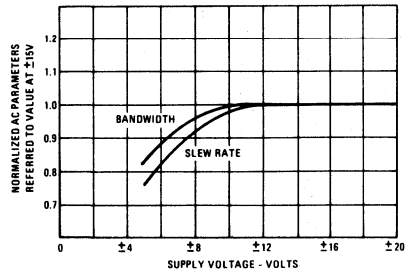


INPUT NOISE VS. FREQUENCY

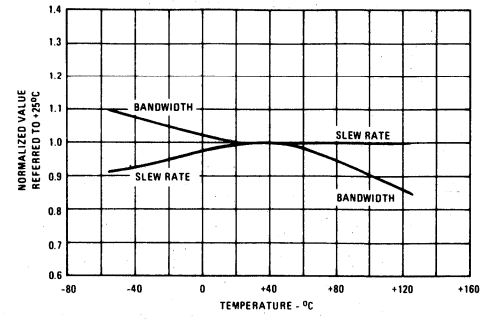


Performance Curves (continued)

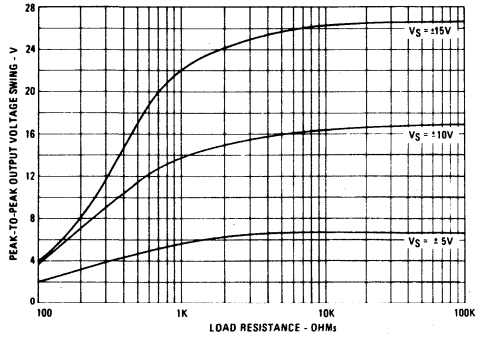
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



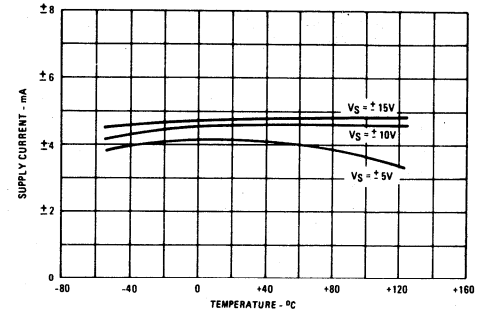
NORMALIZED AC PARAMETERS VS. TEMPERATURE



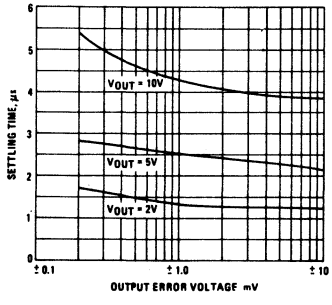
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



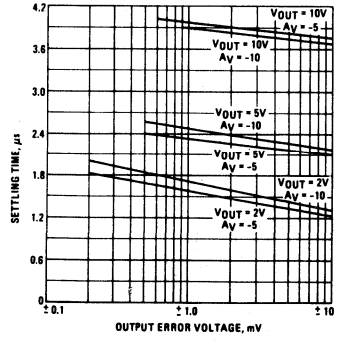
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



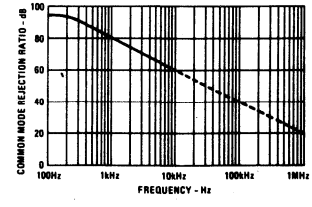
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



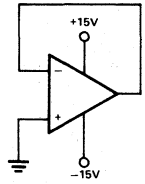
COMMON MODE REJECTION RATIO VS. FREQUENCY



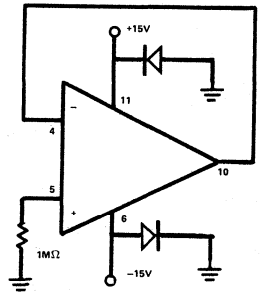
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Irradiation Circuit



Burn-in Circuit



NOTES:
T_A = +125°C
D = IN4002 OR EQUIVALENT

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq$ 50K, $V_{IO} \leq$ ±2.5mV and $I_{BIAS} \leq$ 1.0 μA at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1 x 10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1 x 10^4 and 1 x 10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

HS-4602RH

Radiation Resistant High Performance Quad Operational Amplifier

Features

- LOW OFFSET VOLTAGE — 0.3mV
- HIGH SLEW RATE — ±4V/μs
- WIDE BANDWIDTH — 8MHz
- LOW DRIFT — 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) — 4.2μs
- LOW POWER CONSUMPTION — 35mW/AMP
- SUPPLY RANGE — ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADS (Si)

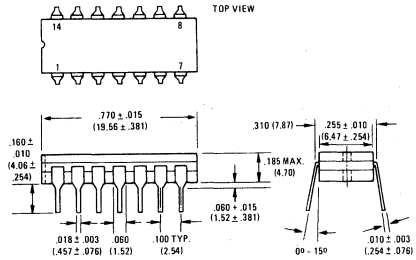
Description

The HS-4602RH is a radiation resistant, high performance dielectrically isolated monolithic quad operational amplifier with superior specifications not previously available in a quad amplifier. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

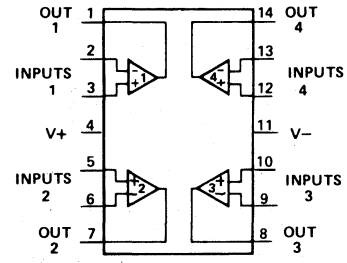
A wide range of applications can be achieved by using the features made available by the HS-4602RH. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power band-width (60KHz). The HS-4602RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2μs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-4602RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

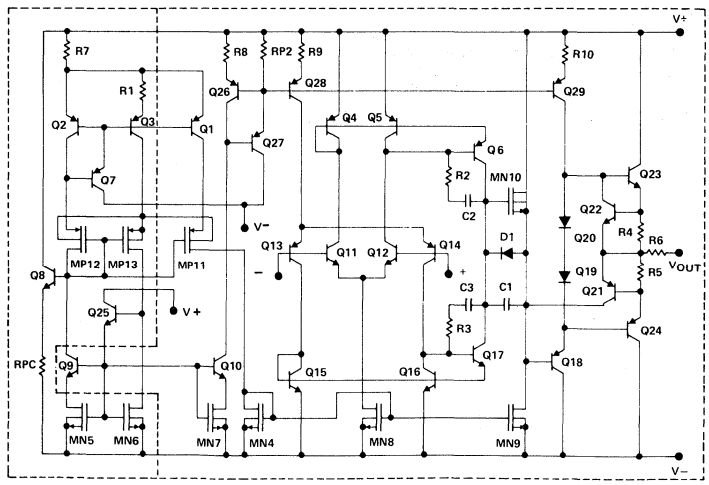
Package



Pinout



Schematic



(ONE FOURTH ONLY HS-4602-RH)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$
Input Voltage (Note 2)	±15.0V	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Output Short Circuit Duration (Note 3)	Indefinite		

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		µV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	50K	150K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			dB
Channel Separation (Note 6)	+25°C		-108		dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 7)	Full	±10	±15		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/µs
Settling Time (Note 10)			4.2		µs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			dB

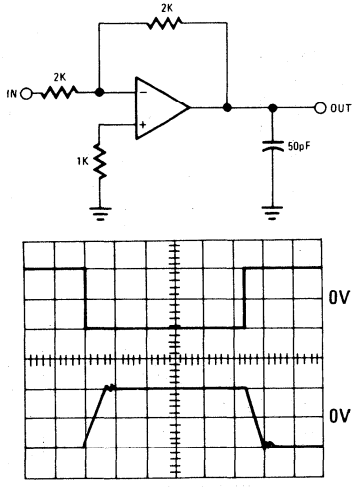
*100% tested

NOTES:

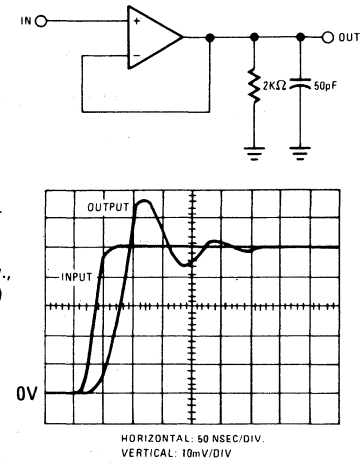
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

Test Circuits

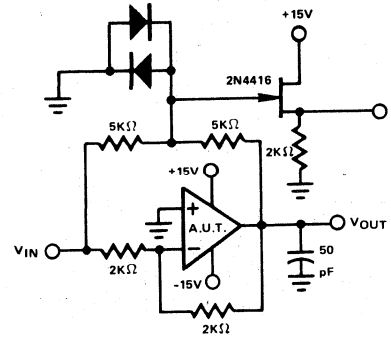
LARGE SIGNAL RESPONSE CIRCUIT
(Volts: 5V/Div., Time: 5μs/Div.)



SMALL SIGNAL RESPONSE CIRCUIT
(Volts: 10mV/Div., Time: 50ns/Div.)



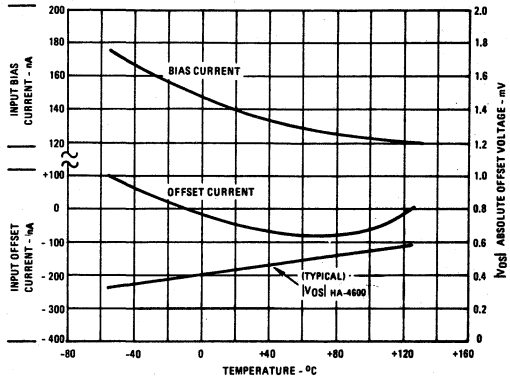
SETTLING TIME CIRCUIT



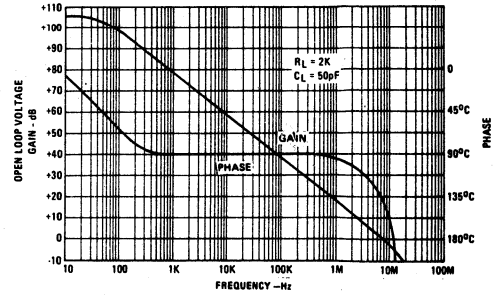
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

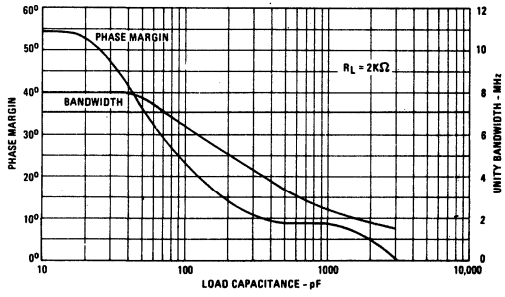
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



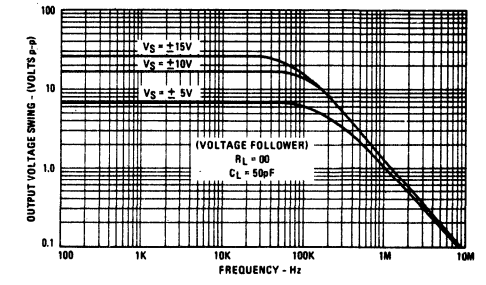
OPEN LOOP FREQUENCY RESPONSE



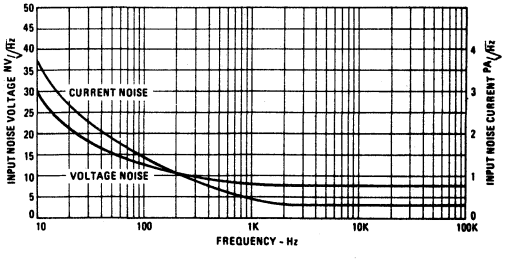
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



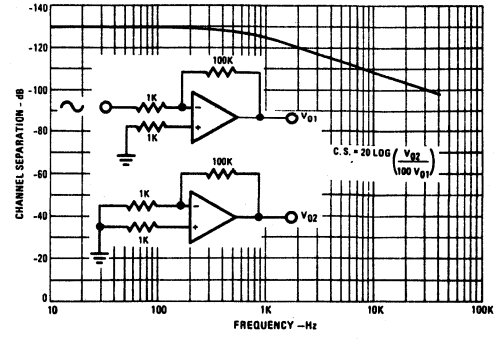
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



INPUT NOISE VS. FREQUENCY

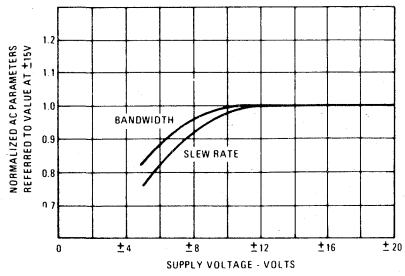


CHANNEL SEPARATION VS. FREQUENCY

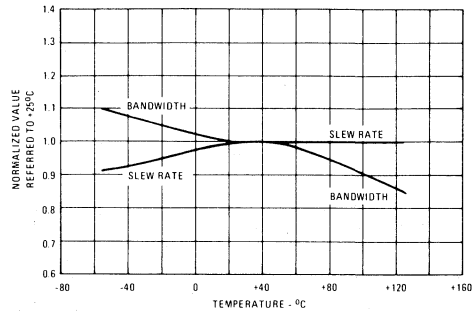


Performance Curves (continued)

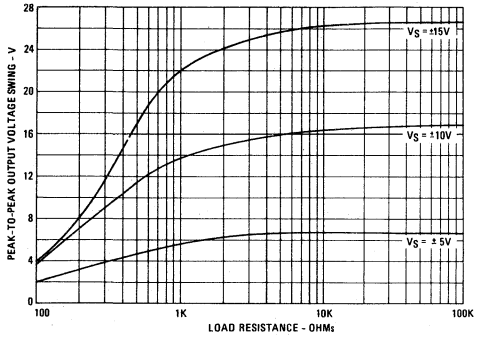
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



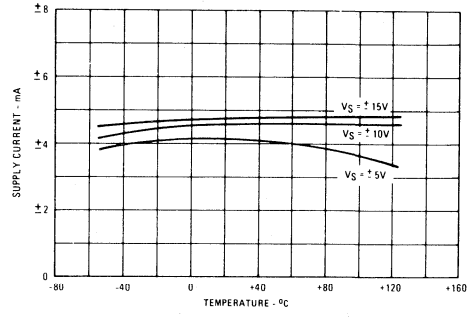
NORMALIZED AC PARAMETERS VS. TEMPERATURE



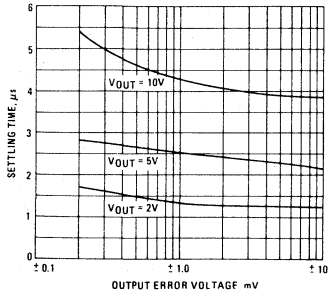
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



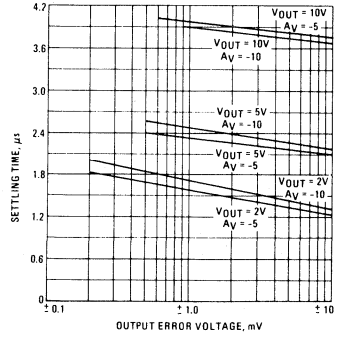
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



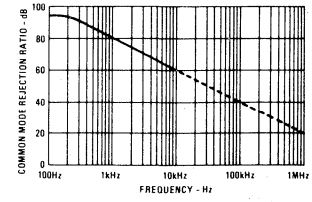
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



COMMON MODE REJECTION RATIO VS. FREQUENCY



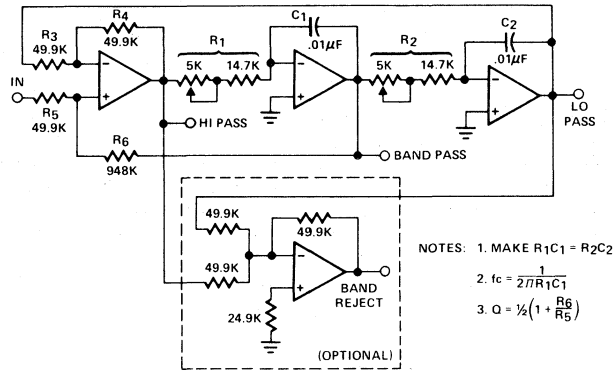
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Applications

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

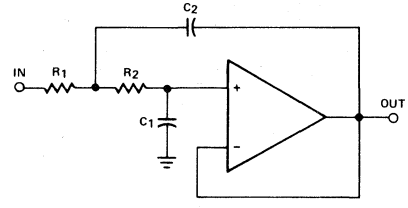
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$).

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

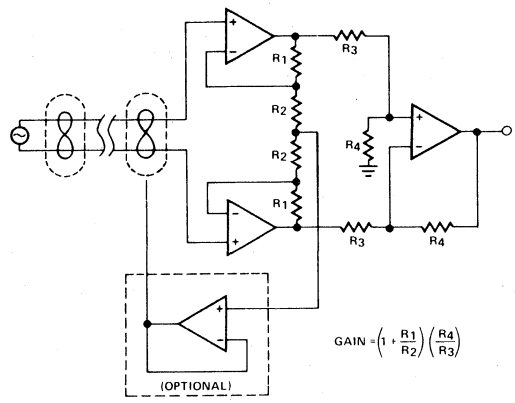
The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HS-4602RH is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

Applications (continued)

INSTRUMENTATION AMPLIFIER

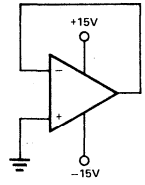


Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HS-4602RH is ideally suited for this application, delivering superior input and speed characteristics.

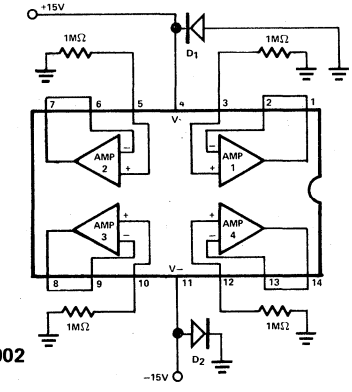
The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

Irradiation Circuit



(1/4 OF HS-4602RH DEPICTED)

Burn-in Circuit



NOTES:
T_A = +125°C
D_1, D_2 = IN4002

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of A_{VOL} ≥ 50K, V_{IO} ≤ ±2.5mV and I_{BIAS} ≤ 1.0 μA at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1 x 10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1 x 10^4 and 1 x 10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

HS-3516RH

High Slew Rate, Wideband, Radiation Resistant, Operational Amplifier

Features

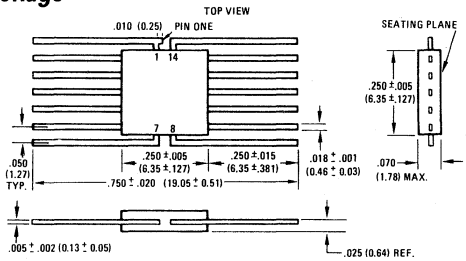
- HIGH SLEW RATE . . . . . >±22V/µs
- FAST SETTLING TIME 450ns
- WIDE POWER BANDWIDTH. 12MHz
- LOW OFFSET VOLTAGE. . . . . ±5mV
- LOW POWER SUPPLY CURRENT 6.5mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) $5 \times 10^{12} n/cm^2$ ($E \geq 10KeV$)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADs Si/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADs Si

Description

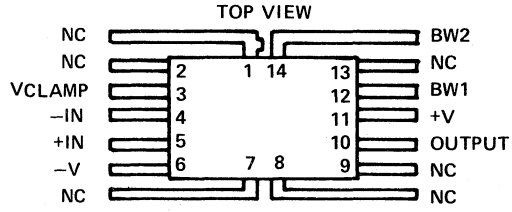
The HS-3516RH is a monolithic, high slew rate, wideband, radiation resistant, operational amplifier. It provides a bandwidth (unity gain stable) of greater than 10MHz and a slew rate in excess of 22V/µsec. Optional frequency compensation adjustment is provided. The HS-3516RH has an internal unity gain frequency compensation capacitor which is internally connected. A clamp node feature enables the user to clamp the output voltage via pin 3 which can source or sink up to 3mA for high frequency clamped switching purposes.

This device is designed to operate from −55°C to +125°C and in strategic-level radiation environments.

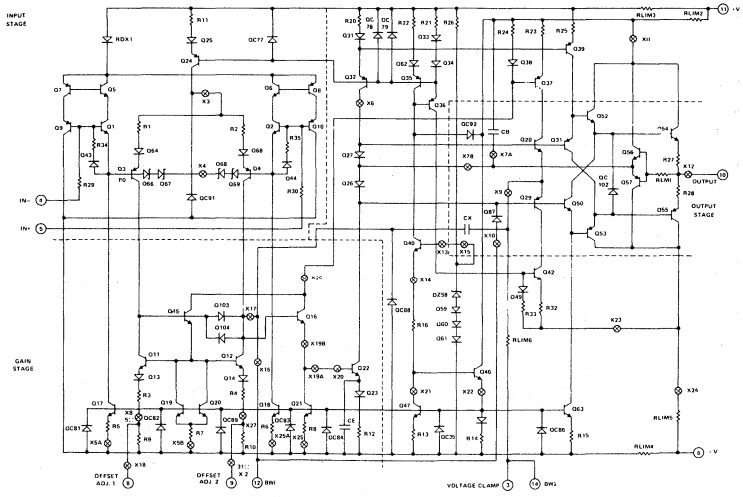
Package



Pinout



Schematic



11

CICD

ABSOLUTE MAXIMUM RATINGS

Voltage Between +V and −V terminals	40V	Internal Power Dissipation	625mW
Differential Input Voltage	±15V	Storage Temperature Range	−65°C to +175°C
Output Short Circuit Duration	Indefinite	Operating Temperature Range	−55°C to +125°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS +V = 15V, −V = −15V, T_A = −55°C to +125°C

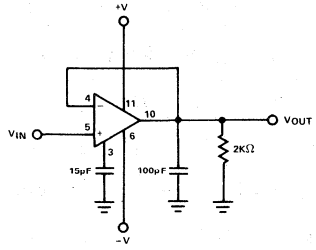
PARAMETER	TEMP	MIN	TYP	MAX	UNITS
Offset Voltage	25°C		1	3	mV
	125°C		2	5	mV
	−55°C		3	6	mV
Input Bias Current	25°C		35	100	nA
	125°C		50	100	nA
	−55°C			200	nA
Input Offset Current	25°C		30	100	nA
	125°C			150	nA
	−55°C			250	nA
Input Resistance	25°C		>100		MΩ
Large Signal Voltage Gain [1]	25°C	90			dB
	Full	90			dB
Common Mode Rejection Ratio [2]	25°C	80	115		dB
	Full	80	90		dB
Supply Current	25°C		5.0	6.5	mA
	125°C			6.5	mA
	−55°C			8.7	mA
Power Supply Rejection Ratio [3]	25°C	80			dB
	Full	80			dB
Output Voltage Swing	25°C	+12.5	+13.0		V
		−11.0	−12.0		V
	125°C	+12.5	+13.0		V
		−11.0	−12.0		V
	−55°C	+12.0			V
		−11.0			V
Output Short Circuit Current	25°C		27	45	mA
	125°C			45	mA
	−55°C			60	mA
Gain Bandwidth Product	25°C		12.0		MHz
	Full		10.0		MHz
Slew Rate [3, 5]	25°C	22	25		V/µs
Rise Time [4]	25°C		30	35	ns
Overshoot [4]	25°C		15	35	%
Overdrive Recovery Time	25°C		2	5	µs
Settling Time [4]	25°C		180	450	ns
	Full			450	ns
Output Clamp Voltage	25°C			0.4	V
Input Clamp (+) Icn− Current (pin 3)	25°C	−1.0		−3.3	mA
	125°C	−1.0		−3.3	mA
	−55°C	−0.8		−3.5	mA
Input Clamp (−) Icn+ Current (pin 3)	25°C	+0.5		+3.0	mA
	125°C	+0.5		+3.0	mA
	−55°C	+0.3		+3.2	mA

NOTES:

1. V_O = ±10V, R_L = 2K
2. V_{cm} = ±10V, R_L = 2K
3. ΔV = ±5.0V
4. A_V = +1, V_{IN} = 1V, R_L = 2K, C_L = 100pf
5. C_{BW} = 0, V_O = ±10V, R_L = 2K, C_L = 100pf

Test Circuits

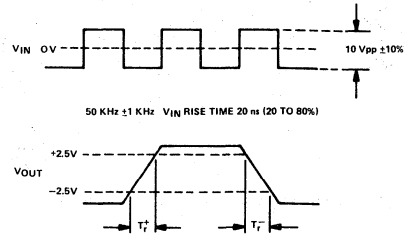
SLEW RATE CIRCUIT



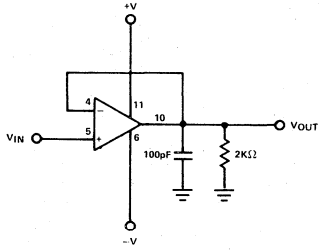
1. SLEW RATE = $\frac{5}{T_r^+ (\mu s)}$ V/μs

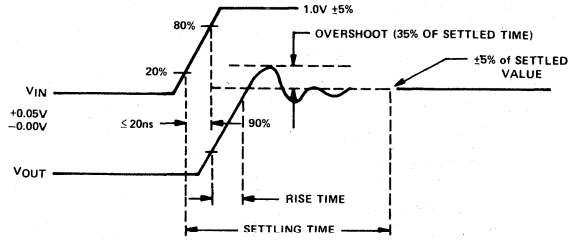
   OR — $\frac{5}{T_r^- (\mu s)}$ V/μs

2. INPUT BIAS CURRENT OF NON-INVERTING INPUT MAY INCREASE IF V_{IN} APPLIED BEFORE + V AND −V.

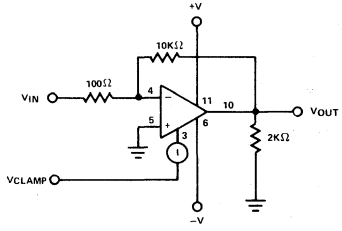


RISE TIME/SETTLING TIME CIRCUIT





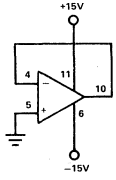
VOLTAGE CLAMP CIRCUIT



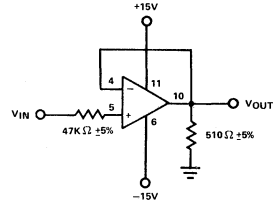
1. V_{IN} = +1.0 VDC
2. V_{CLAMP} = −3.0 VDC
3. MEASURE V_{OUT}; V_{OUT} SHALL BE WITHIN ±0.4 VDC OF V_{CLAMP}.
4. REPEAT STEPS 1, 2, 3 USING BOTH VOLTAGES OF OPPOSITE POLARITY.
5. REPEAT STEPS 1 THRU 4 USING A VALUE OF 6 VDC IN STEP 2.

	MIN	MAX
6. I =	− 1.0mA	− 3.3mA
	+ 0.5mA	+ 3.0mA

IRRADIATION CIRCUIT



BURN-IN CIRCUIT



V_{IN} = 50 KHz SQUARE WAVE 50% DUTY CYCLE −4.0V TO +4.0V

HS-3530RH

Low Power-
Radiation Resistant
Programmable Operational Amplifier

Features

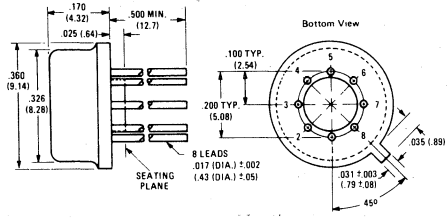
- WIDE RANGE AC PROGRAMMING
  - SLEW RATE 06 TO3V/μs
  - GAIN X BANDWIDTH . . . . . 100KHz TO 5.0MHz
- WIDE RANGE DC PROGRAMMING
  - POWER SUPPLY RANGE . . . . . $\pm$1.5V TO $\pm$18V
  - SUPPLY CURRENT . . . . . 10μA TO 1.2mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE(ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE(γ) . . . . . 1×10^6 RADS (Si)

Description

The HS-3530 is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as $\pm$3 volts may be used with little degradation of AC performance. The HS-3530 has been specifically designed to meet exposure to radiation environments. Operation from -55°C to $+125^{\circ}$C is guaranteed.

A major advantage of the HS-3530 is that operating characteristics remain virtually constant over a wide supply range (+3V to +15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters.

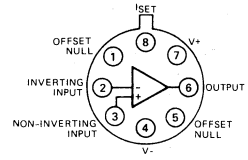
Package



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions $\pm$ .010 ($\pm$0.25mm) unless otherwise shown.

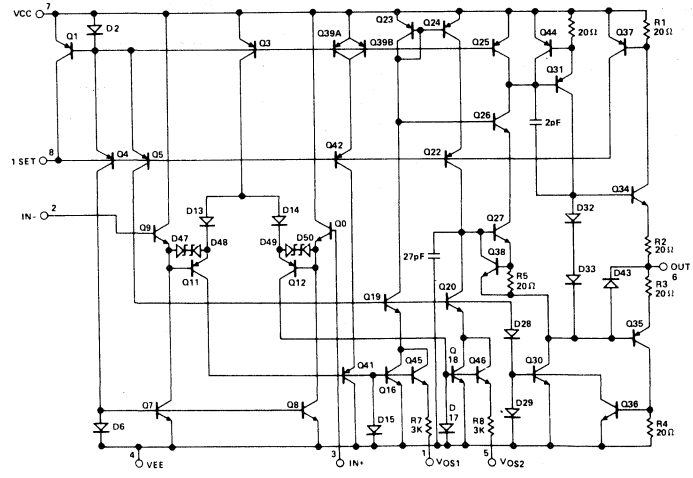
Pinout

TOP VIEW



NOTE: Case tied to V-

Schematic



ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- terminals	40V
Differential Input Voltage	±20V
Input Voltage (Note 1)	±15V

I_{SET} (current at I_{SET})	500μA
V_{SET} (voltage to ground at I_{SET})	(V+ -2.0V)<V_{SET}<V+
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

NOTE:
① For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PRE-RADIATION ELECTRICAL CHARACTERISTICS

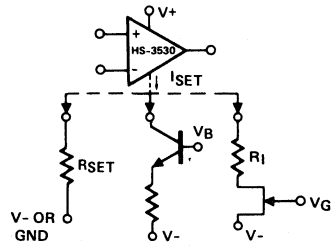
V_{SUPPLY} = ±15V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Offset Voltage	25°C		1	3		1	3	mV
	Full			5			5	mV
Input Bias Current	25°C		1.2			10	20	nA
	Full		2.5			22	40	nA
Input Offset Current	25°C		0.3			2	5	nA
	Full						10	nA
Input Resistance	25°C		>100		50	>100		MΩ
Large Signal Voltage Gain[1]	25°C	65K	115K		80K	130K		V/V
	Full	25K	60K		50K	70K		V/V
Common Mode Rejection Ratio[2]	25°C	80	115		80	115		dB
	Full				80	110		dB
Supply Current	25°C		13	15		125	150	μA
	Full		14	15		130	160	μA
Power Supply Rejection Ratio[3]	25°C	80	130		80	130		dB
	Full				80	120		dB
Output Voltage Swing[2]	25°C	±12.5	±14.2		±12.5	±14.2		V
	Full	±10.5	±14.0		±10.5	±14.0		V
Output Current	25°C		±.5			±5		mA
	Full		±.4			±4		mA
Output Short-Circuit Current	25°C		2			14		mA
Gain-Bandwidth Product	25°C		85			850		kHz
	Full		65			640		kHz
Slew Rate[5]	25°C		.05			.55		V/μS
Rise Time[4]	25°C		7.5			.7		μS
Overshoot[4]	25°C		5			10		%
Overdrive Recovery Time	25°C					2		μS

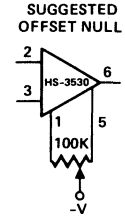
V_{SUPPLY} = ±3V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Large Signal Voltage Gain[1]	25°C	25K	60K		25K	75K		V/V
	Full	15K	40K		25K	50K		V/V
Common Mode Rejection Ratio[2]	25°C	80	100		80	95		dB
	Full	80	90					dB
Supply Current	25°C		12	15		115	150	μA
	Full			15			160	μA
Power Supply Rejection Ratio[3]	25°C	80	105		80	105		dB
	Full	80	100					dB
Output Voltage Swing[1]	25°C	±2.0			±2.0			V
	Full	±2.0			±2.0			V
Gain-Bandwidth Product	25°C		72			730		kHz
	Full		60			600		kHz
Slew Rate[5]	25°C		04			.4		V/μS
Offset Voltage	25°C		1	3		1	3	mV
	Full			5			5	

NOTES:

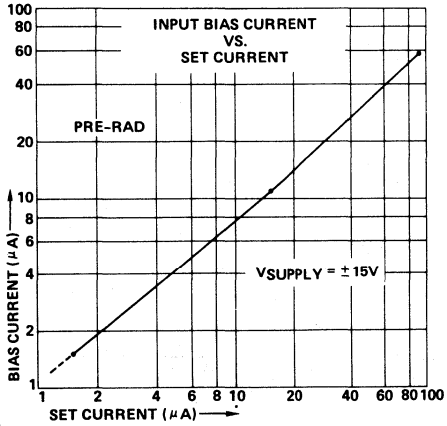
	$V_{SUPPLY} = \pm 3.0V$	$V_{SUPPLY} = \pm 15.0V$	$I_{SET} = 1.5\mu A$	$I_{SET} = 15\mu A$
1.	$V_O = \pm 1.0V$	$V_O = \pm 10.0V$	$R_L = 75K$	$R_L = 5K$ +25°C +125°C $R_L = 75K$ -55°C
2.	$V_{CM} = \pm 1.5V$	$V_{CM} = \pm 5.0V$		
3.	$V = \pm 1.5V$	$\Delta V = \pm 5.0V$		
4.	← $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5K$, $C_L = 100pF$ →			
5.	$V_O = \pm 2.0V$	$V_O = \pm 10.0V$	$R_L = 20K$	$R_L = 5K$ +25°C +125°C $R_L = 75K$ -55°C

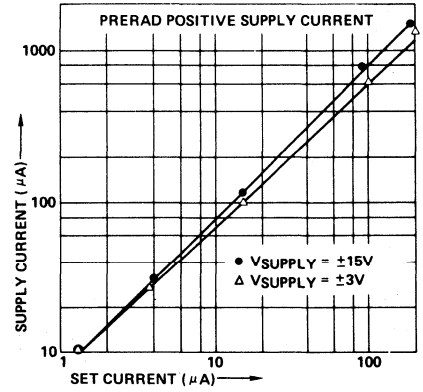
Typical Biasing Circuits

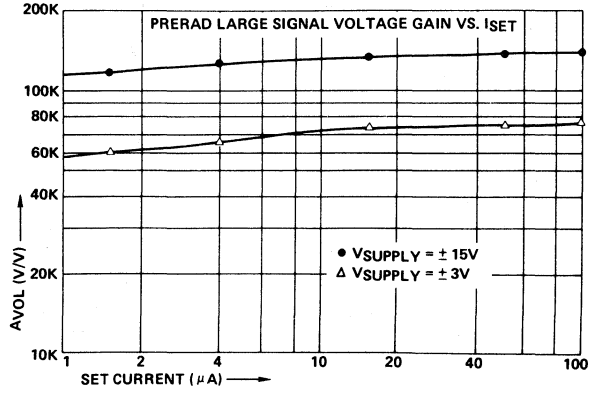




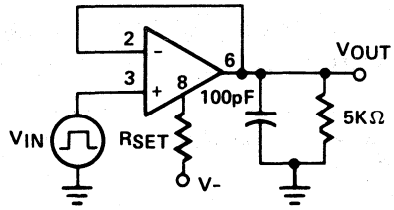
Typical Performance Curves

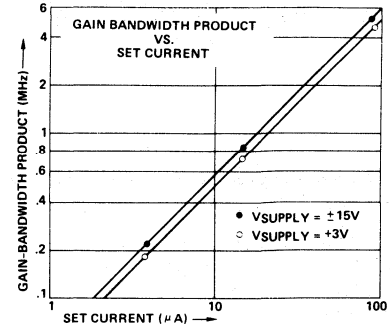




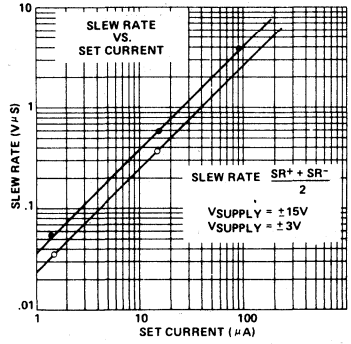


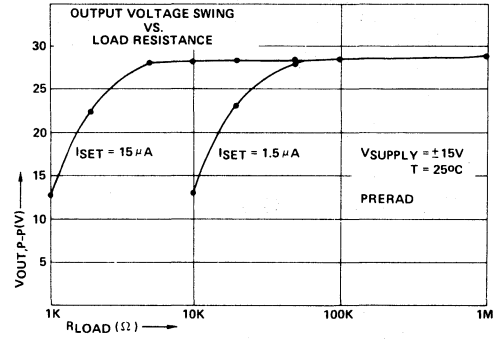
Transient Response/Slew Rate Circuit

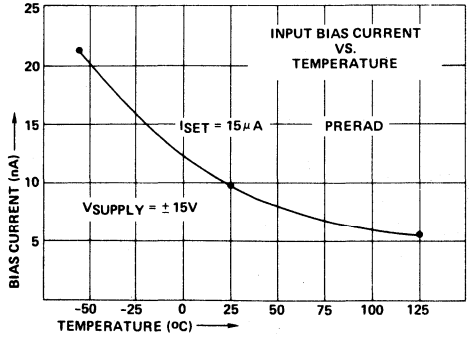


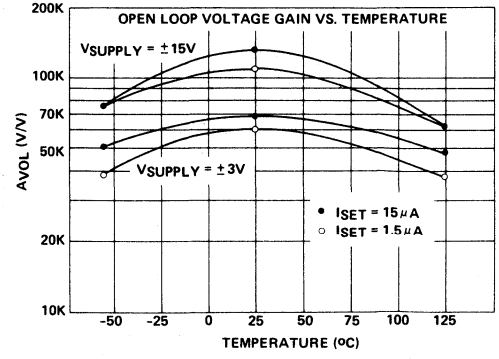


Typical Performance Curves









11

CICD

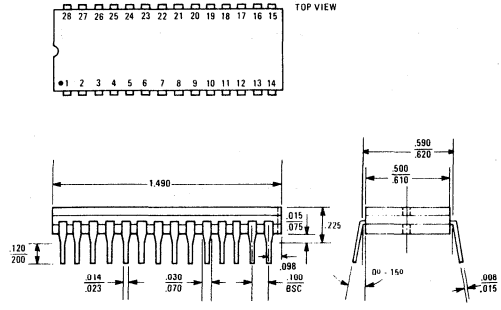
HS-1840RH

Radiation Resistant 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

Features

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) — 500MΩ
- LOW POWER CONSUMPTION (STANDBY) — 600μW
- ACCESS TIME — 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) 1 x 10^{13} n/cm^2 ($E \geq 10$KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1 x 10^8 RADs (Si)/s
  - GAMMA DOSE (γ) . . . . . 2 x 10^5 RADs(Si)

Package



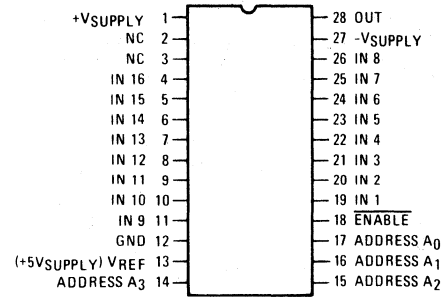
Description

The HS-1840RH is a radiation resistant, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

The HS-1840RH has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

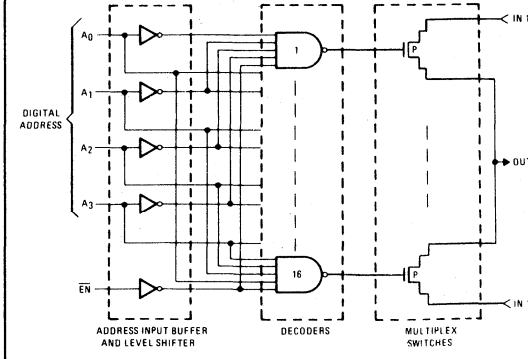
Pinout

TOP VIEW



CAUTION: These devices are sensitive to electronic discharge.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{REF} +4V
Ground -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +20V
V_{Supply} (-) -20V

Total Power Dissipation* 1200mW
Operating Temperature -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		μs
(0.025%)	+25°C		4.1		μs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

Truth Table

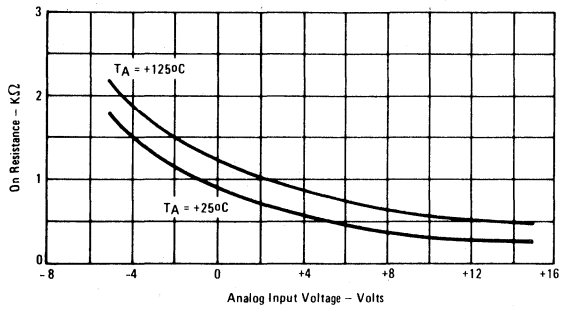
A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

Performance Characteristics and Test Circuits

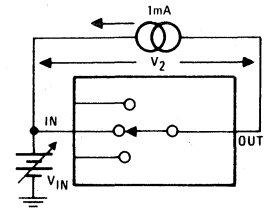
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = 5V$.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

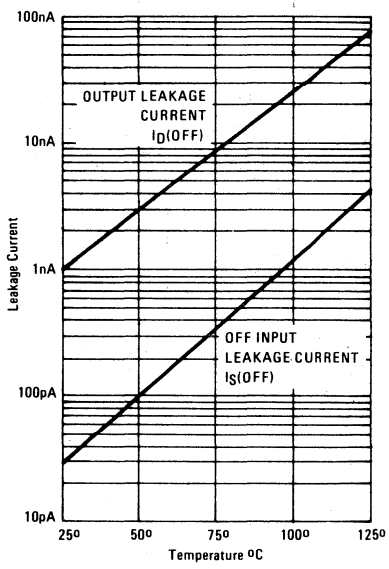


ON RESISTANCE vs INPUT SIGNAL LEVEL

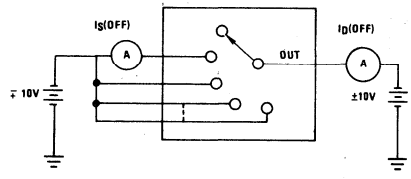
$R_{ON} = \frac{V_2}{1mA}$



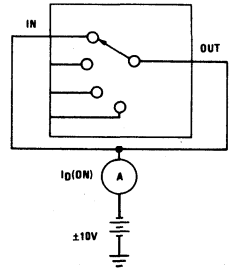
LEAKAGE CURRENT VS. TEMPERATURE



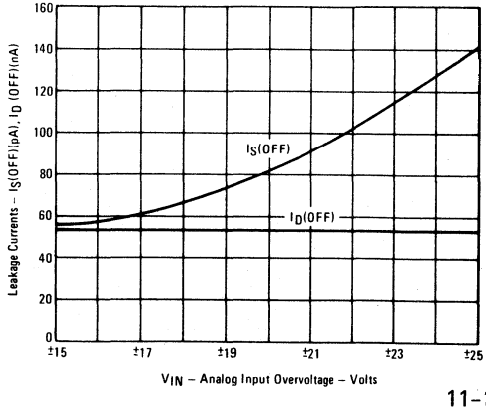
OFF LEAKAGE CURRENT vs TEMPERATURE



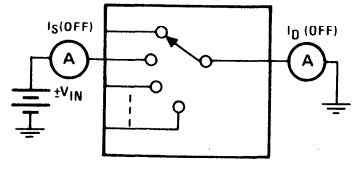
ON LEAKAGE CURRENT vs TEMPERATURE



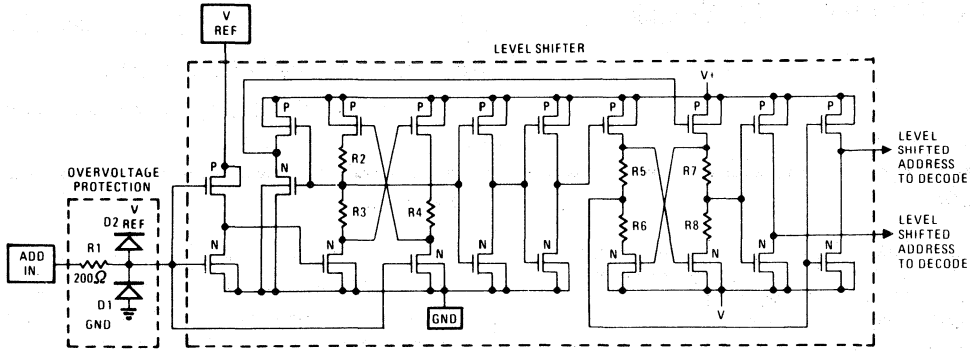
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



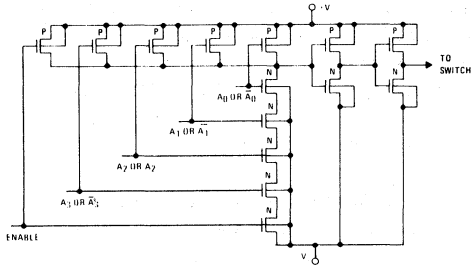
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



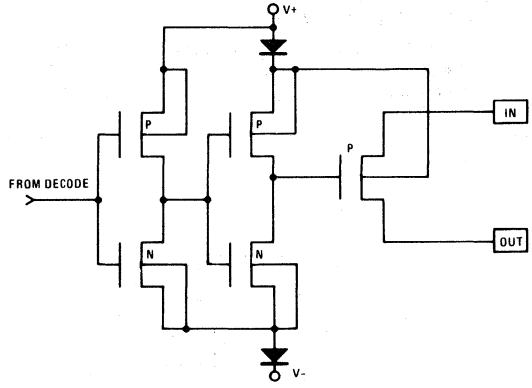
ADDRESS AND ENABLE INPUT BUFFER AND LEVER SHIFTER



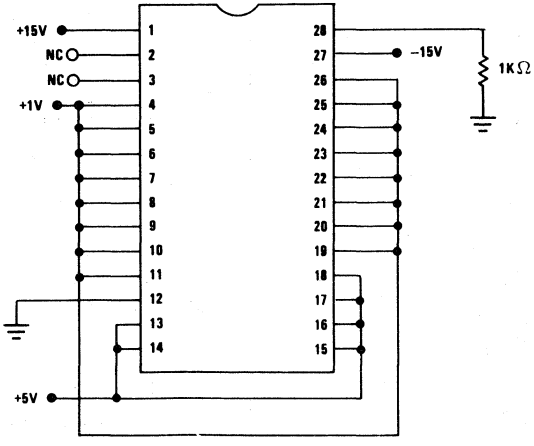
ADDRESS DECODER



MULTIPLEXER SWITCH



HS1840RH IRRADIATION CONFIGURATION



HS-508ARH

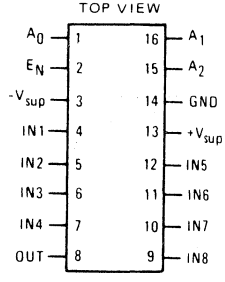
Radiation Resistant 8 Channel CMOS Analog Multiplexer With Overvoltage Protection

Features

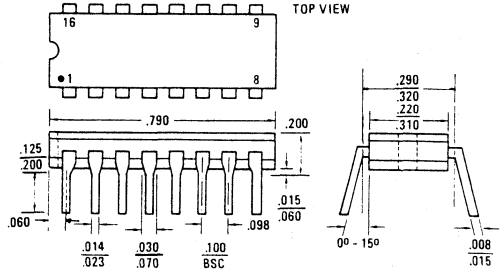
- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW
- RADIATION ENVIRONMENT

NEUTRON FLUENCE (ϕ) 1×10^{13} n/cm^2 (E $\geqslant$10KeV)
GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^{8} RADs(Si)/s
GAMMA DOSE (γ) . . . . . 1×10^{5} RADs(Si)

Pinout



Package

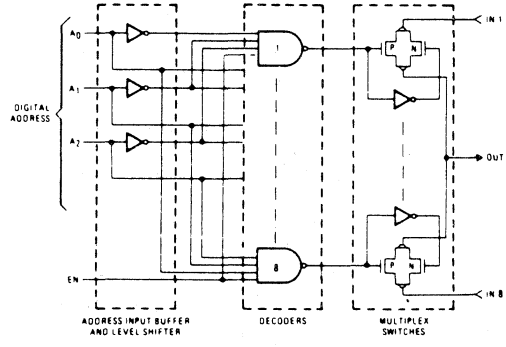


Description

The HS-508ARH is a dielectrically isolated, radiation resistant, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily,ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Analog Products Division of Harris, for further information on the 508A multiplexer in general.

The HS-508ARH has been specifically designed to meet exposure to radiation environments. Operation from –55°C to +125°C is guaranteed.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A | V_{Supply} (+) +4V
V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S | V_{Supply} (+) +20V
V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature -55°C to +125°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5	KΩ
	Full		1.5	1.8	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03		nA
	Full			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0		nA
	Full			±250	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0		nA
	Full			2.0	µA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1		nA
	Full			±250	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold (Note 6)	Full			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5	1.0	µs
t_{OPEN}, Break - Before Make Delay	+25°C		80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300		ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		3.5		µs
"OFF Isolation" (Note 3)	+25°C		65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		25		pF
C_A, Digital Input Capacitance	+25°C		5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0	mA
*I-, Current (Note 4)	Full		0.02	1.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0	mA

Truth Table

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

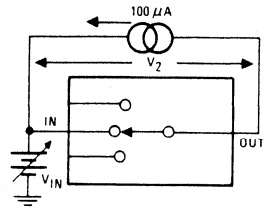
NOTES:
1. V_{OUT} = ± 10V, I_{OUT} = -100µA
2. Analog Overvoltage = ± 33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

* 100% Tested for Dash 8 at +25°C and +125°C Only.

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

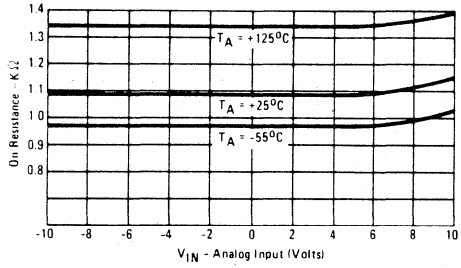
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

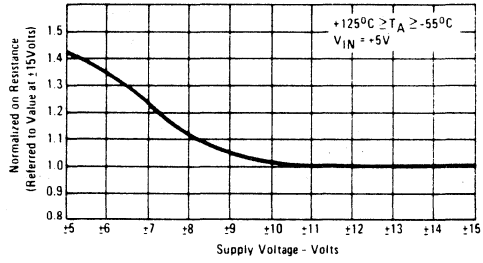


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

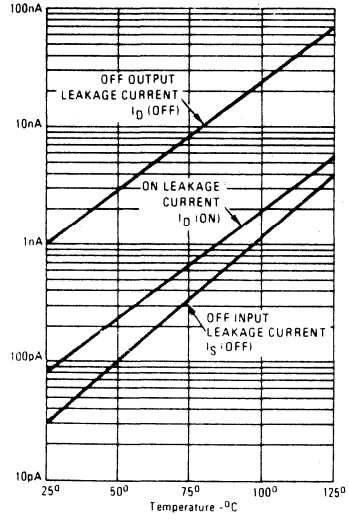
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

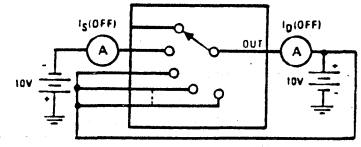


LEAKAGE CURRENT vs. TEMPERATURE



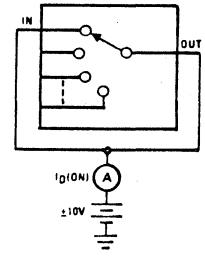
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

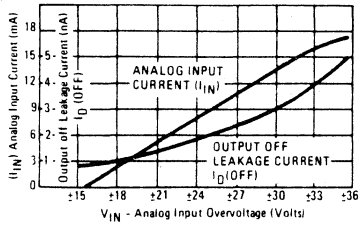


TEST CIRCUIT NO. 3

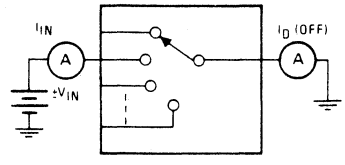
ON LEAKAGE CURRENT vs. TEMPERATURE



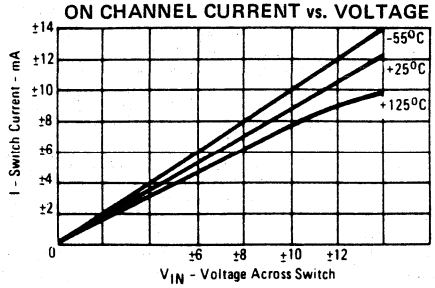
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



TEST CIRCUIT NO. 4

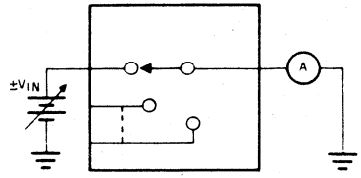


ON CHANNEL CURRENT vs. VOLTAGE

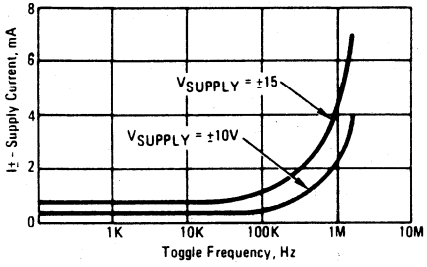


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

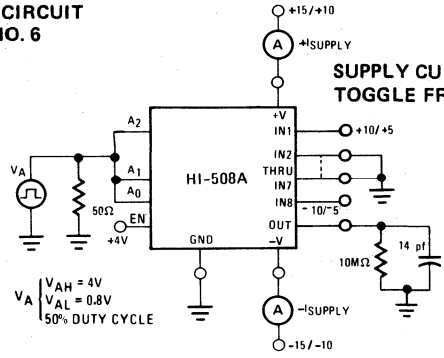


SUPPLY CURRENT vs. TOGGLE FREQUENCY

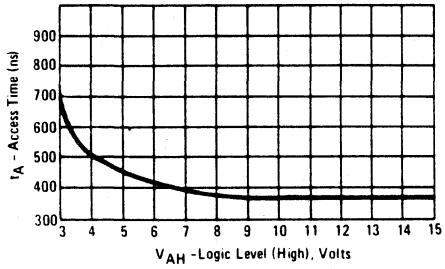


TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY

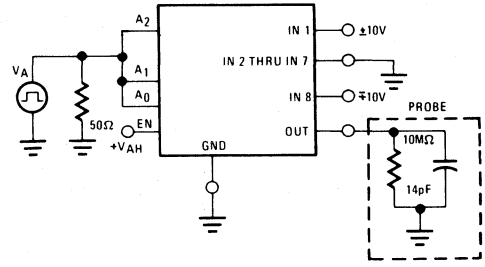


ACCESS TIME vs. LOGIC LEVEL (HIGH)

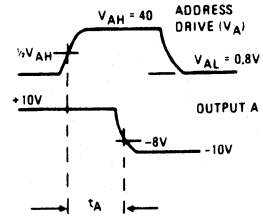


TEST CIRCUIT NO. 7

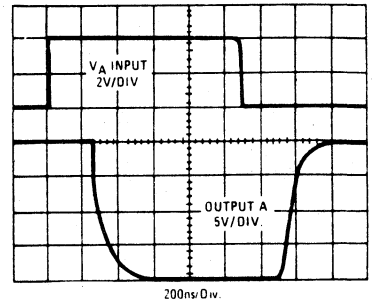
ACCESS TIME vs. LOGIC LEVEL (HIGH)



Switching Waveforms

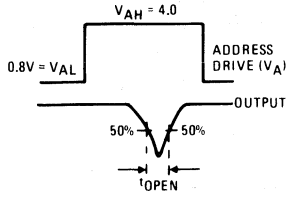


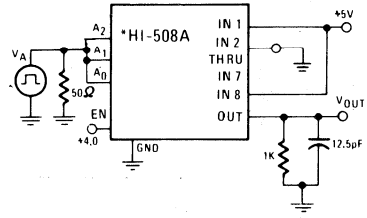
ACCESS TIME



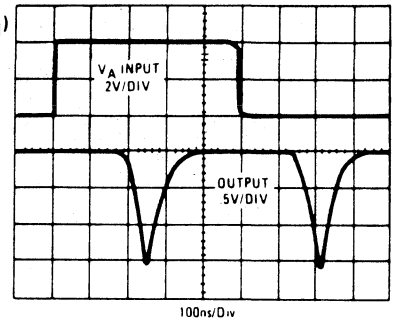
Switching Waveforms (continued)

TEST CIRCUIT
NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})

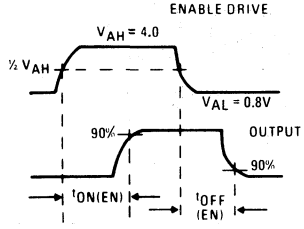


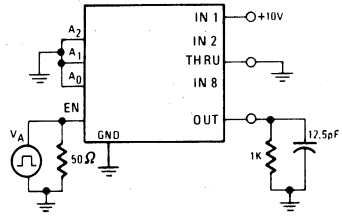


BREAK BEFORE MAKE DELAY (t_{OPEN})

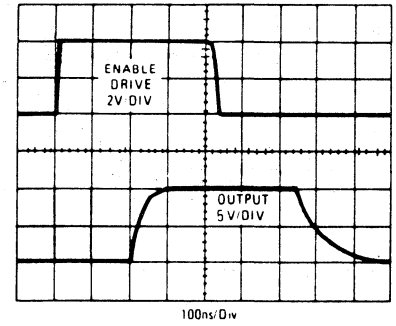


TEST CIRCUIT
NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



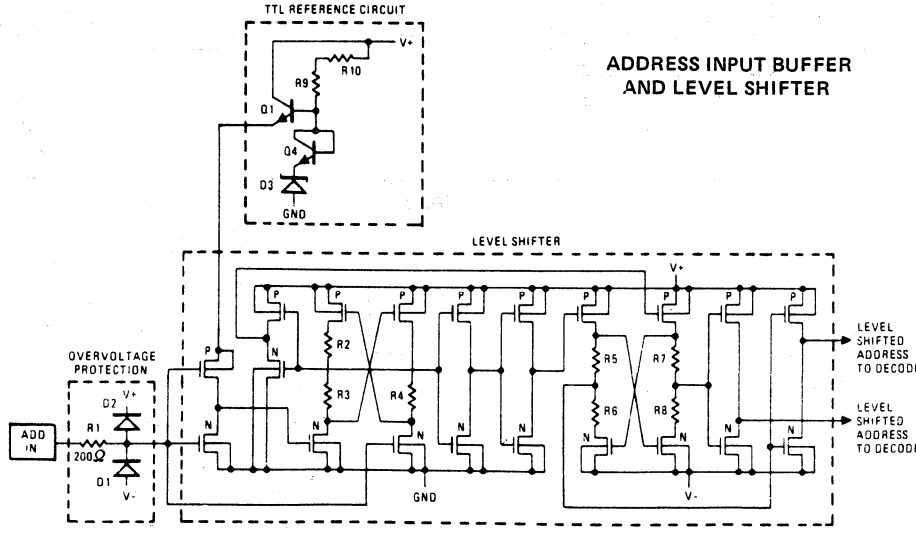


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

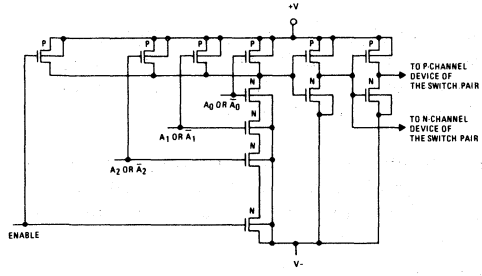


Schematic Diagrams

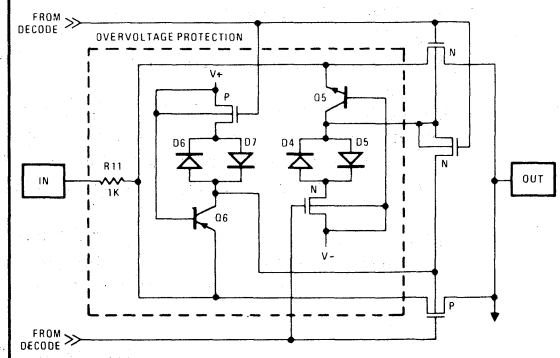
ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad (Si) ±10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with $V_{SUPPLY} = \pm 15V$. The dose rate shall be between 50 rads/sec and 200 rads/sec.

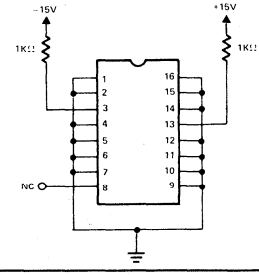
(4) On Current Leakage $I_{D(ON)}$ with $V_{SUPPLY} = \pm 15V$ will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample meets the limit of $I_{D(ON)} \leq 1\mu A$ when tested at 25°C.

Radiation Effects

(1) TOTAL DOSE:
Very little degradation of any of the parameters will be seen up to $\gamma = 1 \times 10^5$ Rad (Si).

(2) DOSE RATE:
The HS508A RH is manufactured in DI, consequently, it is latch up free.

Irradiation Bias Circuit



Harris Analog/Digital Mix

In addition to the available full custom analog design approaches, standard analog building blocks have been developed at Harris for custom and semicustom designs using a digital CMOS process. This allows a mix of high performance digital and medium performance and medium performance analog circuitry to be combined on a single silicon die.

Many systems require the integration of both analog and digital functions. The ability to combine both types of circuitry on the same chip has numerous advantages. Reducing the number of components in a system by taking advantage of this technology can increase system reliability, while decreasing system size, cost, and power consumption.

Typical performance of the analog cells designed and built on a digital process proves to be adequate for most applications, though high resolution circuits such as data acquisition systems may require the increased performance obtained only with a dedicated linear process.

Analog CMOS

The Harris SAJI process can be used to fabricate many analog circuits. Typical analog functions that have been implemented include:

- Operational Amplifiers
- Comparators
- Oscillators
- Switched Capacitor Filters
- Voltage References
- Current References
- Voltage Multipliers (3X)
- Analog Switches
- Analog/Digital Functions on the Same Chip

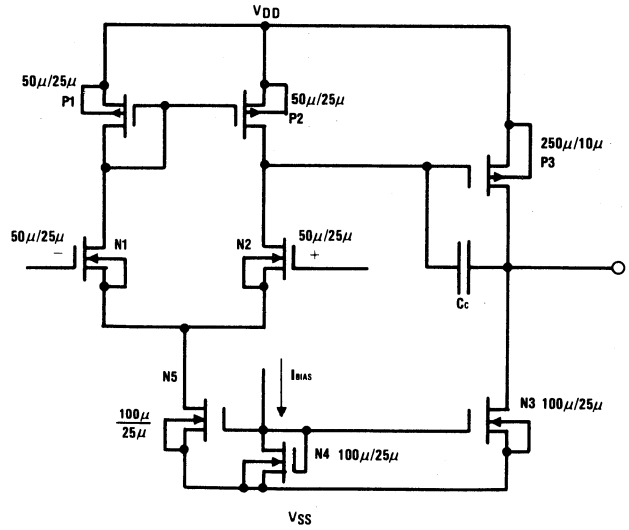


Figure 1. (a) Ckt. Schematic of Basic Amplifier.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Offset Voltage			5	15	MVolts
Voltage Gain	V_{DD} = +2.5Volts	158	224	251	V/MV
Supply Current	V_{SS} = -2.5 Volts		800		ηAmps
Output Voltage Range	-55°C<T_A<125°C	V_{SS}		V_{DD}	Volts
Input Common Mode Range	I_{BIAS} = 200nA CL = 0.5pF	V_{SS} +1.3		V_{DD} -.75	Volts
Common Mode Rejection Ratio @ 1KHz		58	61	64	dB
Unity Gain BW		43	58	78	KHz
Slew Rate		.027	.039	.042	Volt/μS

Figure 1. (b) Performance Table for Basic Amplifier Operating in Sub-Threshold.

The Amplifier building blocks have been used in a variety of applications. The op amps have been implemented as bandpass filters with external resistor-capacitor networks, two pole switch capacitor filters, comparators, programmable voltage sources with three digitally controlled feedback resistors, and voltage reference designs. The basic amplifier has also been designed for operation in the subthreshold current region. The low current consumption is attractive for many applications such as implantable medical electronics.

Military Program Field Managers

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
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106 Seventh Street
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516-747-6776
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TWX: 710-332-1074
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TWX: 510-959-6259

EUROPE

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P. O. Box 27
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Slough SL1 4XD, ENGLAND
011-447-5334666
Telex: 848174 Harris G

ANALOG

Chip Information

12

GENERAL INFORMATION

Harris Analog Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested to the data sheet limits for the commercial device and are 100% visually inspected. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are available through Harris authorized chip suppliers or direct from the factory. Contact the local Harris Sales Office for pricing and delivery information. (Minimum quantities may apply).

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ±.003". Maximum chip thickness is .019" + .001".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

DICE GEOMETRIES AND DIMENSIONS

May be obtained by contacting the factory or your local Harris Sales Office.

PRODUCT CODE EXAMPLE

H A 0 - 4741 - 6

PREFIX:
H (Harris)

FAMILY:
A = Analog
C = Communication
D = Digital
F = Filter
I = Interface
M = Memory
V = Analog, High Voltage

0 = Chip Form

MODEL NUMBER

TEMPERATURE:
6 = 25°C Probe*
*Contact Harris for availability of -2 (-55°C to +125°C) dice

ANALOG

Packaging 13

Analog Package Selection Guide 13-3

Package Configurations 13-5

Harris Analog Package Selection Guide

PART NUMBER	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HA-OP07	U	M	A		
HA-1608	U				
HA-2400/04/05			C	H	
HA-2420/25		N	B		S
HA-2500/02/05	U	M	A		
HA-2510/12/15	U	M	A		
HA-2520/22/25	U	M	A		
HA-2539		N	B		S
HA-2540		N	B		
HA-2600/02/05	U	M	A		
HA-2620/22/25	U	M	A		
HA-2630/35	W				
HA-2640/45	U		A		
HA-2650/55	U	M	A		
HA-2720/25	U		A		
HA-2730/35			B		
HA-2740		O	C		
HA-4156		N	B		
HA-4600/02/05		N	B		
HA-4620/22/25		N	B		
HA-4640			B		
HA-4741		N	B		S
HA-4900/02/05			C		S
HA-5033	W	M			
HA-5062	U	M	A		
HA-5064		N	B		
HA-5082	U	M	A		
HA-5084		N	B		
HA-5100/05	U	M	A		
HA-5102/5112	U	M	A		
HA-5104/5114		N	B		S
HA-5110/15	U	M	A		
HA-5130/35	U	M	A		S
HA-5141	U	M	A		
HA-5142	U	M	A		
HA-5144		N	B		
HA-5160/62	U				
HA-5170	U	M	A		S
HA-5180	U	M	A		
HA-5190/95	W		B		
HA-5320			B		
HA-23080	U	M	A		
HA-23551		N	B		
HC-5502		Q	E		
HC-5502A		Q	E		
HC-5504		Q	E		
HC-5510			E		
HC-5511			*		
HC-5512/12A			C		
HC-5512C			C		

NOTE: "Package Configuration" references drawings on the following pages. Package designations constructing the part number are explained in the Ordering Information, Section 1 - X.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products.

Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP, and "dimension G" in metal cans.

*Contact factory for packaging.

Harris Analog Package Selection Guide (continued)

PART NUMBER	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HC-5521A		R			
HC-55536		*	B		
HC-55564		*	B		S
HD-0165			E		
HF-10		Y	X		S
HI-200	V	N	B		
HI-201		O	C		S
HI-201HS		O	C		S
HI-300/301/304/305	V	N	B		
HI-302/303/306/307		N	B		
HI-381/384/387/390					
HI-381/387	V	N	B		
HI-384/390		O	C		
HI-506/507		R	F		T
HI-506A/507A		R	F		T
HI-506L/507L		R	F		
HI-508/509		O	C		S
HI-508A/509A		O	C		S
HI-508L/509L		P	D		
HI-516		R	F		T
HI-518		P	D		
HI-524		P	D		
HI-539		O	C		
HI-562A		Q		J	T
HI-565A		Q		J	
HI-574A				K	
HI-674A				K	
HI-1818A/28A		O	C		
HI-5040 thru 5051		O	C		
HI-5043/45		O	C		S
HI-5610		Q		J	
HI-5618A/18B		P	D		
HI-5660/60A		Q		J	
HI-5680/85/85A/87		Q		J	
HI-5712/12A	(MC) LCC's on Ceramic Substrate				
HI-5900	(MB) LCC's on Ceramic Substrate				
HI-5901	(MB) LCC's on Ceramic Substrate				
HI-7541		P		I	S
HI-DAC16B/C				L	
HV-1000/1000A		O			
LF 147, 247, 347		N	B		
LF353	U	M	A		
LM118/318	U	M	A		
LM143/343	U	M	A		

NOTE: "Package Configuration" references drawings on the following pages. Package designations constructing the part number are explained in the Ordering Information, Section 1 - X.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products.

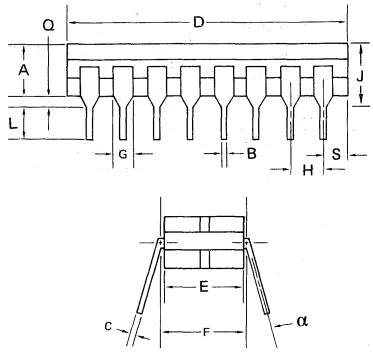
Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP, and "dimension G" in metal cans.

* Contact factory for packaging.

Package Configuration

A J-8 TYPE 8 PIN MINI-CERDIP DUAL-IN-LINE .300

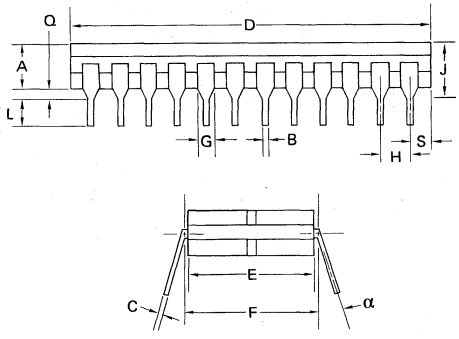
B C D X J TYPE CERDIP DUAL-IN-LINE .300



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. L	DIM. Q	DIM. S	DIM. α
A	8	.140/.170	.016/.018	.008/.012	.375/.405	.245/.265	.290/.310	.050/.070	.090/.110	—/.200	.125/.150	.020/.040	.020/.040	0°/15°
B	14	.140/.170	.016/.018	.008/.012	.760/.790	.265/.285	.290/.310	.050/.070	.090/.110	—/.200	.125/.150	.020/.040	.025/.045	0°/15°
C	16	.140/.170	.016/.018	.008/.012	.760/.790	.265/.285	.290/.310	.050/.070	.090/.110	—/.200	.125/.150	.020/.040	.025/.045	0°/15°
D	18	.140/.170	.016/.018	.008/.012	.885/.915	.285/.305	.300/.320	.050/.070	.090/.110	—/.200	.125/.150	.020/.040	.040/.060	0°/15°
X	20	.140/.170	.016/.018	.008/.012	.940/.970	.285/.305	.300/.320	.050/.070	.090/.110	—/.200	.125/.150	.020/.040	.020/.040	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

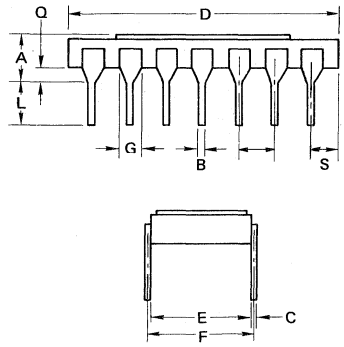
E F J TYPE CERDIP DUAL-IN-LINE .600



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. L	DIM. Q	DIM. S	DIM. α
E	24	.150/.180	.016/.018	.008/.012	1.24/1.27	.515/.535	.595/.615	.050/.070	.090/.110	—/.225	.125/.150	.020/.045	.060/.090	0°/15°
F	28	.160/.190	.016/.018	.008/.012	1.44/1.47	.515/.535	.595/.615	.050/.070	.090/.110	—/.225	.125/.150	.020/.060	.060/.090	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

G H I D TYPE SIDE BRAZED CERAMIC DUAL-IN-LINE .300



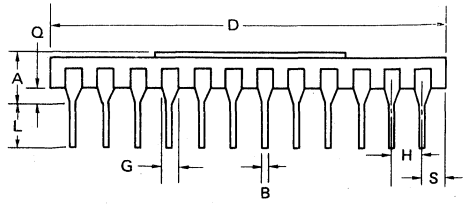
PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
G	14	—/.200	.016/.020	.008/.012	—/.785	—/.300	.290/.310	.045/.055	.100/BSC	.125/.160	.025/.045	.040/.060
H	16	—/.200	.016/.020	.008/.012	—/.840	—/.300	.290/.310	.045/.055	.100/BSC	.125/.160	.025/.045	.040/.060
I	18	—/.200	.016/.020	.008/.012	—/.950	—/.300	.290/.310	.045/.055	.100/BSC	.125/.160	.025/.045	.040/.060

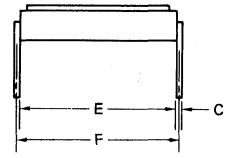
NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches
3) BSC Means Basic Spacing Between Centerlines

13 PACKAGING

Package Configuration

J K L D TYPE SIDE BRAZED CERAMIC DUAL-IN-LINE .600

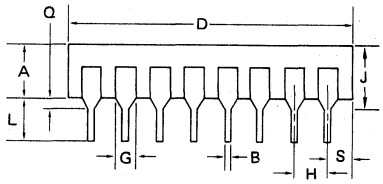


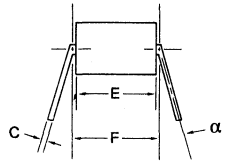


PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
J	24	— .225	.016 .020	.008 .012	1.185 1.215	.587 .603	.590 .610	.045 .055	.100 BSC	.120 .160	.040 .060	.040 .060
K	28	— .225	.016 .020	.008 .012	1.385 1.415	.587 .603	.590 .610	.045 .055	.100 BSC	.120 .160	.040 .060	.040 .060
L	40	— .225	.016 .020	.008 .012	1.980 2.020	.587 .603	.590 .610	.045 .055	.100 BSC	.120 .160	.040 .060	.040 .060

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches
3) BSC Means Basic Spacing Between Centerlines

M N O P Y N TYPE PLASTIC DUAL-IN-LINE .300

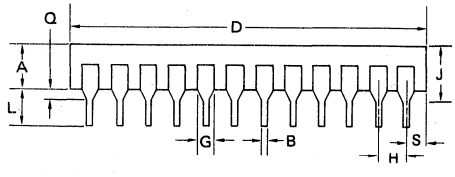


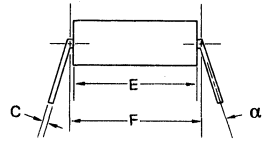


PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. L	DIM. Q	DIM. S	DIM. α
M	8	.125 .140	.016 .020	.008 .012	.370 .390	.245 .265	.290 .310	.050 .070	.090 .110	— .200	.150 .170	.020 .040	.030 .050	0° 15°
N	14	.125 .140	.016 .020	.008 .012	.750 .770	.245 .265	.290 .310	.050 .070	.090 .110	— .200	.150 .170	.020 .040	.030 .050	0° 15°
O	16	.125 .140	.016 .020	.008 .012	.750 .770	.245 .265	.290 .310	.050 .070	.090 .110	— .200	.150 .170	.020 .040	.025 .045	0° 15°
P	18	.125 .140	.016 .020	.008 .012	.900 .920	.245 .265	.290 .310	.050 .070	.090 .110	— .200	.150 .170	.020 .040	.040 .060	0° 15°
Y	20	.130 .145	.016 .020	.008 .012	1.030 1.050	.250 .270	.290 .310	.050 .070	.090 .110	— .200	.150 .170	.020 .040	.060 .080	0° 15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Q R N TYPE PLASTIC DUAL-IN-LINE .600



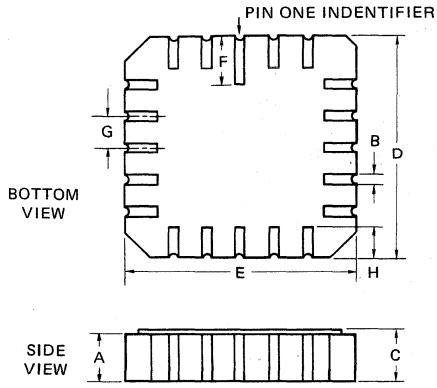


PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. L	DIM. Q	DIM. S	DIM. α
Q	24	.145 .165	.016 .020	.008 .012	1.24 1.26	.540 .560	.590 .610	.050 .070	.090 .110	— .225	.150 .170	.020 .040	.065 .085	0° 15°
R	28	.145 .165	.016 .020	.008 .012	1.54 1.57	.540 .560	.590 .610	.050 .070	.090 .110	— .225	.150 .170	.020 .040	.110 .130	0° 15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Package Configuration

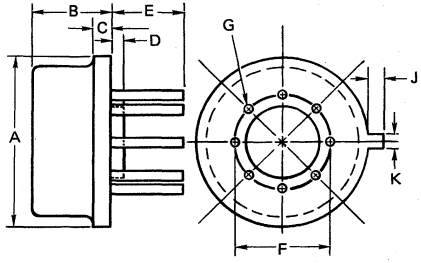
S T LEADLESS CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H
S	20 .350 SQ	.050 .078	.020 .030	.060 .090	.342 .358	.342 .348	.060 .095	.050 BSC	.040 .055
T	28 .450 SQ	.050 .078	.020 .030	.060 .090	.442 .458	.342 .348	.060 .095	.050 BSC	.040 .055

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches
3) BSC Means Basic Spacing Between Centerlines

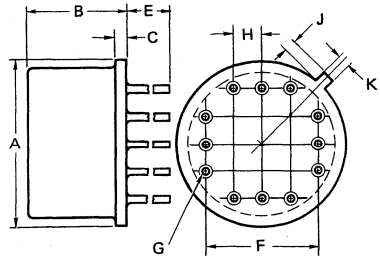
U V H TYPE METAL CAN, T0-99 (8 PIN) OR T0-100 (10 PIN)



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. J	DIM. K
U	8	.345 .365	.165 .185	.020 .040	.010 .045	.500 .550	.200 BSC	.016 .021	.027 .045	.027 .034
V	10	.345 .365	.165 .185	.020 .040	.010 .045	.500 .550	.230 BSC	.016 .021	.027 .045	.027 .034

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches
3) BSC Means Basic Spacing Between Centerlines

W H TYPE METAL CAN, T0-8

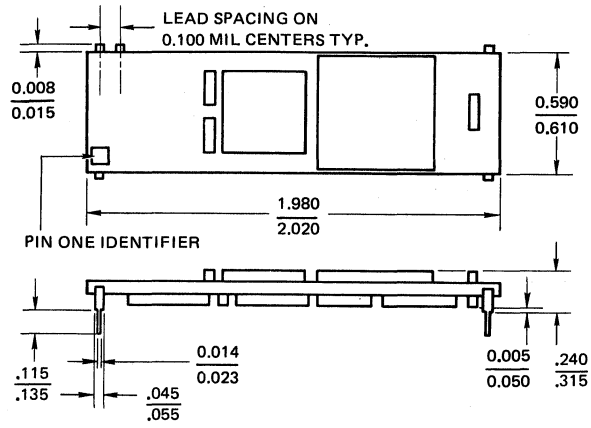


PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. K
W	12	.585 .615	.130 .150	— .040	.500 .550	.400 BSC	.016 .021	.100 BSC	.027 .045	.027 .045

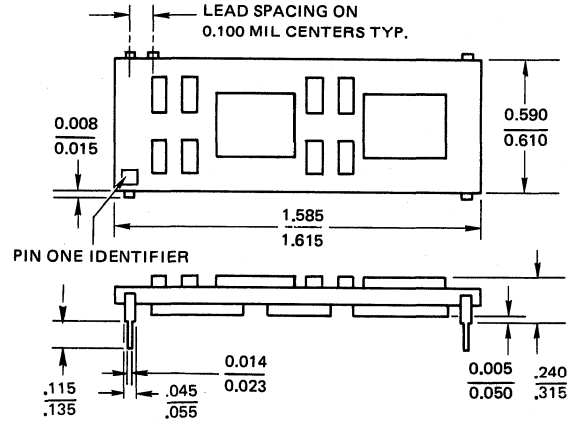
NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches
3) BSC Means Basic Spacing Between Centerlines

Package Configuration

HI-5712/12A MODULE



MB HI-5900/5901 MODULE



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